RCA Solid State

new

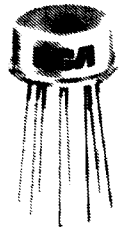
CA5130A, CA5130

Linear Integrated Circuits

Advance Information

(E Suffix)
(M Suffix)
Not Shown

(S Suffix)



(T Suffix)

BiMOS Microprocessor Operational Amplifiers

With MOSFET Input/CMOS Output

Features:

- *MOSFET input stage provides:*
  very high Z_I = 1.5 TΩ (1.5 x 10^{12}Ω) typ.
  very low I_I = 5 pA typ. at 15-V operation
  = 2 pA typ. at 5-V operation
- *Common-mode input-voltage range includes negative supply rail; input terminals can be swung 0.5 V below negative supply rail*
- *CMOS output stage permits signal swing to either (or both) supply rails*

} *Ideal for single-supply applications*

RCA-CA5130A and CA5130 are integrated-circuit operational amplifiers that combine the advantages of both CMOS and bipolar transistors on a monolithic chip. They are designed and guaranteed to operate in microprocessors or logic systems that use +5 V supplies.

Gate-protected p-channel MOSFET (PMOS) transistors are used in the input circuit to provide very-high-input impedance, very-low-input current, and exceptional speed performance. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute in single-supply applications.

A complementary-symmetry MOS (CMOS) transistor-pair, capable of swinging the output voltage to within 10 millivolts of either supply-voltage terminal (at very high values of load impedance), is employed as the output circuit.

The CA5130 Series circuits operate at supply voltages ranging from 5 to 16 volts, or ±2.5 to ±8 volts when using split supplies. They can be phase compensated with a single external capacitor, and have terminals for adjustment of offset voltage for applications requiring offset-null capability. Terminal provisions are also made to permit strobing of the output stage.

The CA5130 Series is supplied in standard 8-lead TO-5 style packages (T suffix), 8-lead dual-in-line formed lead TO-5 style "DIL-CAN" packages (S suffix). The CA5130 is available in chip form (H suffix). The CA5130 and CA5130A are also available in the Mini-Dip 8-lead dual-in-line plastic package (E suffix) and in 8-lead dual-in-line surface-mount plastic packages (M suffix).

The CA5130A, CA5130 have guaranteed specifications for 5 V operation over the full military range of -55°C to +125°C.

- *CA5130A, CA5130 5 V have full military temperature range guaranteed specifications*
- *CA5130A, CA5130 are guaranteed to operate down to V_T = 4.5 V for AOL*
- *CA5130A, CA5130 are guaranteed to operate at ±7.5 CA3130A, CA3130 specifications*

Applications:

- *Ground-referenced single-supply amplifiers*
- *Fast sample-hold amplifiers*
- *Long-duration timers/monostables*
- *High-input-impedance comparators (ideal interface with digital CMOS)*
- *High-input-impedance wideband amplifiers*
- *Voltage followers (e.g., follower for single-supply D/A converter)*
- *Voltage regulators (permits control of output voltage down to zero volts)*
- *Peak detectors*
- *Single-supply full-wave precision rectifiers*
- *Photo-diode sensor amplifiers*
- *5 V logic systems*
- *Microprocessors interface*

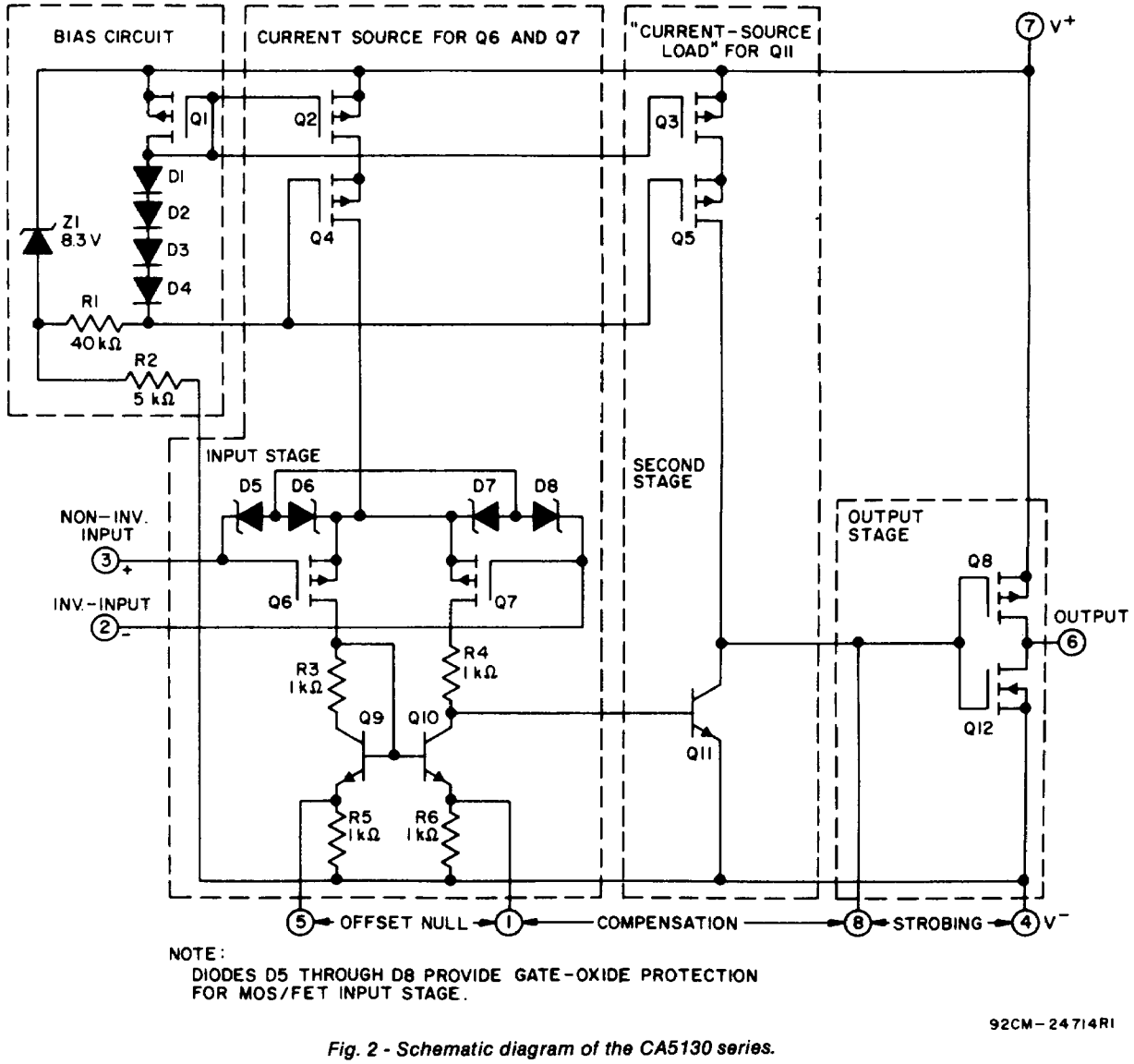
Printed in USA/4-87

File Number **1923**

MAXIMUM RATINGS, *Absolute-Maximum Values*

DC SUPPLY VOLTAGE
(Between V^+ and V^- Terminals) ..... 16 V
DIFFERENTIAL-MODE INPUT VOLTAGE ..... ±8 V
COMMON-MODE DC INPUT VOLTAGE ..... (V^+ +8V) to (V^- -0.5V)
INPUT-TERMINAL CURRENT ..... 1 mA
DEVICE DISSIPATION:
WITHOUT HEAT SINK -
UP TO 55°C ..... 630 mW
ABOVE 55°C ..... Derate Linearly 6.67 mW/°C
WITH HEAT SINK -
UP TO 90°C ..... 1 W
ABOVE 90°C ..... Derate Linearly 16.7 mW/°C
SMALL OUTLINE PACKAGE ..... 250°/W
TEMPERATURE RANGE:
OPERATING (all types) ..... -55 to +125°C
STORAGE (all types) ..... -65 to +150°C
OUTPUT SHORT-CIRCUIT DURATION * ..... INDEFINITE
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

* Short circuit may be applied to ground or to either supply.



NOTE:
DIODES D5 THROUGH D8 PROVIDE GATE-OXIDE PROTECTION FOR MOS/FET INPUT STAGE.

92CM-24714R1

Fig. 2 - Schematic diagram of the CA5130 series.

ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V^+ = 5 V, V^- = 0 V

CHARACTERISTIC		LIMITS						UNITS
		CA5130A			CA5130			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage V_O = 2.5 V	V_{IO}	—	1.5	4	—	2	10	mV
Input Offset Current V_O = 2.5 V	I_{IO}	—	0.1	5	—	0.1	10	pA
Input Current V_O = 2.5 V	I_I	—	2	10	—	2	15	pA
Common-Mode Rejection Ratio	C_{MRR}							dB
V_{CM} = 0 to 1 V		75	87	—	70	85	—	
V_{CM} = 0 to 2.5 V	C_{MRR}	60	69	—	60	69	—	
Input Common-Mode Voltage Range								V
	V_{ICR}^+	2.5	2.8	—	2.5	2.8	—	
	V_{ICR}^-	—	-0.5	0	—	-0.5	0	
Power-Supply Rejection Ratio Δ^+ = 1 V; Δ^- = 1 V	P_{SRR}	60	75	—	55	73	—	dB
Large-Signal Voltage Gain*	A_{OL}							dB
V_O = 0.1 to 4.1 V	R_L = ∞	100	105	—	95	105	—	
V_O = 0.1 to 3.6 V	R_L = 10 k	90	97	—	85	95	—	
Source Current V_O = 0 V	I_{SOURCE}	1.0	3.1	4.0	1.0	2.6	4.0	mA
Sink Current V_O = 5 V	I_{SINK}	1.0	1.6	4.0	1.0	1.7	4.0	mA
Output Voltage	V_{OUT}							V
R_L = ∞	V_{OM}^+	4.99	5	—	4.99	5	—	
	V_{OM}^-	—	0	0.01	—	0	0.01	
R_L = 10 k	V_{OM}^+	4.4	4.7	—	4.4	4.7	—	
	V_{OM}^-	—	0	0.01	—	0	0.01	
R_L = 2 k	V_{OM}^+	2.5	3.5	—	2.5	3.5	—	
	V_{OM}^-	—	0	0.01	—	0	0.01	
Supply Current	I_{SUPPLY}							μA
V_O = 0 V		—	50	100	—	50	100	
V_O = 2.5 V	I_{SUPPLY}	—	260	400	—	260	400	

*For V^+ = 4.5 V and V^- = Gnd; V_{OUT} = 0.5 V to 3.2 V at R_L = 10 k.

ELECTRICAL CHARACTERISTICS AT T_A = -55°C to +125°C, V^+ = 5 V, V^- = 0 V

CHARACTERISTIC		LIMITS						UNITS
		CA5130A			CA5130			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage V_O = 2.5 V	V_{IO}	—	2	10	—	3	15	mV
Input Offset Current V_O = 2.5 V	I_{IO}	—	0.1	5	—	0.1	10	pA
Input Current V_O = 2.5 V	I_I	—	2	10	—	2	15	pA
Common-Mode Rejection Ratio	C_{MRR}							dB
V_{CM} = 0 to 1 V		60	80	—	60	80	—	
V_{CM} = 0 to 2.5 V	C_{MRR}	55	80	—	50	80	—	
Input Common-Mode Voltage Range								V
	V_{ICR}^+	2.5	2.8	—	2.5	2.8	—	
	V_{ICR}^-	—	-0.5	0	—	-0.5	0	
Power-Supply Rejection Ratio Δ^+ = 1 V; Δ^- = 1 V	P_{SRR}	45	70	—	40	66	—	dB
Large-Signal Voltage Gain*	A_{OL}							dB
V_O = 0.1 to 4.1 V	R_L = ∞	94	98	—	90	98	—	
V_O = 0.1 to 3.6 V	R_L = 10 k	80	88	—	75	85	—	
Source Current V_O = 0 V	I_{SOURCE}	0.6	2.2	5.0	0.6	—	5.0	mA
Sink Current V_O = 5 V	I_{SINK}	0.6	1.15	5.0	0.6	—	5.0	mA
Output Voltage	V_{OUT}							V
R_L = ∞	V_{OM}^+	4.99	5	—	4.99	5	—	
	V_{OM}^-	—	0	0.01	—	0	0.01	
R_L = 10 k	V_{OM}^+	4.0	4.6	—	4.0	4.6	—	
	V_{OM}^-	—	0	0.01	—	0	0.01	
R_L = 2 k	V_{OM}^+	2.0	3.0	—	2.0	3.0	—	
	V_{OM}^-	—	0	0.01	—	0	0.01	
Supply Current	I_{SUPPLY}							μA
V_O = 0 V		—	80	220	—	80	220	
V_O = 2.5 V	I_{SUPPLY}	—	300	500	—	300	500	

*For V^+ = 4.5 V and V^- = Gnd; V_{OUT} = 0.5 V to 3.2 V at R_L = 10 k.

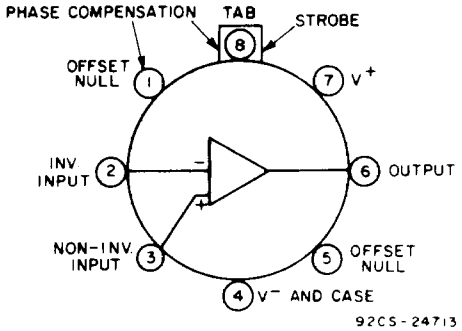
ELECTRICAL CHARACTERISTICS AT T_A = 25°C, V^+ = 15 V, V^- = 0 V (Unless otherwise specified)

CHARACTERISTIC		LIMITS						UNITS
		CA5130A (T, S, E)			CA5130 (T, S, E)			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage $V^{\pm}$ = ±7.5 V	V_{IO}	—	2	5	—	8	15	mV
Input Offset Current $V^{\pm}$ = ±7.5 V	I_{IO}	—	0.5	20	—	0.5	30	pA
Input Current $V^{\pm}$ = ±7.5 V	I_I	—	5	30	—	5	50	pA
Large-Signal Voltage Gain	A_{OL}	50 k	320 k	—	50 k	320 k	—	V/V
V_O = 10 V_{p-p}, R_L = 2 kΩ		94	110	—	94	110	—	dB
Common-Mode Rejection Ratio	C_{MRR}	80	90	—	70	90	—	dB
Common-Mode Input-Voltage Range	V_{ICR}	10	-0.5 to 12	0	10	-0.5 to 12	0	V
Power-Supply Rejection Ratio $\Delta V_{IO}/\Delta V^{\pm}$ $V^{\pm}$ = ±7.5 V	P_{SRR}	—	32	150	—	32	320	μV/V
Maximum Output Voltage								V
At R_L = 2 k	V_{OM}^+	12	13.3	—	12	13.3	—	
	V_{OM}^-	—	0.002	0.01	—	0.002	0.01	
At R_L = ∞	V_{OM}^+	14.99	15	—	14.99	15	—	
	V_{OM}^-	—	0	0.01	—	0	0.01	
Maximum Output Current								mA
I_{OM}^+ (Source) @ V_O = 0 V		12	22	45	12	22	45	
I_{OM}^- (Sink) @ V_O = 15 V		12	20	45	12	20	45	
Supply Current	I^+							mA
V_O = 7.5 V, R_L = ∞		—	10	15	—	10	15	
V_O = 0 V, R_L = ∞		—	2	3	—	2	3	
Input Offset Voltage Temp. Drift $\Delta V_{IO}/\Delta T$*		—	10	—	—	10	—	μV/°C

TYPICAL VALUES INTENDED ONLY FOR DESIGN GUIDANCE

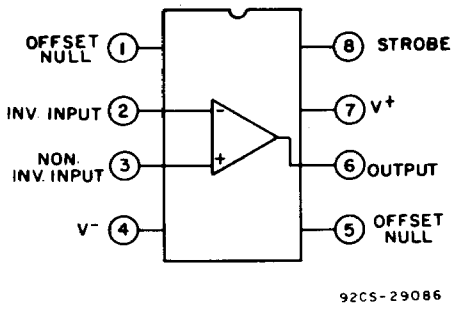
CHARACTERISTIC		TEST CONDITIONS $V^+ = +7.5$ V, $V^- = -7.5$ V, $T_A = 25°C$ (Unless otherwise specified)	TYPICAL VALUES CA5130A (T, S, E)	TYPICAL VALUES CA5130 (T, S, E)	UNITS
Input Offset Voltage Adjustment Range		10 kΩ across Terms. 4 and 5 or 4 and 1	±22	±22	mV
Input Resistance	R_I		1.5	1.5	TΩ
Input Capacitance	C_I	f = 1 MHz	4.3	4.3	pF
Equivalent Input Noise Voltage	e_n	BW = 0.2 MHz, R_S = 1 MΩ*	23	23	μV
Unity Gain Crossover Frequency	f_T	C_C = 0	15	15	MHz
		C_C = 47 pF	4	4	
Slew Rate, SR: Open Loop		C_C = 0	30	30	V/μs
Closed Loop		C_C = 56 pF	10	10	
Transient Response: Rise Time	t_r	C_C = 56 pF, C_L = 25 pF, R_L = 2 kΩ	0.09	0.09	μs
Overshoot			10	10	%
Settling Time (4 Vp-p Input to < 0.1%)		(Voltage Follower)	1.2	1.2	μs

* Although a 1-MΩ source is used for this test, the equivalent input noise remains constant for values of R_S up to 10 MΩ.



TOP VIEW

S and T Suffixes



TOP VIEW

E and M Suffixes

Fig. 1 - Functional diagrams for the CA5130 series.

CIRCUIT DESCRIPTION

Fig. 3 is a block diagram of the CA5130 Series CMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail, and the output can be swung very close to either supply rail in many applications. Consequently, the CA5130 Series circuits are ideal for single-supply operation. Three Class A amplifier stages, having the individual gain capability and current consumption shown in Fig. 3, provide the total gain of the CA5130. A biasing circuit provides two potentials for common use in the first and second stages. Term. 8 can be used both for phase compensation and to strobe the output stage into quiescence. When Term. 8 is tied to the negative supply rail (Term. 4) by mechanical or electrical means, the output potential at Term. 6 essentially rises to the positive supply-rail potential at Term. 7. This condition of essentially zero current drain in the output stage under the strobed "OFF" condition can only be achieved when the ohmic load resistance presented to the amplifier is very high (e.g., when the amplifier output is used to drive CMOS digital circuits in comparator applications).

Input Stages

The circuit of the CA5130 is shown in Fig. 2. It consists of a differential-input stage using PMOS field-effect transistors (Q6, Q7) working into a mirror-pair of bipolar transistors (Q9, Q10) functioning as load resistors together with resistors R3 through R6. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base drive to the second-stage bipolar transistor (Q11). Offset nulling, when desired, can be effected by connecting a 100,000-ohm potentiometer across Terms. 1 and 5 and the potentiometer slider arm to Term. 4. Cascode-connected PMOS transistors Q2, Q4 are the constant-current source for the input stage. The biasing circuit for the constant-current source is subsequently described. The small diodes D5 through D8 provide gate-oxide protection against high-voltage transients, e.g., including static electricity during handling for Q6 and Q7.

Second-Stage

Most of the voltage gain in the CA5130 is provided by the second amplifier stage, consisting of bipolar transistor Q11 and its cascode-connected load resistance provided by PMOS transistors Q3 and Q5. The source of bias potentials for these PMOS transistors is subsequently described. Miller-Effect compensation (roll-off) is accomplished by simply connecting a small capacitor between Terms. 1 and 8. A 47-picofarad capacitor provides sufficient compensation for stable unity-gain operation in most applications.

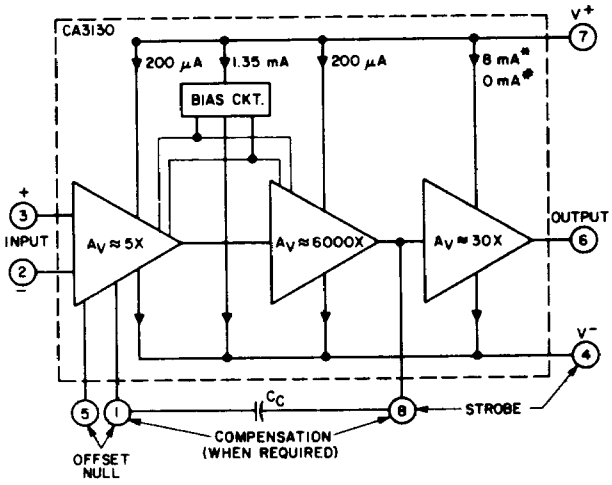


Fig. 3 - Block diagram of the CA5130 series.

Bias-Source Circuit

At total supply voltages, somewhat above 8.3 volts, resistor R2 and zener diode Z1 serve to establish a voltage of 8.3 volts across the series-connected circuit, consisting of resistor R1, diodes D1 through D4, and PMOS transistor Q1. A tap at the junction of resistor R1 and diode D4 provides a gate-bias potential of about 4.5 volts for PMOS transistors Q4 and Q5 with respect to Term. 7. A potential of about 2.2 volts is developed across diode-connected PMOS transistor Q1 with respect to Term. 7 to provide gate bias for PMOS transistors Q2 and Q3. It should be noted that Q1 is "mirror-connected"† to both Q2 and Q3. Since transistors Q1, Q2, Q3 are designed to be identical, the approximately 200-microampere current in Q1 establishes a similar current in Q2 and Q3 as constant-current sources for both the first and second amplifier stages, respectively.

At total supply voltages somewhat less than 8.3 volts, zener diode Z1 becomes non-conductive and the potential, developed across series-connected R1, D1-D4, and Q1, varies directly with variations in supply voltage, Consequently, the gate bias for Q4, Q5 and Q2, Q3 varies in accordance with supply-voltage variations. This variation results in deterioration of the power-supply-rejection ratio (PSRR) at total supply voltages below about 8.3 volts. Operation at total supply voltages below about 4.5 volts results in seriously degraded performance.

Output Stage

The output stage consists of a drain-loaded inverting amplifier using CMOS transistors operating in the Class A mode. When operating into very high resistance load, the output can be swung within millivolts of either supply rail. Because the output stage is a drain-loaded amplifier, its gain is dependent upon the load impedance. The transfer characteristics of the output stage for a load returned to the negative supply rail are shown in Fig. 6. Typical op-amp loads are readily driven by the output stage. Because large-signal excursions are non-linear, requiring feed-back for good waveform reproduction, transient delays may be encountered. As a voltage follower, the amplifier can achieve 0.01 percent accuracy levels, including the negative supply rail.

†For general information on the characteristics of CMOS transistor-pairs in linear-circuit applications, see File No. 619, data bulletin on CA3600E "CMOS Transistor Array".

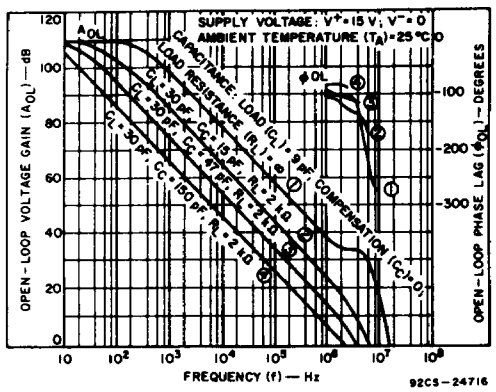


Fig. 4 - Open-loop voltage gain and phase shift vs. frequency for various values of C_L, C_C, and R_L.

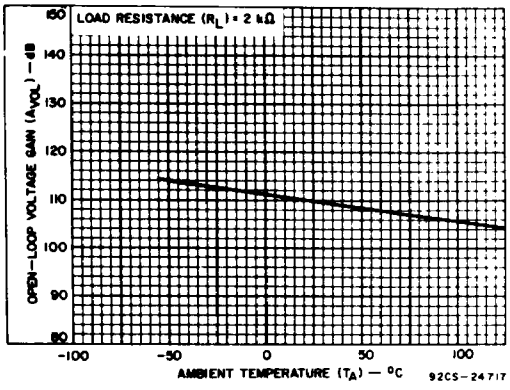


Fig. 5 - Open-loop gain vs. temperature.

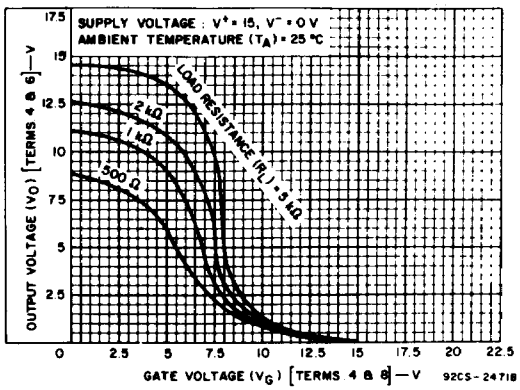


Fig. 6 - Voltage transfer characteristics of CMOS output stage.

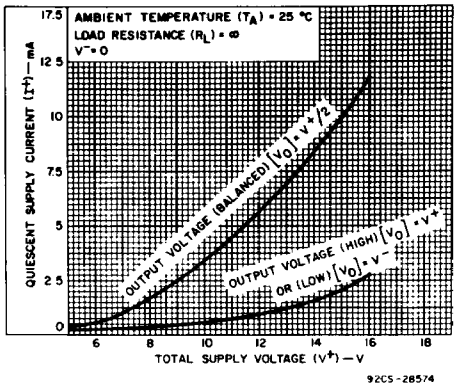


Fig. 7 - Quiescent supply current vs. supply voltage.

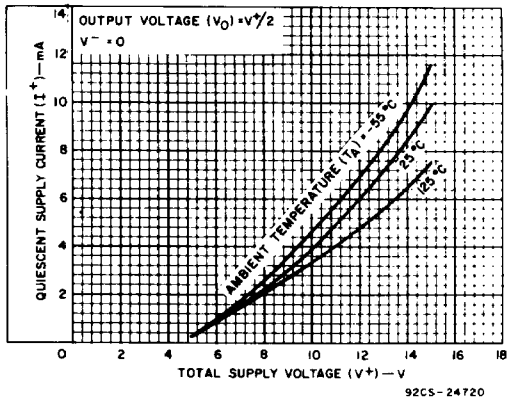


Fig. 8 - Quiescent supply current vs. supply voltage at several temperatures.

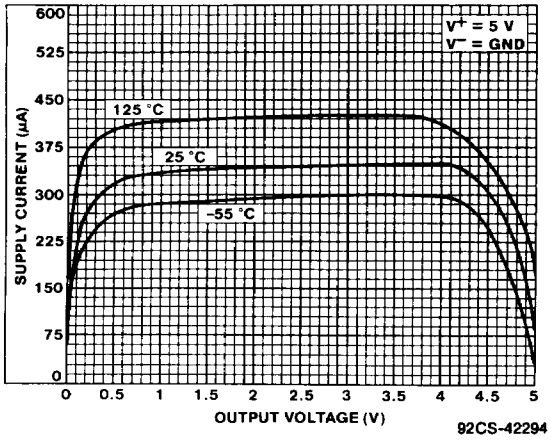


Fig. 9 - Supply current vs. output voltage.

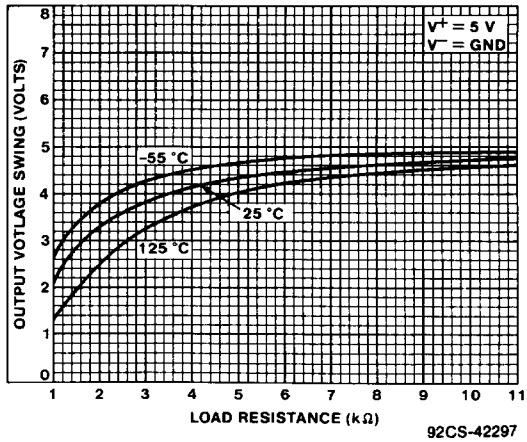


Fig. 10 - Output voltage swing vs. load resistance.

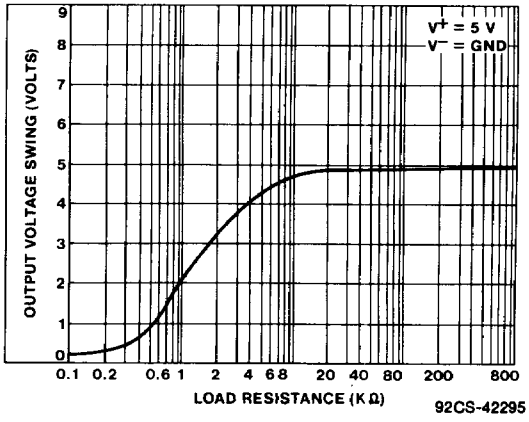


Fig. 11 - Output swing vs. load resistance.

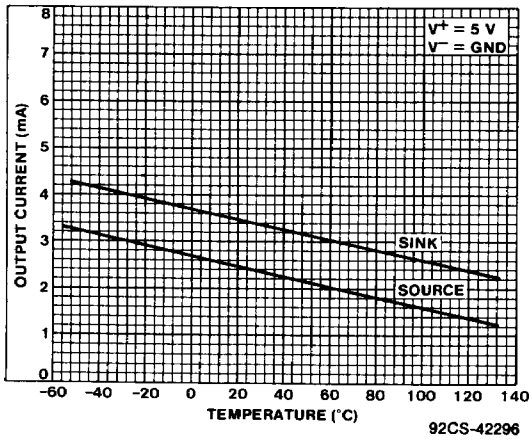


Fig. 12 - Output current vs. temperature.

Input Current Variation with Common-Mode Input Voltage

As shown in the Table of Electrical Characteristics, the input current for the CA5130 Series Op-Amps is typically 5 pA at T_A = 25°C when terminals 2 and 3 are at a common-mode potential of +7.5 volts with respect to negative supply Terminal 4. Fig. 15 contains data showing the variation of input current as a function of common-mode input voltage at T_A = 25°C. These data show that circuit designers can advantageously exploit these characteristics to design circuits which typically require an input current of less than 1 pA, provided the common-mode input voltage does not exceed 2 volts. As previously noted, the input current is essentially the result of the leakage current through the gate-protection diodes in the input circuit and, therefore, a function of the applied voltage. Although the finite resistance of the glass terminal-to-case insulator of the TO-5 package also contributes an increment of leakage current, there are useful compensating factors. Because the gate-protection network functions as if it is connected to Terminal 4 potential, and the TO-5 case of the CA5130 is also internally tied to Terminal 4, input terminal 3 is essentially "guarded" from spurious leakage currents.

Offset Nulling

Offset-voltage nulling is usually accomplished with a 100,000-ohm potentiometer connected across Terms. 1 and 5 and with the potentiometer slider arm connected to Term. 4. A fine offset-null adjustment usually can be effected with the slider arm positioned in the mid-point of the potentiometer's total range.

Input-Current Variation with Temperature

The input current of the CA5130 Series circuits is typically 5 pA at 25° C. The major portion of this input current is due to leakage current through the gate-protective diodes in the input circuit. As with any semiconductor-junction device, including op amps with a junction-FET input stage, the leakage current approximately doubles for every 10°C increase in temperature. Fig. 16 provides data on the typical variation of input bias current as a function of temperature in the CA5130.

In applications requiring the lowest practical input current and incremental increases in current because of "warm-up" effects, it is suggested that an appropriate heat sink be used with the CA5130. In addition, when "sinking" or "sourcing" significant output current the chip temperature increases, causing an increase in the input current. In such cases, heat-sinking can also very markedly reduce and stabilize input current variations.

Input-Offset-Voltage (V_{IO}) Variation with DC Bias vs. Device Operating Life

It is well known that the characteristics of a MOS/FET device can change slightly when a dc gate-source bias potential is applied to the device for extended time periods. The magnitude of the change is increased at high temperatures. Users of the CA5130 should be alert to the possible impacts of this effect if the application of the device involves extended operation at high temperatures with a significant differential dc bias voltage applied across

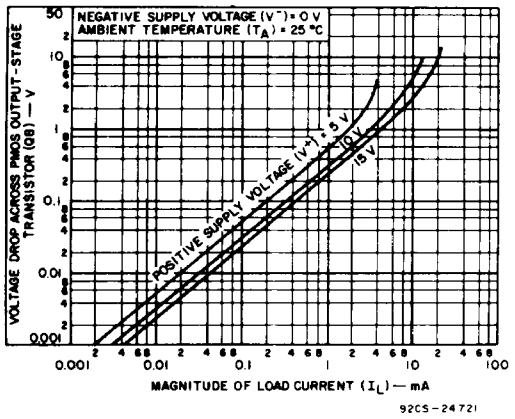


Fig. 13 - Voltage across PMOS output transistor (Q8) vs. load current.

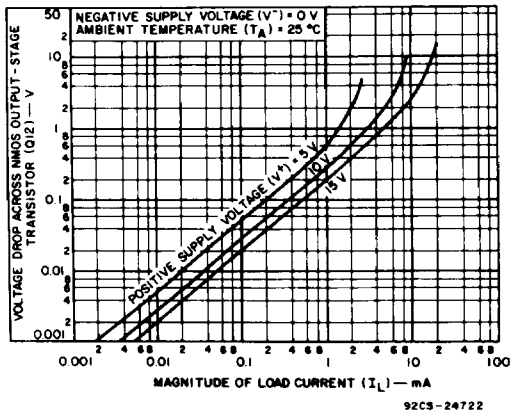


Fig. 14 - Voltage across NMOS output transistor (Q12) vs. load current.

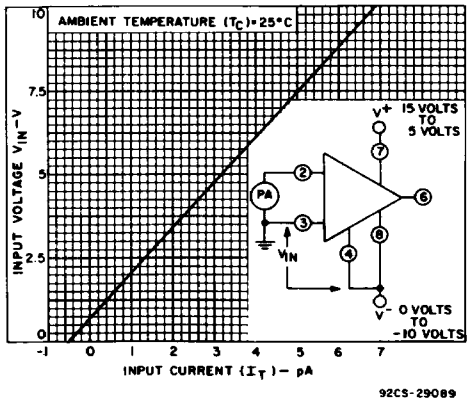


Fig. 15 - CA5130 input current vs. common-mode voltage.

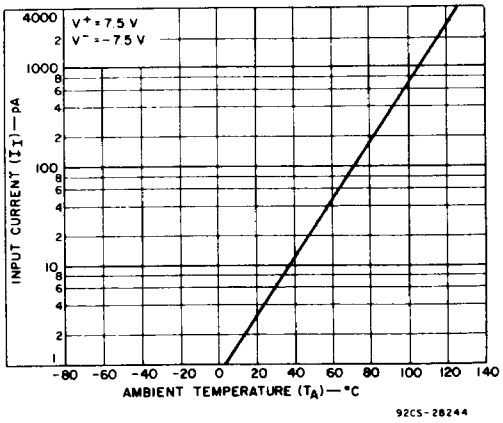


Fig. 16 - Input current vs. ambient temperature.

Terms. 2 and 3. Fig. 17 shows typical data pertinent to shifts in offset voltage encountered with CA5130 devices (TO-5 package) during life testing. At lower temperatures (TO-5 and plastic), for example at 85°C, this change in voltage is considerably less. In typical linear applications where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar transistor input stage. The two-volt dc differential voltage example represents conditions when the amplifier output stage is "toggled", e.g., as in comparator applications.

Power-Supply Considerations

Because the CA5130 is very useful in single-supply applications, it is pertinent to review some considerations relating to power-supply current consumption under both single- and dual-supply service. Figs. 18a and 18b show the CA5130 connected for both dual- and single-supply operation.

Dual-supply operation: When the output voltage at Term. 6 is zero-volts, the currents supplied by the two power supplies are equal. When the gate terminals of Q8 and Q12 are driven increasingly positive with respect to ground, current flow through Q12 (from the negative supply) to the load is increased and current flow through Q8 (from the positive supply) decreases correspondingly. When the gate terminals of Q8 and Q12 are driven increasingly negative with respect to ground, current flow through Q8 is increased and current flow through Q12 is decreased accordingly.

Single-supply operation: Initially, let it be assumed that the value of R_L is very high (or disconnected), and that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is at V+/2, i.e., the voltage-drops across Q8 and Q12 are of equal magnitude. Fig. 7 shows typical quiescent supply-current vs. supply-voltage for the CA5130 operated under these conditions. Since the output stage is operating as a Class A amplifier, the supply-current will remain constant under dynamic operating conditions as long as the transistors are operated in the linear portion of their voltage-transfer characteristics (see Fig. 6). If either Q8 or Q12 are swung out of their linear regions toward cut-off (a non-linear region), there will be a corresponding reduction in supply-current. In the extreme case, e.g., with Term. 8 swung down to ground potential (or tied to ground), NMOS transistor Q12 is completely cut off and the supply-current to series-connected transistors Q8, Q12 goes essentially to zero. The two preceeding stages in the CA5130, however, continue to draw modest supply-current (see the lower curve in Fig. 7) even though the output stage is strobed off. Fig. 14a shows a dual-supply arrangement for the output stage that can also be strobed off, assuming $R_L = \infty$, by pulling the potential of Term. 8 down to that of Term. 4.

Let it now be assumed that a load-resistance of nominal value (e.g., 2 kilohms) is connected between Term. 6 and ground in the circuit of Fig. 18b. Let it further be assumed again that the input-terminal bias (Terms. 2 and 3) is such that the output terminal (No. 6) voltage is a $V^+/2$. Since PMOS transistor Q8 must now supply quiescent current to

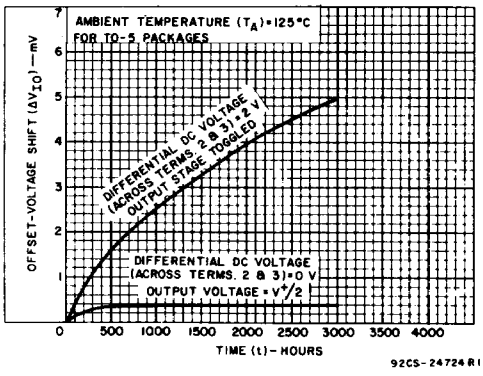


Fig. 17 - Typical incremental offset-voltage shift vs. operating life.

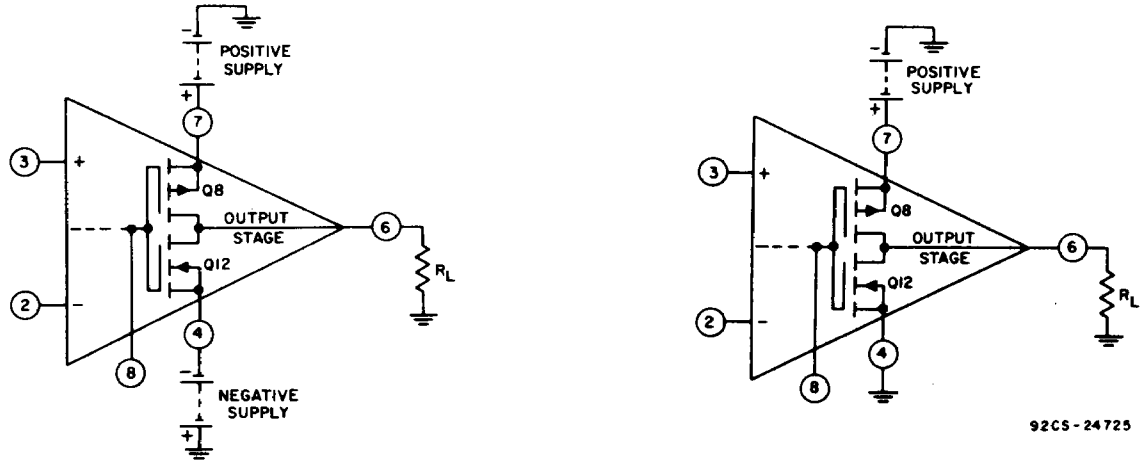


Fig. 18 - CA5130 output stage in dual and single power-supply operation.

both R_L and transistor Q12, it should be apparent that under these conditions the supply-current must increase as an inverse function of the R_L magnitude. Fig. 9 shows the voltage-drop across PMOS transistor Q8 as a function of load current at several supply-voltages. Fig. 6 shows the voltage-transfer characteristics of the output stage for several values of load resistance.

Wideband Noise

From the standpoint of low-noise performance considerations, the use of the CA5130 is most advantageous in applications where in the source resistance of the input signal is in the order of 1 megohm or more. In this case, the total input-referred noise voltage is typically only 23 μV when the test-circuit amplifier of Fig. 19 is operated at a total supply voltage of 15 volts. This value of total input-referred noise remains essentially constant, even though the value of source resistance is raised by an order of magnitude. This characteristic is due to the fact that reactance of the input capacitance becomes a significant factor in shunting the source resistance. It should be noted, however, that for values of source resistance very much greater than 1 megohm, the total noise voltage generated can be dominated by the thermal noise contributions of both the feedback and source resistors.

TYPICAL APPLICATIONS

Voltage Followers

Operational amplifiers with very high input resistances, like the CA5130, are particularly suited to service as voltage followers. Fig. 20 shows the circuit of a classical voltage follower, together with pertinent waveforms using the CA5130 in a split-supply configuration.

A voltage follower, operated from a single supply, is shown in Fig. 21, together with related waveforms. This follower circuit is linear over a wide dynamic range, as illustrated by the reproduction of the output waveform in Fig. 21a with input-signal ramping. The waveforms in Fig. 21b show that the follower does not lose its input-to-output phase-sense, even though the input is being swung 7.5 volts below ground potential. This unique characteristic is an important attribute in both operational amplifier and comparator applications. Fig. 21b also shows the manner in which the CMOS output stage permits the output signal to swing down to the negative supply-rail potential (i.e., ground in the case shown). The digital-to-analog converter (DAC) circuit, described in the following section, illustrates the practical use of the CA5130 in a single-supply voltage-follower application.

9-Bit CMOS DAC

A typical circuit of a 9-bit Digital-to-Analog Converter (DAC)* is shown in Fig. 22. This system combines the concepts of multiple-switch CMOS IC's a low-cost ladder network of discrete metal-oxide-film resistors, a CA5130 op amp connected as a follower, and an inexpensive monolithic regulator in a simple single power-supply arrangement. An additional feature of the DAC is that it is readily interfaced with CMOS input logic, e.g., 10-volt logic levels are used in the circuit of Fig. 22.

The circuit uses an R/2R voltage-ladder network, with the output potential obtained directly by terminating the ladder arms at either the positive or the negative power-supply terminal. Each CD4007A contains three "inverters", each "inverter" functioning as a single-pole double-throw switch to terminate an arm of the R/2R network at either the positive or negative power-supply terminal. The resistor ladder is an assembly of one percent tolerance metal-oxide film resistors. The five arms requiring the highest accuracy are assembled with series and parallel combinations of 806,000-ohm resistors from the same manufacturing lot.

A single 15-volt supply provides a positive bus for the CA5130 follower amplifier and feeds the CA3085 voltage regulator. A "scale-adjust" function is provided by the regulator output control, set to a nominal 10-volt level in this system. The line-voltage regulation (approximately 0.2%) permits a 9-bit accuracy to be maintained with variations of several volts in the supply. The flexibility afforded by the CMOS building blocks simplifies the design of DAC systems tailored to particular needs.

*"Digital-to-Analog Conversion Using the RCA-CD4007A CMOS IC", Application Note ICAN-6080.

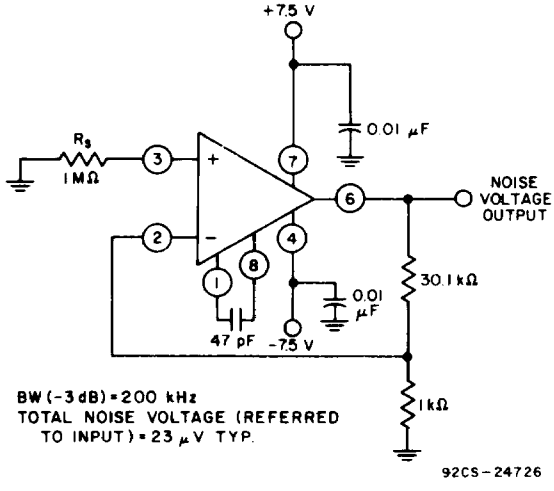
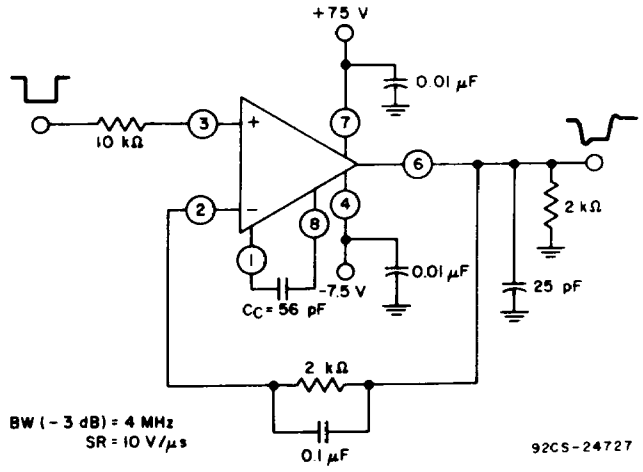
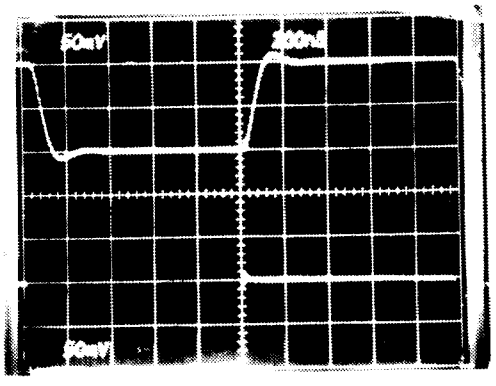


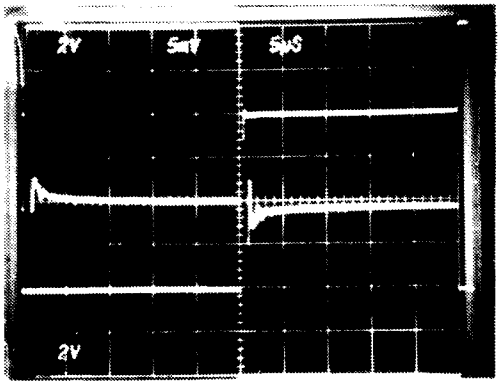
Fig. 19 - CA5130 test-circuit amplifier (30 -dB gain) used for wideband noise measurements.





Top Trace: Output
Bottom Trace: Input

(a) *Small-signal response (50 mV/div. and 200 ns/div.)*



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Top Trace: Output signal (2 V/div. and 5 μs/div.)
Center Trace: Difference signal (5 mV/div. and 5 μs/div.)
Bottom Trace: Input signal (2 V/div. and 5 μs/div.)

(b) *Input-output difference signal showing settling time (Measurement made with Tektronix 7A13 differential amplifier)*

Fig. 20 - CA5130 split-supply voltage follower with associated waveforms.

Single-Supply, Absolute-Value, Ideal Full-Wave Rectifier

The absolute-value circuit using the CA5130 is shown in Fig. 23. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No. 6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA5130 functions as a normal inverting amplifier with a gain equal to -R2/R1. When the equality of the two equations shown in Fig. 23 is satisfied, the full-wave output is symmetrical.

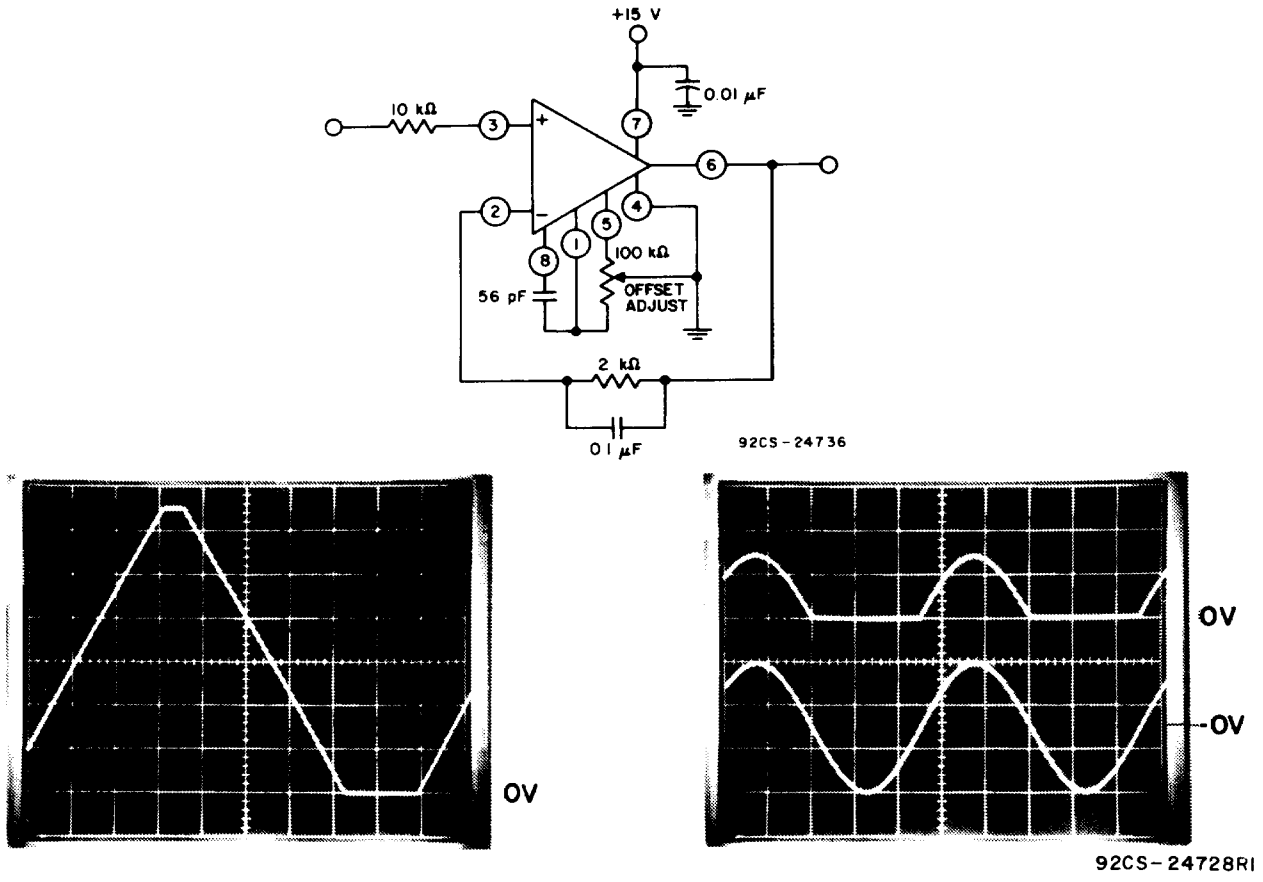
Peak Detectors

Peak-detector circuits are easily implemented with the CA5130, as illustrated in Fig. 24 for both the peak-positive and the peak-negative circuit. It should be noted that with large-signal inputs, the bandwidth of the peak-negative circuit is much less than that of the peak-positive circuit. The second stage of the CA5130 limits the bandwidth in this case. Negative-going output-signal excursion requires a positive-going signal excursion at the collector of transistor Q11, which is loaded by the intrinsic capacitance of the associated circuitry in this mode. On the other hand, during a negative-going signal excursion at the collector of Q11, the transistor functions in active "pull-down" mode so that the intrinsic capacitance can be discharge more expeditiously.

Error-Amplifier in Regulated-Power Supplies

The CA5130 is an ideal choice for error-amplifier service in regulated power supplies since it can function as an error-amplifier when the regulated output voltage is required to approach zero. Fig. 25 shows the schematic diagram of a 40-mA power supply capable of providing regulated output voltage by continuous adjustment over the range from 0 to 13 volts. Q3 and Q4 in IC2 (a CA3086 transistor-array IC) function as zerners to provide supply-voltage for the CA5130 comparator (IC1). Q1, Q2, and Q5 in IC2 are configured as a low impedance, temperature-compensated source of adjustable reference voltage for the error amplifier.

Transistors Q1, Q2, Q3, and Q4 in IC3 (another CA3086 transistor-array IC) are connected in parallel as the series-pass element. Transistor Q5 in IC3 functions as a current-limiting device by diverting base drive from the series-pass transistors, in accordance with the adjustment of resistor R2.



(a) *Output-waveform with input-signal ramping (2 V/div. and 500 μs/div.)*

Top Trace: Output (5 V/div. and 200 μs/div.)
Bottom Trace: Input (5 V/div. and 200 μs/div.)

(b) *Output-waveform with ground-reference sine-wave input*

Fig. 21 - Single-supply voltage-follower with associated waveforms. (e.g., for use in single-supply D/A converter; see Fig. 9 in ICAN-6080).

Fig. 26 contains the schematic diagram of a regulated power-supply capable of providing regulated output voltage by continuous adjustment over the range from 0.1 to 50 volts and currents up to 1 ampere. The error amplifier (IC1) and circuitry associated with IC2 function as previously described, although the output of IC1 is boosted by a discrete transistor (Q4) to provide adequate base drive for the Darlington-connected series-pass transistors Q1, Q2. Transistor Q3 functions in the previously described current-limiting circuit.

Multivibrators

The exceptionally high input resistance presented by the CA5130 is an attractive feature for multivibrator circuit design because it permits the use of timing circuits with high R/C ratios. The circuit diagram of a pulse generator (astable multivibrator), with provisions for independent control of the "on"and "off" periods, is shown in Fig. 27, Resistors R1 and R2 are used to bias the CA5130 to the mid-point of the supply-voltage and R3 is the feedback resistor. The pulse repetition rate is selected by positioning S1 to the desired position and the rate remains essentially constant when the resistors which determine "on-period" and "off-period" are adjusted.

Function Generator

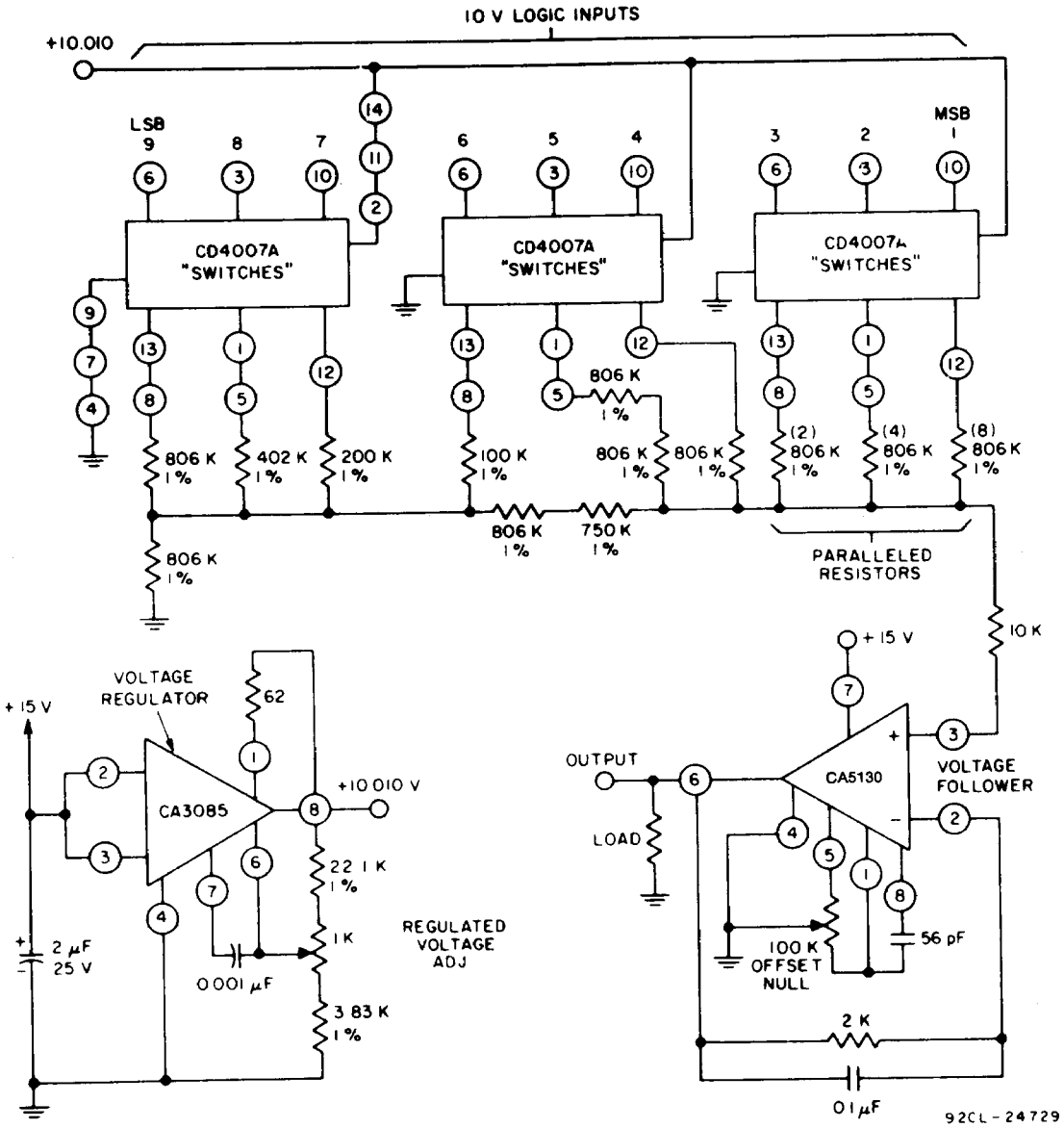
Fig. 24 contains a schematic diagram of a function generator using the CA5130 in the integrator and threshold detector functions. This circuit generates a triangular or square-wave output that can be swept over a 1,000,000:1 range (0.1 Hz to 100 kHz) by means of a single control, R1. A voltage-control input is also available for remote sweep-control.

The heart of the frequency-determining system is an operational-transconductance-amplifier (OTA)*, IC1, operated as a voltage-controlled current-source. The output, I_o, is a current applied directly to the integrating capacitor, C1, in the feedback loop of the integrator IC2, using a CA5130, to provide the triangular-wave output. Potentiometer R2 is used to adjust the circuit for slope symmetry of positive-going and negative-going signal excursions.

Another CA5130, IC3, is used as a controlled switch to set the excursion limits of the triangular output from the integrator circuit. Capacitor C2 is a "peaking adjustment" to optimize the high-frequency square-wave performance of the circuit.

Potentiometer R3 is adjustable to perfect the "amplitude symmetry" of the square-wave output signals. Output from the threshold detector is fed back via resistor R4 to the input of IC1 so as to toggle the current source from plus to minus in generating the linear triangular wave.

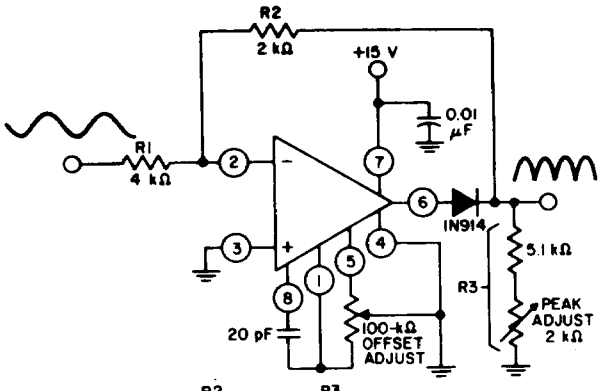
*See File No. 475 and ICAN-6668.



BIT	REQUIRED RATIO-MATCH
1	STANDARD
2	±0.1%
3	±0.2%
4	±0.4%
5	±0.8%
6-9	±1% ABS

ALL RESISTANCES IN OHMS

Fig. 22 - 9-bit DAC using CMOS digital switches and CA5130.



$$\text{GAIN} = \frac{R2}{RI} = X = \frac{R3}{RI + R2 + R3}$$

$$R3 = RI\left(\frac{X + X^2}{1 - X}\right)$$

FOR $X = 0.5$: $\frac{2\text{ k}\Omega}{4\text{ k}\Omega} = \frac{R2}{RI}$

$$R3 = 4\text{ k}\Omega\left(\frac{0.75}{0.5}\right) = 6\text{ k}\Omega$$

20 V p-p INPUT: BW(-3dB) = 230 kHz, DC OUTPUT (AVG.) = 3.2 V
1 VOLT p-p INPUT: BW(-3dB) = 130 kHz, DC OUTPUT (AVG.) = 160 mV

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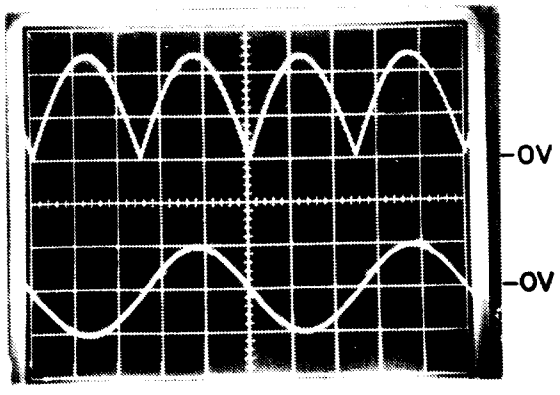

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Top Trace: Output signal (2 V/div.)
Bottom Trace: Input signal (10 V/div.)
Time base on both traces: 0.2 ms/div.

Fig. 23 - CA5130 single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.

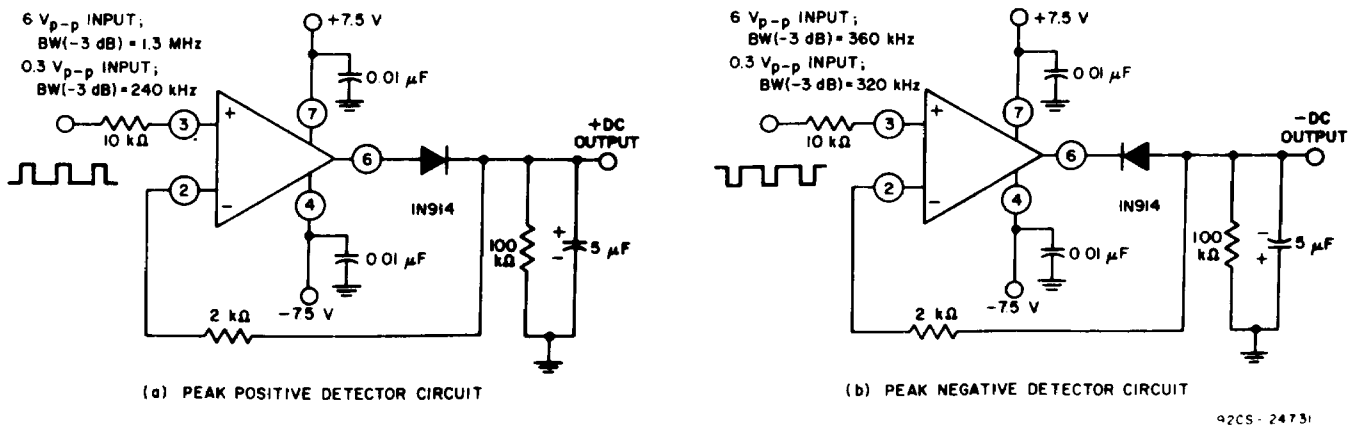


Fig. 24 - CA5130 peak-detector circuits.

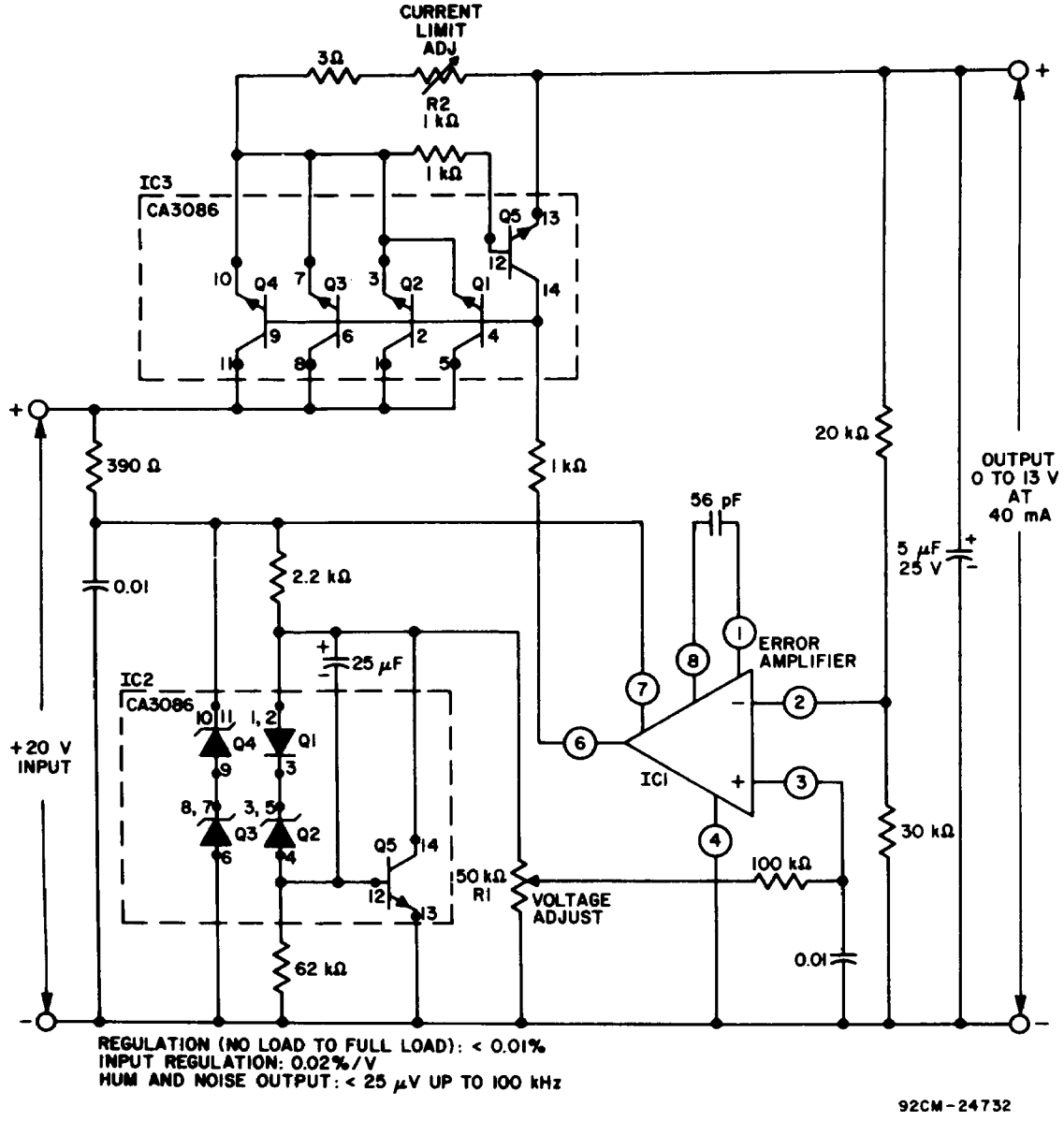
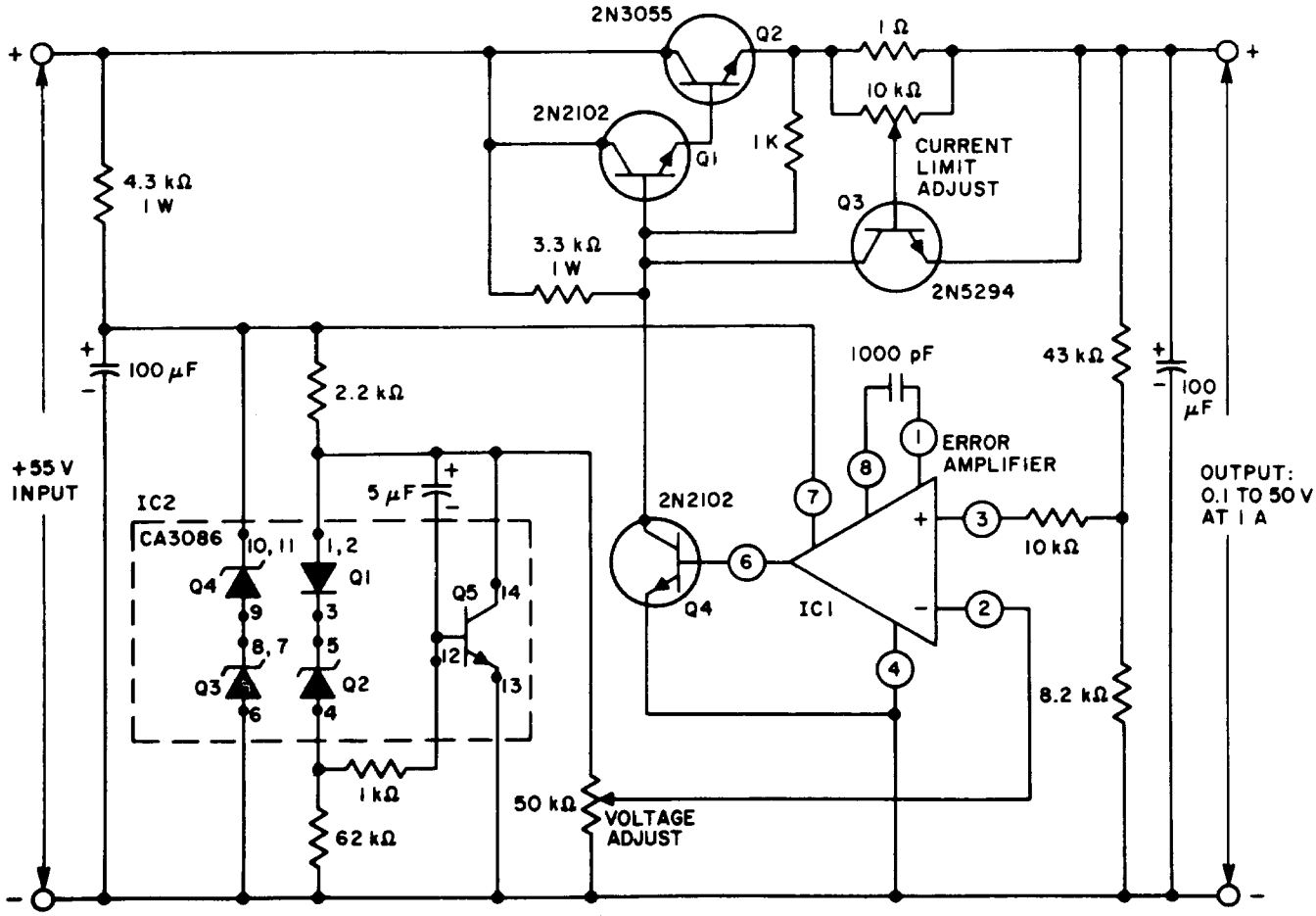


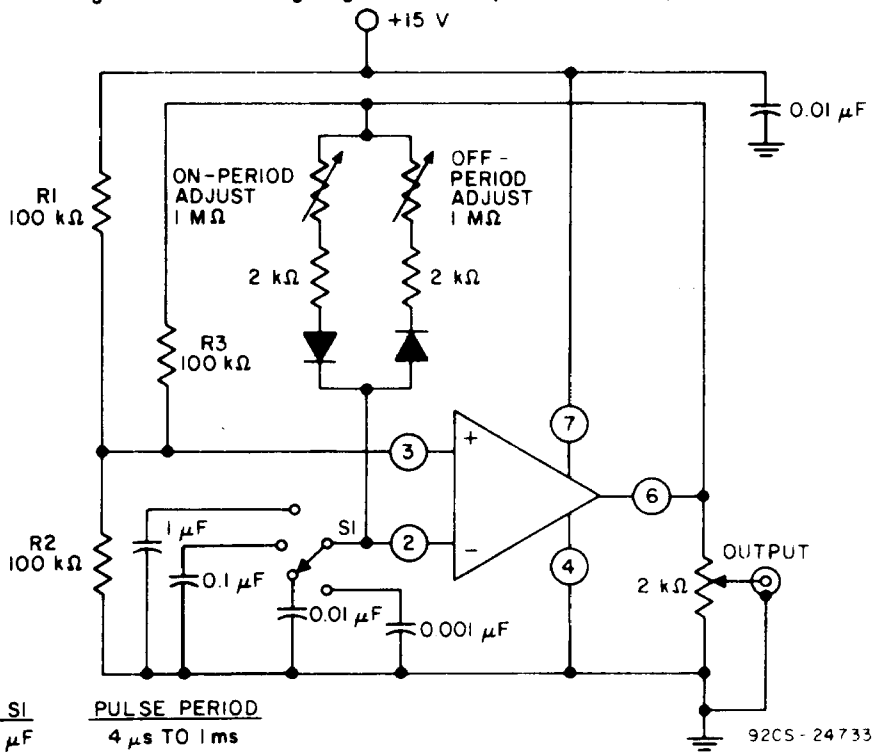
Fig. 25 - CA5130 voltage regulator circuit (0 to 13 V at 40 mA).



REGULATION (NO LOAD TO FULL LOAD): <0.005%
INPUT REGULATION: <0.01%/V
HUM AND NOISE OUTPUT: <250 μV RMS UP TO 100 kHz

92CM-24734

Fig. 26 - CA5130 voltage regulator circuit (0.1 to 50 V at 1 A).



FREQUENCY RANGE

POSITION OF SI	PULSE PERIOD
0.001 μF	4 μs TO 1 ms
0.01 μF	40 μs TO 10 ms
0.1 μF	0.4 ms TO 100 ms
1 μF	4 ms TO 1 s

Fig. 27 - CA5130 pulse generator (astable multivibrator) with provisions for independent control of "ON" and "OFF" periods.

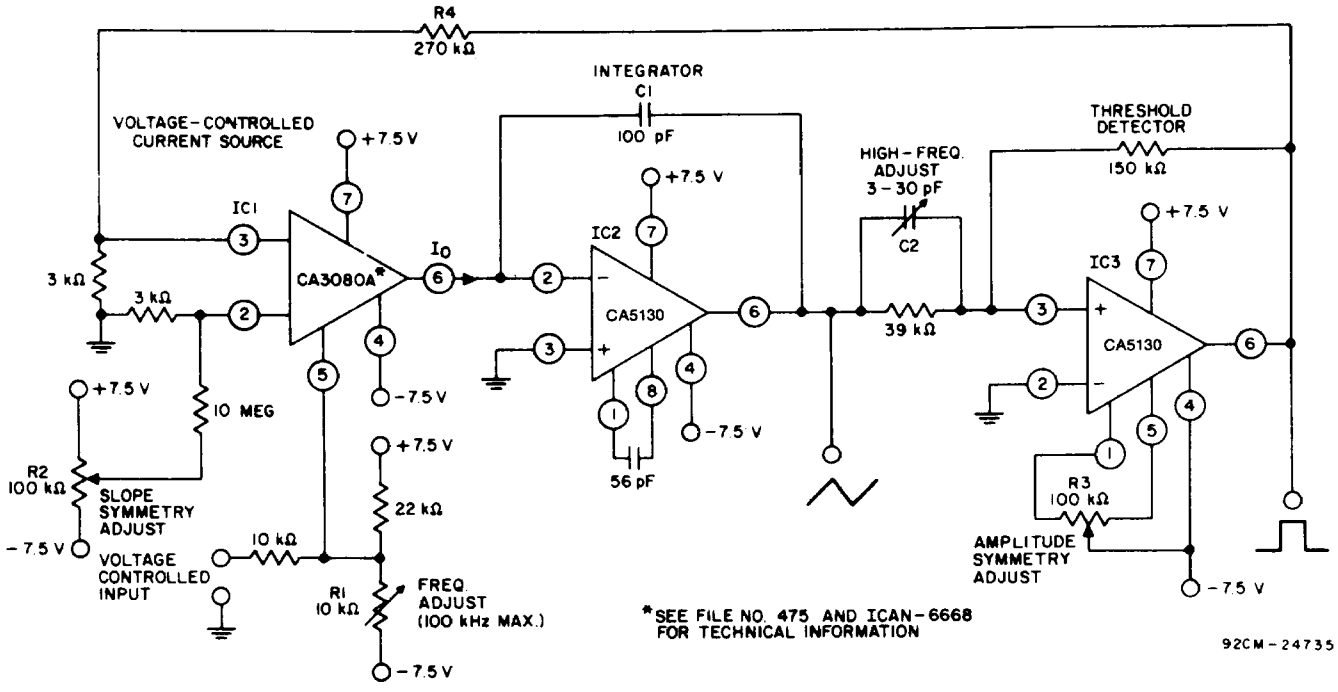


Fig. 28 - Function generator (frequency can be varied 1,000,000/1 with a single control).

Operation with Output-Stage Power-Booster

The current-sourcing and -sinking capability of the CA5130 output stage is easily supplemented to provide power-boost capability. In the circuit of Fig. 29, three CMOS transistor-pairs in a single CA3600E* IC array are shown parallel connected with the output stage in the CA5130. In the Class A mode of CA3600E shown, a typical device consumes 20 mA of supply current at 15-V operation. This arrangement boosts the current-handling capability of the CA5130 output stage by about 2.5X.

The amplifier circuit in Fig. 29 employs feedback to establish a closed-loop gain of 48 dB. The typical large-signal bandwidth (-3 dB) is 50 kHz.

*See File No. 619 for technical information.

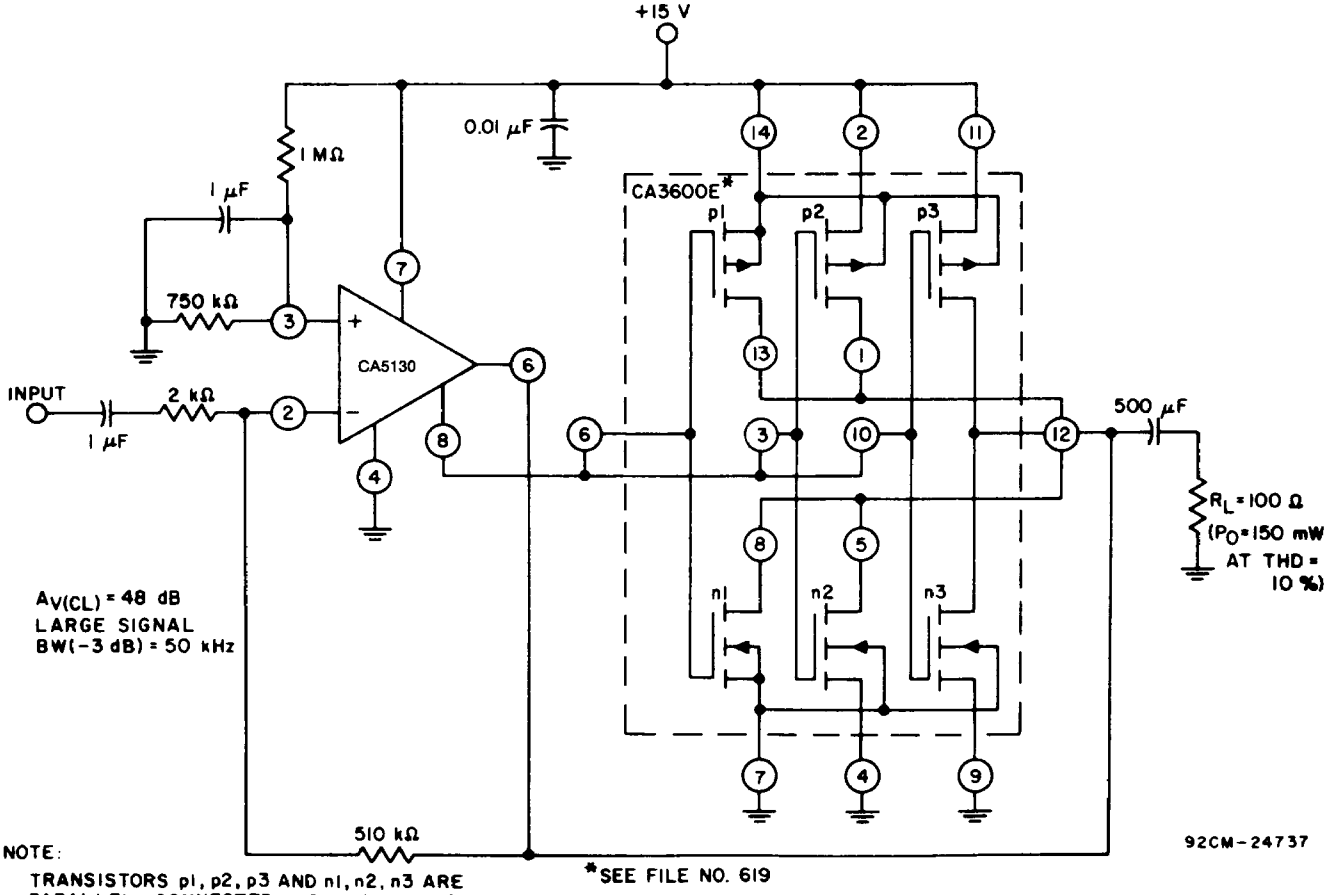
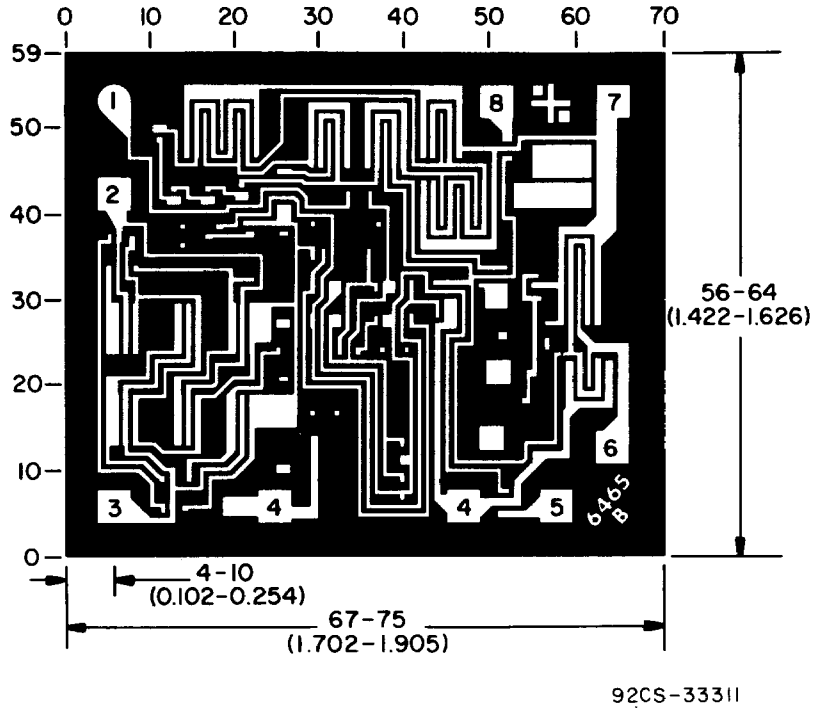


Fig. 29 - CMOS transistor array (CA3600E) connected as power-booster in the output stage of the CA5130.



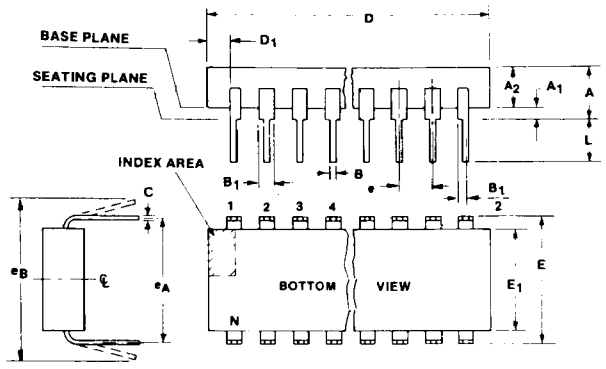
Dimensions and Pay Layout for CA5130H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

DIMENSIONAL OUTLINES

(E Suffix)
8-Lead Dual-In-Line Plastic Package (MINI-DIP)



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	—	0.210	—	5.33	9
A_1	0.015	—	0.39	—	9
A_2	0.115	0.195	2.93	4.95	
B	0.014	0.022	0.356	0.558	
B_1	0.045	0.070	1.15	1.77	3
C	0.008	0.015	0.204	0.381	
D	0.348	0.430	8.84	10.92	4
D_1	0.005	—	0.13	—	12
E	0.300	0.325	7.62	8.25	5
E_1	0.240	0.280	6.10	7.11	6, 7
e	0.100 BSC		2.54 BSC		8
e_A	0.300 BSC		7.62 BSC		9
e_B	—	0.430	—	10.92	10
L	0.115	0.160	2.93	4.06	9
N	8		8		11

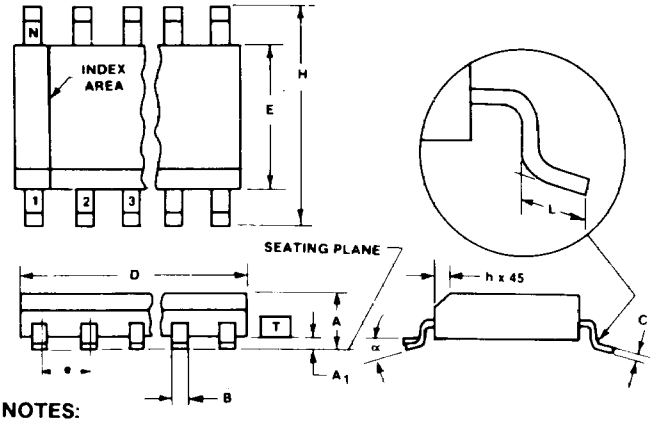
92CS-39998

Notes:

1. Refer to JEDEC Publication No. 95 JEDEC Registered and Standard Outlines for Solid State Products, for rules and general information concerning registered and standard outlines, in Section 2.2.
2. Protrusions (flash) on the base plane surface shall not exceed 0.010 in. (0.25 mm).
3. The dimension shown is for full leads. "Half" leads are optional at lead positions

   $1, N, \frac{N}{2}, \frac{N}{2}+1.$
4. Dimension D does not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 in. (0.25 mm).
5. E is the dimension to the outside of the leads and is measured with the leads perpendicular to the base plane (zero lead spread).
6. Dimension E_1 does not include mold flash or protrusions.
7. Package body and leads shall be symmetrical around center line shown in end view.
8. Lead spacing e shall be non-cumulative and shall be measured at the lead tip. This measurement shall be made before insertion into gauges, boards or sockets.
9. This is a basic installed dimension. Measurement shall be made with the device installed in the seating plane gauge (JEDEC Outline No. GS-3, seating plane gauge). Leads shall be in true position within 0.010 in. (0.25 mm) diameter for dimension e_A.
10. e_B is the dimension to the outside of the leads and is measured at the lead tips before the device is installed. Negative lead spread is not permitted.
11. N is the maximum number of lead positions.
12. Dimension D_1 at the left end of the package must equal dimension D_1 at the right end of the package within 0.030 in. (0.76 mm).
13. Pointed or rounded lead tips are preferred to ease insertion.
14. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

(M Suffix) JEDEC MS-012-AA
8-Lead Dual-In-Line Surface-Mount Plastic Package



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.0532	0.0688	1.35	1.75	
A_1	0.0040	0.0098	0.10	0.25	
B	0.0138	0.0192	0.35	0.49	
C	0.0075	0.0098	0.19	0.25	
D	0.1890	0.1968	4.80	5.00	4
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		
H	0.2284	0.2440	5.80	6.20	
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	

Notes: 1, 2, 3, 8, 9

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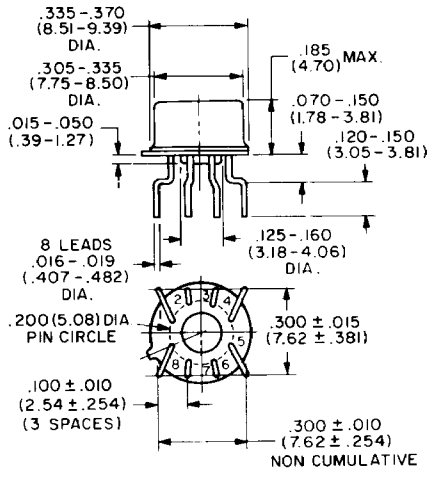
NOTES:

1. Refer to applicable symbol list.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. "T" is a reference datum.
4. "D" and "E" are reference datums and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006 in.).
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the cross hatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Controlling dimensions: MILLIMETERS.

DIMENSIONAL OUTLINES (Continued)

(S Suffix)
8-Lead TO-5 Style Dual-In-Line Formed Leads (DIL-CAN)



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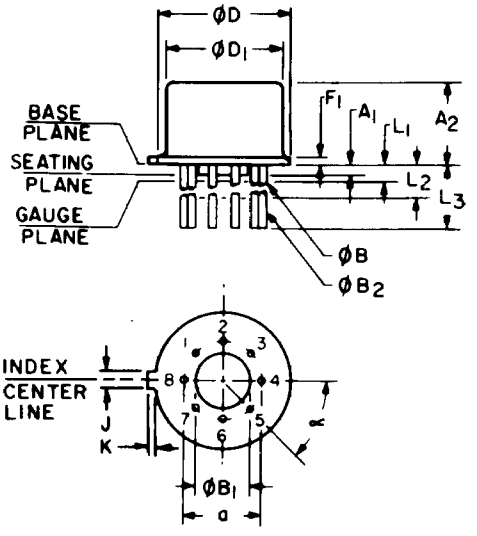
(T Suffix) JEDEC MO-002-AL
8-Lead TO-5 Style



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SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
a	0.200 TP		5.88 TP		2
A_1	0.010	0.050	0.26	1.27	
A_2	0.165	0.185	4.20	4.69	
ϕB	0.016	0.019	0.407	0.482	3
ϕB_1	0.125	0.160	3.18	4.06	
ϕB_2	0.016	0.021	0.407	0.482	3
ϕD	0.335	0.370	8.51	9.39	
ϕD_1	0.305	0.335	7.75	8.50	
F_1	0.020	0.040	0.51	1.01	
j	0.028	0.034	0.712	0.863	
k	0.029	0.045	0.74	1.14	4
L_1	0.000	0.050	0.00	1.27	3
L_2	0.250	0.500	6.4	12.7	3
L_3	0.500	0.562	12.7	14.27	3
α	45° TP		45° TP		
N	8		8		6
N_1	3		3		5

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NOTES:

Refer to Rules for Dimensioning (JEDEC Publication No. 95) for Axial Lead Product Outlines.

1. **Leads at gauge plane within 0.007 in. (0.178 mm) radius of True Position (TP) at maximum material condition.**
2. **ϕB applies between L_1 and L_2. ϕB_2 applies between L_2 and 0.500 in. (12.70 mm) from seating plane. Diameter is uncontrolled in L_1 and beyond 0.500 in. (12.70 mm).**
3. **Measure from Max. ϕD.**
4. **N_1 is the quantity of allowable missing leads.**
5. **N is the maximum quantity of lead positions.**

When incorporating RCA Solid State Devices in equipment, it is recommended that the designer refer to "Operating Considerations for RCA Solid State Devices," Form No. 1CE-402, available on request from RCA Solid State Division, Box 3200, Somerville, N.J. 08876.