4 Signals and DC Characteristics

4.1 Terminology

The I/O type abbreviations used in the pin list in Table 4.2 on page 4-3 are defined below. A numbered suffix indicates the current rating of the output (in mA).

Analog	Analog input signal
I	Input only
I/O	Input and output
O	Output only
OD	Open drain output
PD	Pulled-down internally
PU	Pulled-up internally
TP	Totem pole output
TTL	Input with TTL thresholds
TTL SCH	Schmitt trigger input with TTL thresholds
3S	Tri–state output

4.2 DC Characteristics and Pin Assignments

Table 4.1 DC Electrical Characteristics (V_{DD} = 5 V ± 10%)

Symbol	Parameter	Signal Type	Test Conditions	Tested at 0°C to 70°C	
				Min	Max
V_{IH}	Min. high-level input	CTTL	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	2.2 V	V_{DD} + 0.3V
		CMOS	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	0.7V_{DD}	V_{DD} + 0.3V
V_{IL}	Max. low-level input	CTTL	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	–0.3 V	0.8V
		CMOS	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	–0.3 V	0.3V_{DD}
V_{T+}	Positive going Schmitt trigger voltage	CTTL/ SCH	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	–	2.4 V
		CMOS/ SCH	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	–	0.7V_{DD}
V_{T-}	Negative going Schmitt trigger voltage	CTTL/ SCH	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	0.8 V	–
		CMOS/ SCH	V_{OUT} = 0.1V or V_{DD} – 0.1V; [I_{OUT}] = 20 µA	0.25V_{DD}	–
$V_{Hysteresis}$	Schmitt trigger hysteresis voltage	CTTL/ SCH	V_{T+} to V_{T-}	0.05V_{DD}	–
		CMOS/ SCH	V_{T+} to V_{T-}	0.12V_{DD}	–
I_{IN}	Maximum input leakage current	CMOS and CTTL	With no pull-up resistor (V_{IN} = V_{SS} or V_{DD})	–5.0 µA	5.0 µA
I_{OZ}	Maximum output leakage current	3S	(V_{OUT} = V_{SS} or V_{DD})	–10.0 µA	10.0 µA
		OD	(V_{OUT} = V_{DD})	–10.0 µA	10.0 µA

Table 4.2 Pin List and DC Characteristics for Universe Signals[1].

Pin Name	PBGA Pin Number	CBGA Pin Number	Type	Input Type	Output Type	I_{OL} (mA)	I_{OH} (mA)	Signal Description
ACK64#	W11	W8	I/O	TTL	3S	6	–2	PCI Acknowledge 64 Bit Transfer
AD [63:0]	TABLE 4.3		I/O	TTL	3S	6	–2	PCI Address/Data Pins
C/BE# [0]	Y14	T11	I/O	TTL	3S	6	–2	PCI Command and Byte Enables
C/BE# [1]	V14	Y11						
C/BE# [2]	T14	U11						
C/BE# [3]	W13	W10						
C/BE# [4]	AE15	Y12						
C/BE# [5]	AD14	V11						
C/BE# [6]	T12	V10						
C/BE# [7]	AD12	Y9						
CLK64	C23	D16	I	TTL	–	–	–	VME Clock 64 MHz—60-40 duty, 5 ns rise time
DEVSEL#	AC7	V6	I/O	–	3S	6	–2	PCI Device Select
ENID	AE21	Y16	I	CMOS	–	–	–	Enable IDD Tests
FRAME#	W17	T12	I/O	TTL	3S	6	–2	PCI Cycle Frame
GNT#	AE17	Y14	I	TTL	–	–	–	PCI Grant
IDSEL	AB16	Y15	I	TTL	–	–	–	PCI Initialization Device Select
LINT# [0]	K20	H15	I/O	TTL	OD	12	–12	PCI Interrupt
LINT# [1]	AA5	U3	I/O	TTL	OD	4	–4	
LINT# [2]	L9	J3						
LINT# [3]	V6	R4						
LINT# [4]	M4	J4						
LINT# [5]	L3	J6						
LINT# [6]	M8	J5						
LINT# [7]	L1	K4						
IRDY#	AC15	V12	I/O	TTL	3S	6	–2	PCI Initiator Ready
LCLK	AA3	W3	I	TTL	–	–	–	PCI Clock Signal
LOCK#	AA23	T18	I/O	TTL	3S	6	–2	PCI Lock
LRST#	R1	M1	O	–	3S	6	–2	PCI Reset Output
PAR	P8	L1	I/O	TTL	3S	6	–2	PCI parity
PAR64	AE5	W4	I/O	TTL	3S	6	–2	PCI Parity Upper DWORD
PERR#	AB4	W5	I/O	TTL	3S	6	–2	PCI Parity Error
PLL_TESTOUT	AB2	V1	FOR FACTORY TESTING					

Table 4.2 Pin List and DC Characteristics for Universe Signals[1]. (Continued)

Pin Name	PBGA Pin Number	CBGA Pin Number	Type	Input Type	Output Type	I_{OL} (mA)	I_{OH} (mA)	Signal Description
PLL_TESTSEL	AC1	T2	FOR FACTORY TESTING					
PWRRST#	T4	R1	I	TTL/ SCHM	–	–	–	Power–up Reset
REQ#	K22	F20	O	–	3S	6	–2	PCI Request
REQ64#	AD18	T13	I/O	TTL	3S	6	–2	PCI Request 64 Bit Transfer
RST#	AA19	W17	I	TTL	–	–	–	PCI Reset
SERR#	AA7	R7	O	TTL	OD	12	–12	PCI System Error
STOP#	AB18	W15	I/O	TTL	3S	6	–2	PCI Stop
TCK	H12	A10	I	TTL	–	–	–	JTAG Test Clock Input
TDI	A13	F10	I	TTL (PU)	–	–	–	JTAG Test Data Input
TDO	C13	E11	O	–	3S	–	–	JTAG Test Data OUTput
TMODE [0]	AA13	W11	I	TTL	–	–	–	Test Mode Enable
TMODE [1]	AA21	V17						
TMODE [2]	W23	R18						
TMS	C11	C9	I	TTL (PU)	–	–	–	JTAG Test Mode Select
TRDY#	AD8	W7	I/O	TTL	3S	6	–2	PCI Target Ready
TRST#	E13	B10	I	TTL (PU)	–	–	–	JTAG Test Reset
VA [31:0]	TABLE 4.4		I/O	TTL (PD)	3S	3	–3	VMEbus Address Pins
VAM [0]	E11	D8	I/O	TTL	3S	3	–3	VMEbus Address Modifier Signals
VAM [1]	D10	A6						
VAM [2]	G9	E9						
VAM [3]	B10	B8						
VAM [4]	H10	D9						
VAM [5]	A9	A7						
VAM_DIR	B8	E8	O	–	3S	6	–6	VMEbus AM Signal Direction Control
VAS#	B14	A12	I/O	TTL/ SCHM (PU)	3S	3	–3	VMEbus Address Strobe
VAS_DIR	K12	D10	O	–	3S	6	–6	VMEbus AS Direction Control
VA_DIR	G13	B11	O	–	3S	12	–12	VMEbus Address Direction Control

Table 4.2 Pin List and DC Characteristics for Universe Signals[1]. (Continued)

Pin Name	PBGA Pin Number	CBGA Pin Number	Type	Input Type	Output Type	I_{OL} (mA)	I_{OH} (mA)	Signal Description
VBCLR#	N3	K5	O	–	3S	3	–3	VMEbus BCLR* Signal
VBGI# [0]	N21	K19	I	TT	–	–	–	VMEbus Bus Grant In
VBGI# [1]	M16	K17						
VBGI# [2]	N25	K15						
VBGI# [3]	N23	L16		TT (PD)				
VBGO# [0]	M20	K16	O	–	3S	12	–12	VMEbus Bus Grant Out
VBGO# [1]	L25	J20						
VBGO# [2]	M18	K20						
VBGO# [3]	M24	K18						
VCOCTL	AE3	T5	I	–	–	–	–	Factory testing
VD [31:0]	TABLE 4.4		I/O	TTL	3S	3	–3	VMEbus Data Pins
VD_DIR	F10	F8	O	–	3S	12	–12	VMEbus Data Direction Control
VDS# [0]	F12	E10	I/O	TTL (PU)	3S	3	–3	VMEbus Data Strobes
VDS# [1]	A11	A9						
VDS_DIR	J11	F9	O	–	3S	6	–6	VMEbus Data Strobe Direction Control
VDTACK#	G15	B13	I/O	TTL/ SCHM (PU)	3S	3	–3	VMEbus DTACK* Signal
VIACK#	E7	E6	I/O	TTL	3S	3	–3	VMEbus IACK* Signal
VIACKI#	AE23	W16	I	TTL	–	–	–	VMEbus IACKIN* Signal
VIACKO#	L21	H17	O	–	3S	12	–12	VMEbus IACKOUT* Signal
VLWORD#	K14	C11	I/O	TTL (PD)	3S	3	–3	VMEbus LWORD* Signal
VME_RESET#	V22	T19	I	TTL				VMEbus Reset Input
VOE#	B12	C10	O	–	3S	24	–24	VMEbus Transceiver Output Enable
VRACFAIL#	P18	M16	I	TTL/ SCHM	–	–	–	VMEbus ACFAIL* Signal
VRBBSY#	M6	J2	I	TTL/ SCHM	–	–	–	VMEbus Received BBSY* Signal
VRBERR#	A7	B7	I	TTL/ SCHM	–	–	–	VMEbus Receive Bus Error

Table 4.2 Pin List and DC Characteristics for Universe Signals[1]. (Continued)

Pin Name	PBGA Pin Number	CBGA Pin Number	Type	Input Type	Output Type	I_{OL} (mA)	I_{OH} (mA)	Signal Description
VRBR# [0]	W5	U2	I	TTL/ SCHM	–	–	–	VMEbus Receive Bus Request
VRBR# [1]	U1	P1						
VRBR# [2]	R3	M3						
VRBR# [3]	L7	H2						
VRIRQ# [1]	H22	F19	I	TTL/ SCHM	–	–	–	VMEbus Receive Interrupts
VRIRQ# [2]	H20	F17						
VRIRQ# [3]	E25	E20						
VRIRQ# [4]	J21	G18						
VRIRQ# [5]	V16	U12						
VRIRQ# [6]	P20	M19						
VRIRQ# [7]	R17	M18						
VRSYSFAIL#	AC13	T10	I	TTL	–	–	–	VMEbus Receive SYSFAIL Signal
VRSYSRST#	C21	C16	I	TTL/ SCHM	–	–	–	VMEbus Receive SYSRESET* Signal
VSCON_DIR	M2	J1	O	–	3S	6	–6	SYSCON signals direction control
VSLAVE_DIR	C15	F12	O	–	3S	6	–6	DTACK/BERR direction control
VSYSCLK	N7	K2	I/O	TTL	3S	3	–3	VMEbus SYSCLK Signal
VWRITE#	D8	B6	I/O	TTL	3S	3	–3	VMEbus Write
VXBBSY	P2	L3	O	–	3S	3	–3	VMEbus Transmit BBSY* Signal
VXBERR	D12	B9	O	–	3S	3	–3	VMEbus Transmit Bus Error (BERR*)
VXBR [0]	G25	G19	O	–	3S	3	–3	VMEbus Transmit Bus Request
VXBR [1]	H24	H16						
VXBR [2]	P24	M20						
VXBR [3]	G23	C19						

Table 4.2 Pin List and DC Characteristics for Universe Signals[1]. (Continued)

Pin Name	PBGA Pin Number	CBGA Pin Number	Type	Input Type	Output Type	I_{OL} (mA)	I_{OH} (mA)	Signal Description
VXIRQ [1]	J19	J16	O	–	3S	3	–3	VMEbus Transmit Interrupts
VXIRQ [2]	K24	H19						
VXIRQ [3]	K18	J17						
VXIRQ [4]	J25	G20						
VXIRQ [5]	L23	J18						
VXIRQ [6]	M22	J19						
VXIRQ [7]	R25	L17						
VXSYSFAIL	M10	K3	O	–	3S	3	–3	VMEbus Transmit SYSFAIL Signal
VXSYSRST	A23	E16	O	–	3S	3	–3	VMEbus Transmit SYSRESET* Signal

Note 1: All PCI pins meet PCI's AC current specifications.

Table 4.3 PCI Bus Address/Data Pins

Signal	PBGA	CBGA	Signal	PBGA	CBGA
AD [0]	P16	L18	AD [32]	L17	J15
AD [1]	P22	M17	AD [33]	N19	L19
AD [2]	R19	N19	AD [34]	R23	M15
AD [3]	T18	U20	AD [35]	U19	N18
AD [4]	T22	N15	AD [36]	U23	R20
AD [5]	T20	T20	AD [37]	W25	P16
AD [6]	AA25	U19	AD [38]	U21	P17
AD [7]	AB24	R17	AD [39]	V20	R19
AD [8]	AB22	R16	AD [40]	Y22	U18
AD [9]	AE25	T17	AD [41]	W21	P15
AD [10]	AC21	V19	AD [42]	AD22	Y18
AD [11]	AB20	V15	AD [43]	Y20	T15
AD [12]	AC19	W18	AD [44]	AD20	T14
AD [13]	AA17	V14	AD [45]	Y18	U15
AD [14]	AA15	U13	AD [46]	AE19	W14
AD [15]	U15	R12	AD [47]	AD16	W13
AD [16]	AE11	U10	AD [48]	V12	T9

Table 4.3 PCI Bus Address/Data Pins

Signal	PBGA	CBGA	Signal	PBGA	CBGA
AD [17]	AB12	U9	AD [49]	Y12	W9
AD [18]	W9	V8	AD [50]	AC11	R9
AD [19]	AD10	U8	AD [51]	V10	Y4
AD [20]	AE7	T7	AD [52]	AB10	R8
AD [21]	Y8	W6	AD [53]	AA9	U7
AD [22]	AD4	U6	AD [54]	AB8	T6
AD [23]	Y6	R5	AD [55]	AB6	V4
AD [24]	Y2	P5	AD [56]	Y4	R3
AD [25]	V4	R2	AD [57]	W3	V2
AD [26]	U5	P3	AD [58]	AA1	T1
AD [27]	W1	P2	AD [59]	V2	N5
AD [28]	U7	M5	AD [60]	R5	N4
AD [29]	T8	M4	AD [61]	T2	N2
AD [30]	P6	L5	AD [62]	R9	M6
AD [31]	P10	L4	AD [63]	N5	L2

Table 4.4 VMEbus Address Pins[a]

Signal	PBGA	CBGA	Signal	PBGA	CBGA
VA [1]	H14	E12	VA [17]	D18	B16
VA [2]	A15	D11	VA [18]	C19	C15
VA [3]	F14	B12	VA [19]	B20	D17
VA [4]	J15	C12	VA [20]	B22	D15
VA [5]	D14	D12	VA [21]	D20	C17
VA [6]	G17	C13	VA [22]	F20	E15
VA [7]	H16	A17	VA [23]	E19	F14
VA [8]	B16	D13	VA [24]	A25	C20
VA [9]	C17	A15	VA [25]	E23	B18
VA [10]	D16	F13	VA [26]	C25	E19
VA [11]	A19	E14	VA [27]	G21	F16
VA [12]	B18	B14	VA [28]	E21	D18
VA [13]	F16	A16	VA [29]	F22	F18
VA [14]	E17	D14	VA [30]	D24	D19
VA [15]	A21	B17	VA [31]	F24	G16
VA [16]	F18	B15			

a. All VA pins have an internal pull-down.

Table 4.5 VMEbus Data Pins[a]

Signal	PBGA	CBGA	Signal	PBGA	CBGA
VD [0]	J7	H3	VD [16]	F6	E2
VD [1]	K8	D1	VD [17]	G5	G6
VD [2]	K2	H4	VD [18]	B2	E5
VD [3]	J3	F1	VD [19]	C1	E3
VD [4]	K4	H6	VD [20]	E3	E4
VD [5]	G1	G5	VD [21]	C3	A3
VD [6]	H2	G2	VD [22]	A1	C2
VD [7]	K6	E1	VD [23]	A3	B5
VD [8]	J5	G4	VD [24]	C5	C4
VD [9]	E1	D2	VD [25]	D6	C6
VD [10]	H6	F2	VD [26]	B4	B4
VD [11]	H4	F5	VD [27]	B6	E7
VD [12]	G3	F3	VD [28]	C7	B3
VD [13]	F2	D4	VD [29]	F8	D6
VD [14]	D2	F4	VD [30]	A5	A5
VD [15]	F4	D3	VD [31]	E9	C7

a. VD[30:27] have internal pull-downs.

Table 4.6 Pin Assignments for Power and Ground

V_{SS} Pins		V_{DD} Pins		
PBGA		PBGA		
AB14	N15	A17	H8	W15
AC9	N17	AA11	H18	W19
AC25	P4	AC3	J1	Y24
AD6	P12	*AC5	J9	
*AE1	P14	AC17	J17	
AE13	R11	AC23	J23	
J13	R13	AD2	L5	
K10	R15	AD24	L19	
K16	T6	AE9	R7	
L11	T16	B24	R21	
L13	T24	C9	T10	
L15	U11	D4	U3	
M12	U13	D22	U9	
M14	V24	E5	U17	
N1	Y10	E15	U25	
N9	Y16	G7	V8	
N11		G11	V18	
N13		G19	W7	

*AVDD and AVSS are power pins specifically used for powering the analog circuitry in the Universe. Extra care should be taken to avoid noise and ground shifting on these pins through the use of decoupling capacitors or isolated ground and power planes.

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	AA	AB	AC	AD	AE	
1	VD[22]		VD[19]		VD[9]		VD[5]		VDD		INT#[7]		VSS		LRST#		VRBR#[1]		AD[27]		AD[58]		PLL_ TESTSEL		AVSS	1
2		VD[18]		VD[14]		VD[13]		VD[6]		VD[2]		VSCON_ DIR		VXBBSY		AD[61]		AD[59]		AD[24]		PLL_ TESTOUT		VDD		2
3	VD[23]		VD[21]		VD[20]		VD[12]		VD[3]		INT#[5]		VBCLR#		VRBR#[2]		VDD		AD[57]		LCLK		VDD		VCOCTL	3
4		VD[26]		VDD		VD[15]		VD[11]		VD[4]		INT#[4]		VSS		PWRRST#		AD[25]		AD[56]		PERR#		AD[22]		4
5	VD[30]		VD[24]		VDD		VD[17]		VD[8]		VDD		AD[63]		AD[60]		AD[26]		VRBR#[0]		INT#[1]		AVDD		PAR64	5
6		VD[27]		VD[25]		VD[16]		VD[10]		VD[7]		VRBBSY#		AD[30]		VSS		INT#[3]		AD[23]		AD[55]		VSS		6
7	VRBERR#		VD[28]		VIACK#		VDD		VD[0]		VRBR#[3]		VSYSCLK		VDD		AD[28]		VDD		SERR#		DEVSEL#		AD[20]	7
8		VAM_DIR		VWRITE#		VD[29]		VDD		VD[1]		INT#[6]		PAR		AD[29]		VDD		AD[21]		AD[54]		TRDY#		8
9	VAM[5]		VDD		VD[31]		VAM[2]		VDD		INT#[2]		VSS		AD[62]		VDD		AD[18]		AD[53]		VSS		VDD	9
10		VAM[3]		VAM[1]		VD_DIR		VAM[4]		VSS		VXSYSFAIL		AD[31]		VDD		AD[51]		VSS		AD[52]		AD[19]		10
11	VDS#[1]		TMS		VAM[0]		VDD		VDS_DIR		VSS		VSS		VSS		VSS		ACK64#		VDD		AD[50]		AD[16]	11
12		VOE#		VXBERR		VDS#[0]		TCK		VAS_DIR		VSS		VSS		CBE[6]		AD[48]		AD[49]		AD[17]		CBE[7]		12
13	TDI		TDO		TRST#		VA_DIR		VSS		VSS		VSS		VSS		VSS		CBE[3]		TMODE[0]		VRSYS-FAIL#		VSS	13
14		VAS#		VA[5]		VA[3]		VA[1]		VLWORD#		VSS		VSS		CBE[2]		CBE[1]		CBE[0]		VSS		CBE[5]		14
15	VA[2]		VSLAVE_DIR		VDD		VDTACK#		VA[4]		VSS		VSS		VSS		AD[15]		VDD		AD[14]		IRDY#		CBE[4]	15
16		VA[8]		VA[10]		VA[13]		VA[7]		VSS		VBGI#[1]		AD[0]		VSS		VRIRQ#[5]		VSS		IDSEL		AD[47]		16
17	VDD		VA[9]		VA[14]		VA[6]		VDD		AD[32]		VSS		VRIRQ#[7]		VDD		FRAME#		AD[13]		VDD		GNT#	17
18		VA[12]		VA[17]		VA[16]		VDD		VXIRQ[3]		VBGO#[2]		VRACFAIL#		AD[3]		VDD		AD[45]		STOP#		REQ64#		18
19	VA[11]		VA[18]		VA[23]		VDD		VXIRQ[1]		VDD		AD[33]		AD[2]		AD[35]		VDD		RST#		AD[12]		AD[46]	19
20		VA[19]		VA[21]		VA[22]		VRIRQ#[2]		INT#[0]		VBGO#[0]		VRIRQ#[6]		AD[5]		AD[39]		AD[43]		AD[11]		AD[44]		20
21	VA[15]		VRSYSRST#		VA[28]		VA[27]		VRIRQ#[4]		VIACKO#		VBGI#[0]		VDD		AD[38]		AD[41]		TMODE[1]		AD[10]		ENID	21
22		VA[20]		VDD		VA[29]		VRIRQ#[1]		REQ#		VXIRQ[6]		AD[1]		AD[4]		VME_RST#		AD[40]		AD[8]		AD[42]		22
23	VXSYSRST		CLK64		VA[25]		VXBR[3]		VDD		VXIRQ[5]		VBGI#[3]		AD[34]		AD[36]		TMODE[2]		LOCK#		VDD		VIACKI#	23
24		VDD		VA[30]		VA[31]		VXBR[1]		VXIRQ[2]		VBGO#[3]		VXBR[2]		VSS		VSS		VDD		AD[7]		VDD			24
25	VA[24]		VA[26]		VRIRQ#[3]		VXBR[0]		VXIRQ[4]		VBGO#[1]		VBGI#[2]		VXIRQ[7]		VDD		AD[37]		AD[6]		VSS		AD[9]	25

Figure 4. 1: Pinout for 313-pin Plastic BGA Package

(Top view)

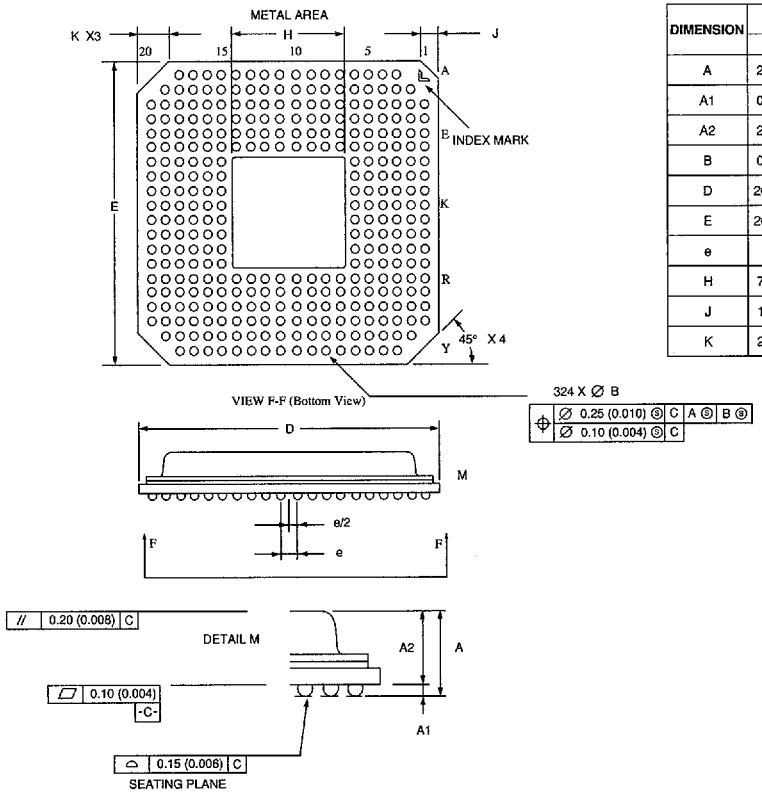
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W	Y	
1			VSS	VD[1]	VD[7]	VD[3]	VSS	VDD	VSCON_DIR	VDD	PAR	LRST#	VDD	VRBR#[1]	PWRRST#	AD[58]	VDD	PLL_TESTOUT			1
2		VSS	VD[22]	VD[9]	VD[16]	VD[10]	VD[6]	VRBR#[3]	VRBBSY#	VSYSCLK	AD[63]	VSS	AD[61]	AD[27]	AD[25]	PLL_TESTSEL	VRBR#[0]	AD[57]	VSS		2
3	VD[21]	VD[28]	VDD	VD[15]	VD[19]	VD[12]	VDD	VD[0]	INT#[2]	VXSYSFAIL	VXBBSY	VRBR#[2]	VDD	AD[26]	AD[56]	VDD	INT#[1]	VDD	LCLK	VSS	3
4	VDD	VD[26]	VD[24]	VD[13]	VD[20]	VD[14]	VD[8]	VD[2]	INT#[4]	INT#[7]	AD[31]	AD[29]	AD[60]	VDD	INT#[3]	VDD	VSS	AD[55]	PAR64	AD[51]	4
5	VD[30]	VD[23]	VDD	VDD	VD[18]	VD[11]	VD[5]	VDD	INT#[6]	VBCLR#	AD[30]	AD[28]	AD[59]	AD[24]	AD[23]	VCOCTL	AVSS	AVDD	PERR#	VSS	5
6	VAM[1]	VWRITE#	VD[25]	VD[29]	VIACK#	VDD	VD[17]	VD[4]	INT#[5]	VSS	VSS	AD[62]	VSS	VSS	VDD	AD[54]	AD[22]	DEVSEL#	AD[21]	VSS	6
7	VAM[5]	VRBERR#	VD[31]	VDD	VD[27]	VSS									SERR#	AD[20]	AD[53]	VDD	TRDY#	VSS	7
8	VDD	VAM[3]	VDD	VAM[0]	VAM_DIR	VD_DIR									AD[52]	VDD	AD[19]	AD[18]	ACK64#	VDD	8
9	VDS#[1]	VXBERR	TMS	VAM[4]	VAM[2]	VDS_DIR									AD[50]	AD[48]	AD[17]	VSS	AD[49]	CBE[7]	9
10	TCK	TRST#	VOE#	VAS_DIR	VDS#[0]	TDI									VSS	VRSYSFAIL#	AD[16]	CBE[6]	CBE[3]	VDD	10
11	VDD	VA_DIR	VLWORD#	VA[2]	TDO	VSS									VSS	CBE[0]	CBE[2]	CBE[5]	TMODE[0]	CBE[1]	11
12	VAS#	VA[3]	VA[4]	VA[5]	VA[1]	VSLAVE_DIR									AD[15]	FRAME#	VRIRQ#[3]	IRDY#	VSS	CBE[4]	12
13	VDD	VDTACK#	VA[6]	VA[8]	VDD	VA[10]									VSS	REQ64#	AD[14]	VDD	AD[47]	VDD	13
14	VSS	VA[12]	VDD	VA[14]	VA[11]	VA[23]									VSS	AD[44]	VDD	AD[13]	AD[46]	GNT#	14
15	VA[9]	VA[16]	VA[18]	VA[20]	VA[22]	VDD	VSS	INT#[0]	AD[32]	VBGI#[2]	VSS	AD[34]	AD[4]	AD[41]	VDD	AD[43]	AD[45]	AD[11]	STOP#	IDSEL	15
16	VA[13]	VA[17]	VRSYSRST#	CLK64	VXSYSRST	VA[27]	VA[31]	VXBR[1]	VXIRQ[1]	VBGO#[0]	VBGI#[3]	VRACFAIL#	VDD	AD[37]	AD[8]	VSS	VDD	VDD	VIACKI#	ENID	16
17	VA[7]	VA[15]	VA[21]	VA[19]	VDD	VRIRQ#[2]	VDD	VIACKO#	VXIRQ[3]	VBGI#[1]	VXIRQ[7]	AD[1]	VSS	AD[38]	AD[7]	AD[9]	VDD	TMODE[1]	RST#	VDD	17
18	VSS	VA[25]	VDD	VA[28]	VDD	VA[29]	VRIRQ#[4]	VDD	VXIRQ[5]	VBGO#[3]	AD[0]	VRIRQ#[7]	AD[35]	VDD	TMODE[2]	LOCK#	AD[40]	VDD	AD[12]	AD[42]	18
19		VSS	VXBR[3]	VA[30]	VA[26]	VRIRQ#[1]	VXBR[0]	VXIRQ[2]	VXIRQ[6]	VBGI#[0]	AD[33]	VRIRQ#[6]	AD[2]	VSS	AD[39]	VME_RESET#	AD[6]	AD[10]	VSS		19
20			VA[24]	VDD	VRIRQ#[3]	REQ#	VXIRQ[4]	VDD	VBGO#[1]	VBGO#[2]	VDD	VXBR[2]	VDD	VSS	AD[36]	AD[5]	AD[3]	VSS			20

Figure 4. 2: Pinout for 324–pin Ceramic BGA Package

(Top view)

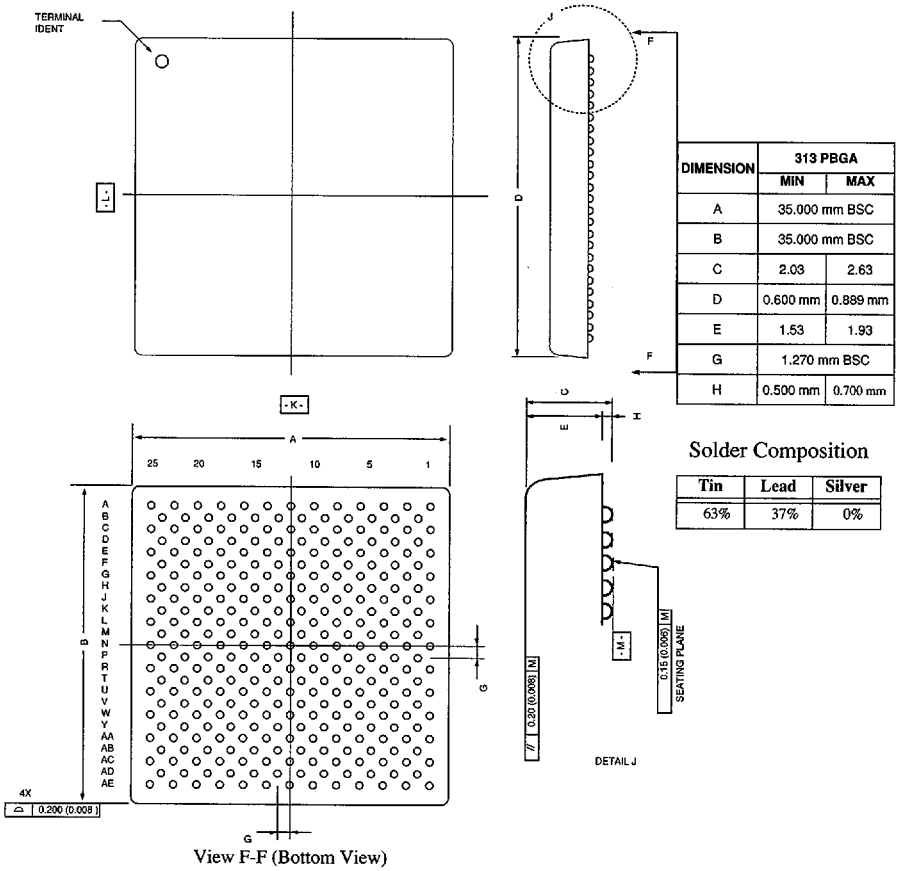
Appendix H Mechanical and Ordering Information

H.1 Mechanical Information



DIMENSION	324 CBGA	
	MIN	MAX
A	2.80 mm	3.50 mm
A1	0.74 mm	0.80 mm
A2	2.30 mm	2.70 mm
B	0.50 mm	0.70 mm
D	20.85 mm	21.15 mm
E	20.85 mm	21.15 mm
e	1.00 mm (BSC)	
H	7.35 mm	7.65 mm
J	1.20 mm	1.80 mm
K	2.20 mm	2.80 mm

Figure H.1 : Mechanical Dimensions for the 324-Pin Ceramic BGA Package



DIMENSION	313 PBGA	
	MIN	MAX
A	35.000 mm BSC	
B	35.000 mm BSC	
C	2.03	2.63
D	0.600 mm	0.889 mm
E	1.53	1.93
G	1.270 mm BSC	
H	0.500 mm	0.700 mm

Solder Composition

Tin	Lead	Silver
63%	37%	0%

Figure H.2 : Mechanical Dimensions for 313-Pin Plastic BGA Package

Note that dimensions and tolerancing for all mechanical drawings follow ANSI Y14.5M, 1982.

H.2 Ordering Information

Tundra Semiconductor Corporation products are designated by a Product Code. When ordering, refer to products by their full code. For detailed mechanical drawings or alternative packaging requirements, please contact our factory directly