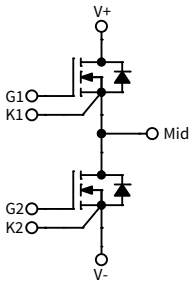
CAB003M09DM3

V_{DS}	900 V
$R_{DS(on)}$	2.5 mΩ

900 V, 2.5 mΩ, Silicon Carbide, Half-Bridge Module

Technical Features

- Ultra-Low Loss and Lightweight AlSiC Baseplate
- High Frequency Operation
- High Power Density Footprint
- High Junction Temperature (175 °C) Operation
- Implements Wolfspeed's Third Generation SiC MOSFET Technology
- Silicon Nitride Insulator



Typical Applications

- E-Mobility Inverters
- EV Chargers
- High-Efficiency Converters / Inverters
- Renewable Energy

System Benefits

- Enables Compact, Lightweight Systems
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Drain-Source Voltage	V_{DS}			900	V	T_C = 25 °C	
Maximum Gate-Source Voltage	$V_{GS\ (max)}$	-8		+19		Transient	Fig. 32 Note 1
Operational Gate-Source Voltage	$V_{GS(op)}$		-4/+15			Static	
DC Continuous Drain Current (T_{VJ} < 175 °C)	I_D		518		A	V_{GS} = 15V, T_C = 25 °C, T_{VJ} ≤ 175 °C	Notes 2, 3 Fig. 20
			391			V_{GS} = 15 V, T_C = 90 °C, T_{VJ} ≤ 175 °C	
Pulsed Drain Current	I_{DM}		1036			t_{Pmax} limited by $T_{VJ\ max}$ V_{GS} = 15 V, T_C = 25 °C	
Power Dissipation	P_D		1163		W	T_C = 25 °C, T_{VJ} ≤ 175 °C	Fig. 20 Note 4
Operational Virtual Junction Temperature	$T_{VJ(op)}$	-40		175	°C		

Note (1): Recommended turn-on gate voltage is 15 V with ±5% regulation tolerance

Note (2): Current limit calculated by $I_{D(max)} = \sqrt{(P_D / R_{DS(typ)}(T_{VJ(max)}, I_{D(max)}))}$. Please refer to Application Note, PRD-07635, for guidance on PCB ampacity.

Note (3): Verified by design

Note (4): $P_D = (T_{VJ} - T_C) / R_{TH(JC,typ)}$

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MOSFET Characteristics (Per Position) (T_{VJ} = 25˚C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	900			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.1	3.5	V	V_{DS} = V_{GS}, I_D = 130 mA	
			1.6		V	V_{DS} = V_{GS}, I_D = 130 mA, T_{VJ} = 175 °C	
Zero Gate Voltage Drain Current	I_{DSS}		4	400	µA	V_{GS} = 0 V, V_{DS} = 900 V	
Gate-Source Leakage Current	I_{GSS}		0.04	1.0	µA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		2.5	3.25	mΩ	V_{GS} = 15 V, I_D = 400 A	Fig. 2 Fig. 3
			4.3		mΩ	V_{GS} = 15 V, I_D = 400 A, T_{VJ} = 175 °C	
Transconductance	g_{fs}		316		S	V_{DS}= 20 V, I_D = 400 A	Fig. 4
			284		S	V_{DS}= 20 V, I_D = 400 A, T_{VJ} = 175 °C	
Turn-On Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{on}		6.5 6.2 6.5		mJ	V_{DS} = 400 V I_D = 400 A V_{GS} = -4 V / 15 V $R_{G(ON)}$ = 6.8 Ω $R_{G(OFF)}$ = 4.0 Ω L= 13.6 µH	Fig. 11 Fig. 13
Turn-Off Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{off}		7.2 6.9 7.1		mJ		
Internal Gate Resistance	$R_{G(int)}$		0.5		Ω	f = 100 kHz	
Input Capacitance	C_{iss}		20.4		nF	V_{GS} = 0 V, V_{DS} = 900 V V_{AC} = 25 mV, f = 100 kHz	Fig. 9
Output Capacitance	C_{oss}		1.49		nF		
Reverse Transfer Capacitance	C_{rss}		78		pF		
Gate to Source Charge	Q_{GS}		208		nC	V_{DS} = 600 V, V_{GS} = -4 V / 15 V I_D = 400 A Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		280		nC		
Total Gate Charge	Q_G		840		nC		
FET Thermal Resistance, Junction to Case	$R_{th\ JC}$		0.129		°C/W		Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25 ˚C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	V_{SD}		4.5		V	V_{GS} = -4 V, I_{SD} = 400 A	Fig. 7
			3.9			V_{GS} = -4 V, I_{SD} = 400 A, T_{VJ} = 175 °C	
DC Source-Drain Current	I_{BD}		282		A	V_{GS} = -4 V, T_C = 25 ˚C, T_{VJ} ≤ 175 ˚C	
			178			V_{GS} = -4 V, T_C = 90 ˚C, T_{VJ} ≤ 175 ˚C	
Reverse Recovery Time	t_{RR}		43.8		ns	V_{GS} = -4 V, I_{SD} = 400 A, V_R = 400 V di_F/dt = 8.5 A/ns, T_{VJ} = 175 °C	Fig. 31
Reverse Recovery Charge	Q_{RR}		6.2		µC		
Peak Reverse Recovery Current	I_{RRM}		233		A		
Reverse Recovery Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 150 °C	E_{RR}		0.5 1.0 1.3		mJ	V_{DS} = 400 V, I_D = 400A V_{GS} = -4 V / 15 V, $R_{G(ON)}$ = 6.8 Ω L= 13.6 µH	Fig. 14

Module Physical Characteristics

Parameter	symbol	Min.	Typ.	Max.	Unit	Test Conditions
High-Side Package Resistance, M1	R_{3-1}		0.41		mΩ	T_C = 125 °C, Note 5
Low-Side Package Resistance, M2	R_{1-2}		0.56			T_C = 125 °C, Note 5
Stray Inductance	L_{stray}		11.5		nH	Between DC- and DC+, f = 10 MHz
Case Temperature	T_C	-40		125	°C	
Weight	W		41		g	
Mounting Torque	M_S		1.1	2.3	N-m	Baseplate, M4 bolts
Case Isolation Voltage	V_{isol}	4			kV	AC, 50 Hz, 1 min
Comparative Tracking Index	CTI	600				
Clearance Distance			4.2		mm	Terminal to Terminal
			13.4			Terminal to Baseplate
Creepage Distance			8.8			Terminal to Terminal
			15.5			Terminal to Baseplate

Note (5): Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance.

Typical Performance

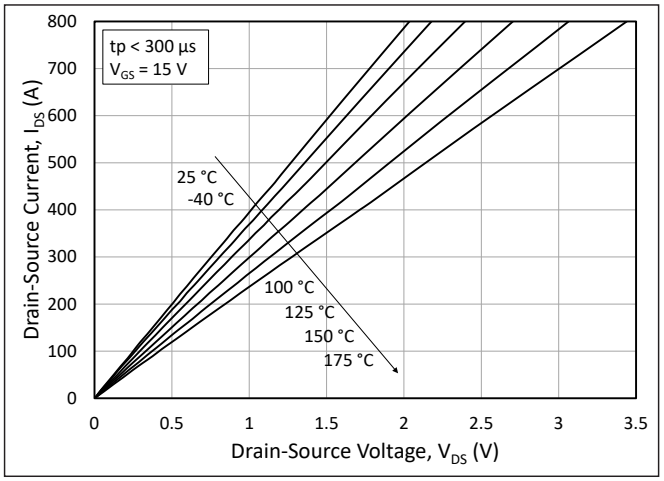


Figure 1. Output Characteristics for Various Junction Temperatures

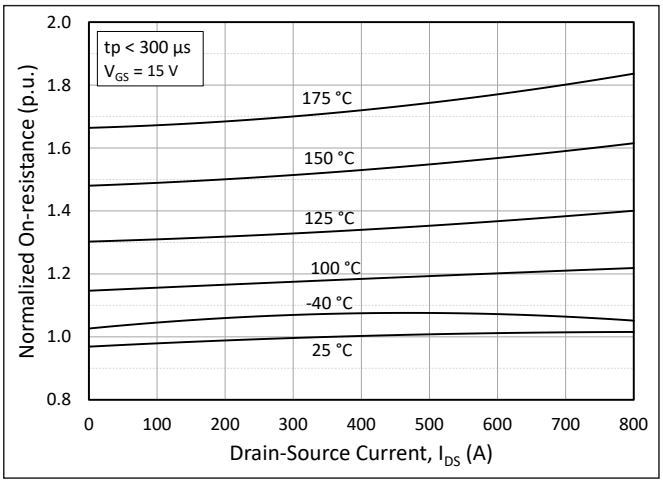


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

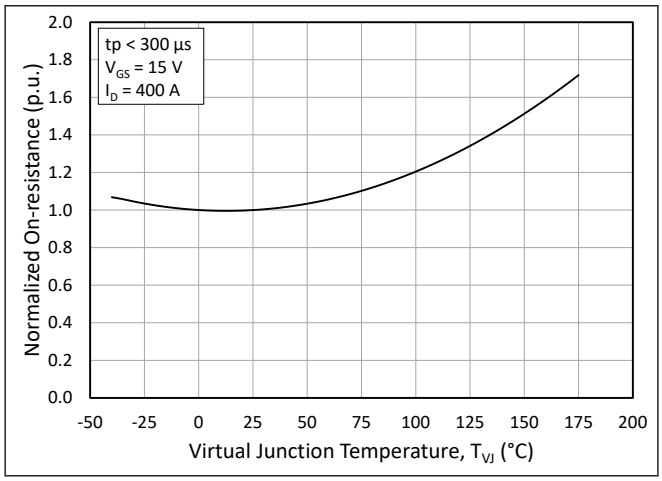


Figure 3. Normalized On-State Resistance vs. Junction Temperature

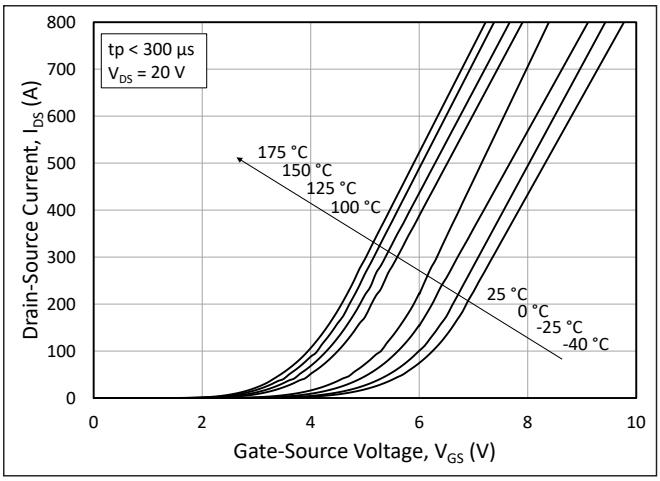


Figure 4. Transfer Characteristic for Various Junction Temperatures

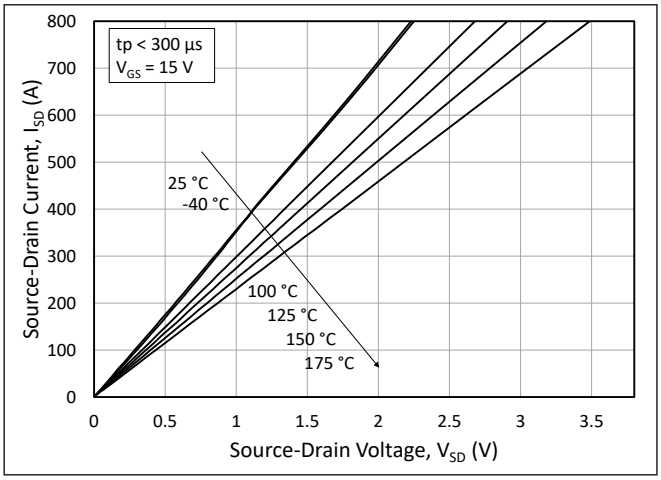


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

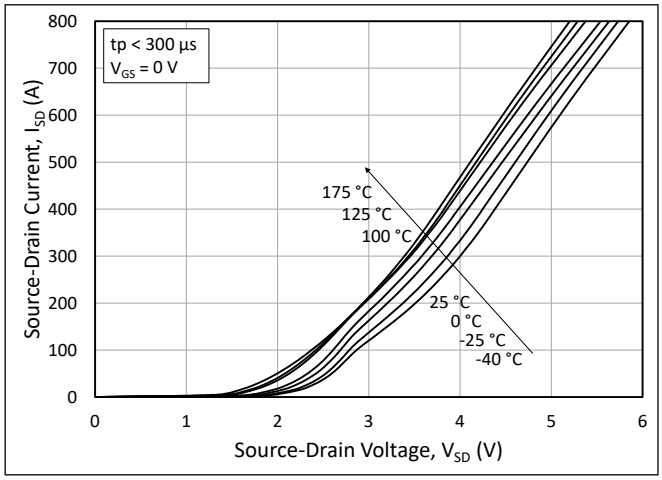


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0V (Diode)

Typical Performance

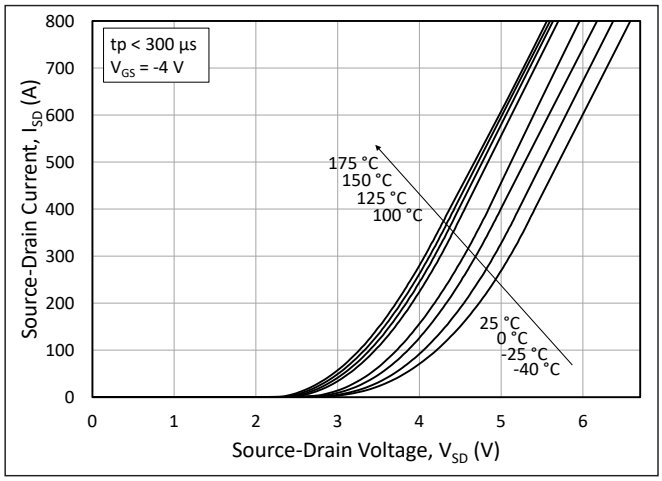


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = - 4 V (Diode)

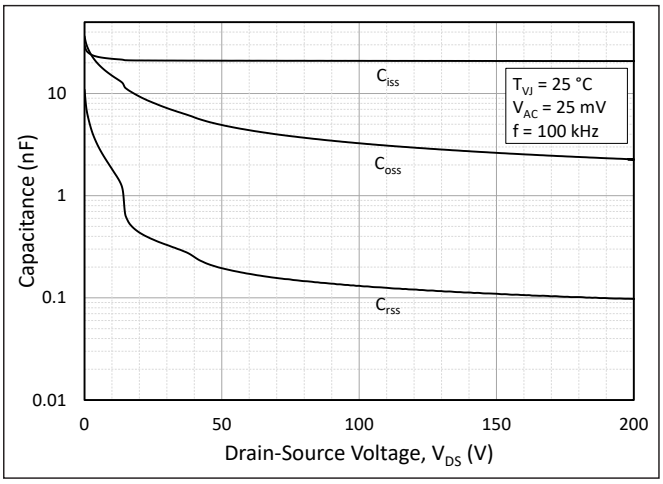


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

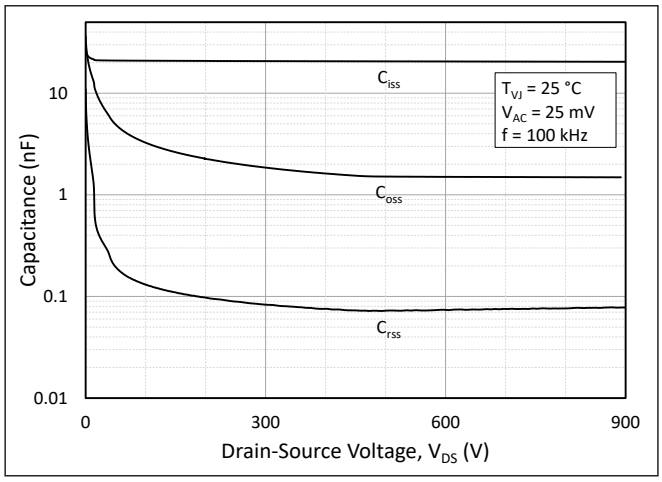


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 900V)

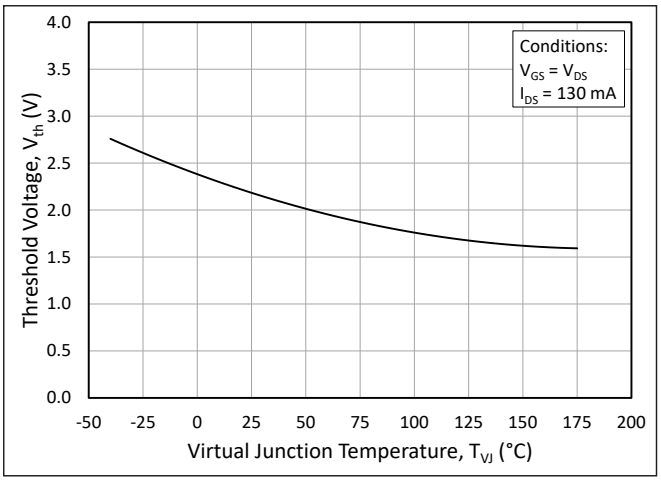


Figure 10. Threshold Voltage vs. Junction Temperature

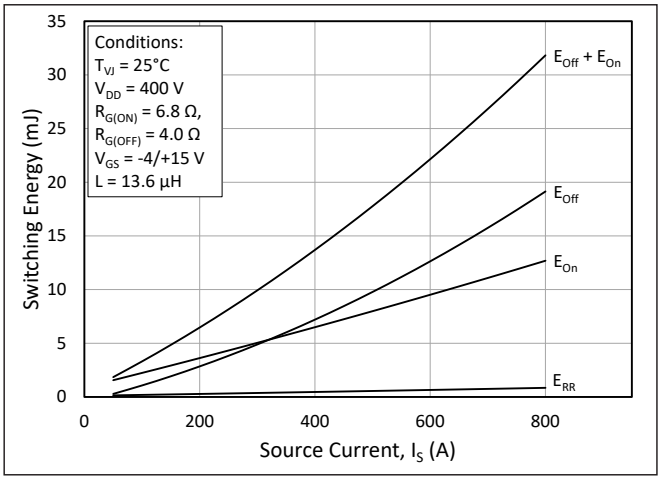


Figure 11. Switching Energy vs. Drain Current (V_{DS} = 400 V)

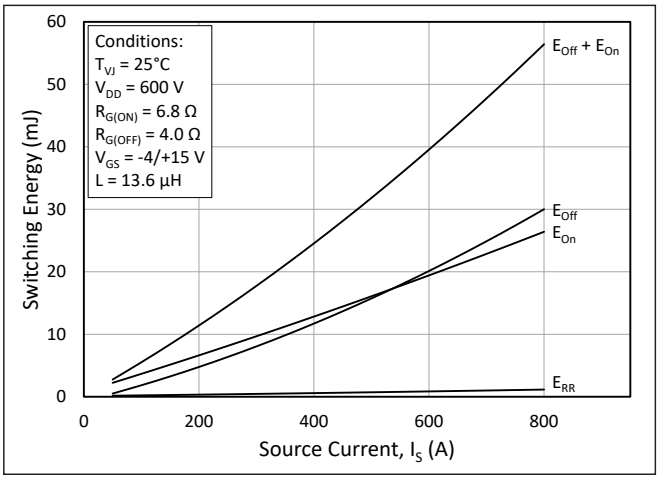


Figure 12. Switching Energy vs. Drain Current (V_{DS} = 600 V)

Typical Performance

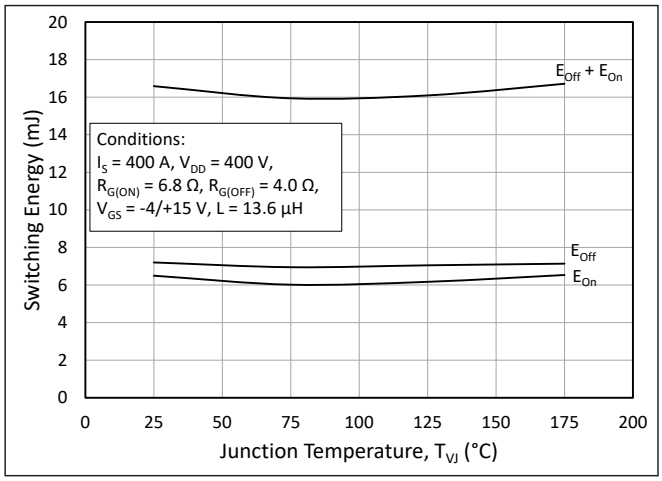


Figure 13. MOSFET Switching Energy vs. Junction Temperature

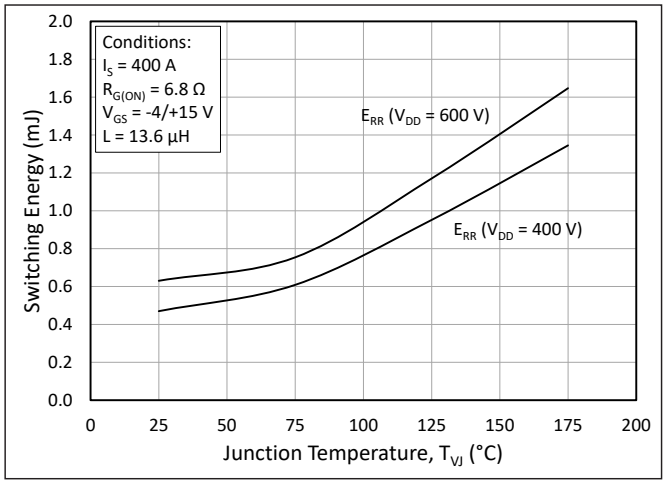


Figure 14. Reverse Recovery Energy vs. Junction Temperature

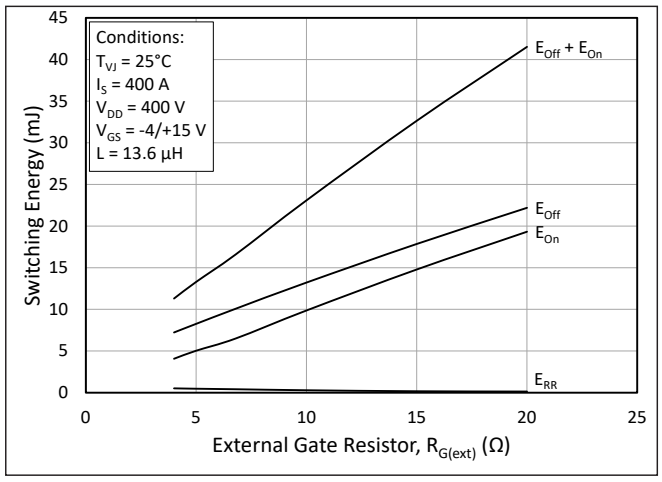


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

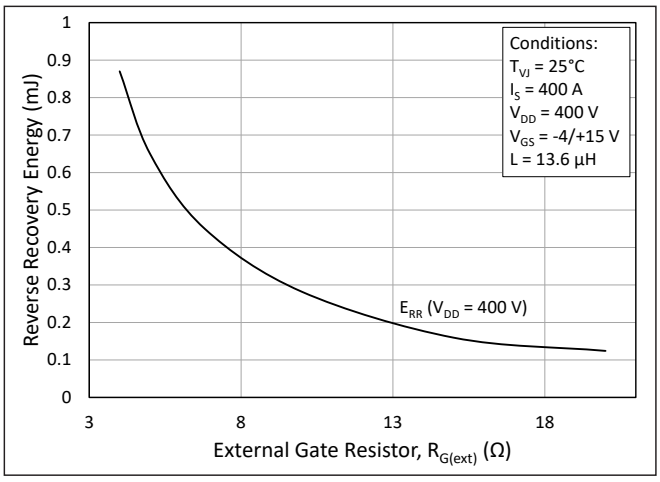


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

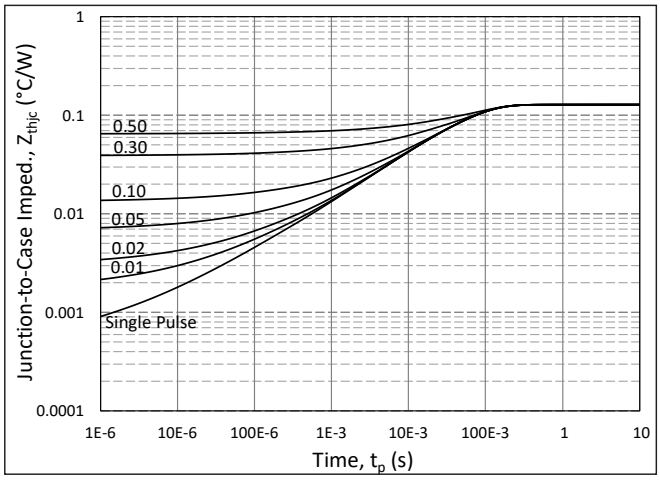


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, $Z_{th\ JC}$ (°C/W)

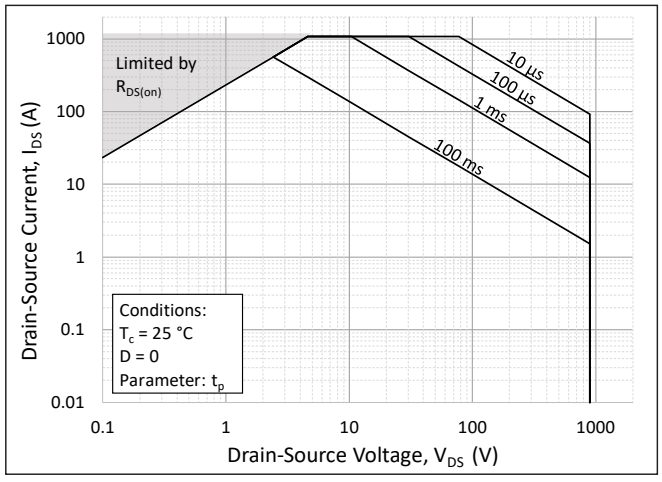


Figure 18. Forward-Bias Safe Operating Area (FBSOA)

Typical Performance

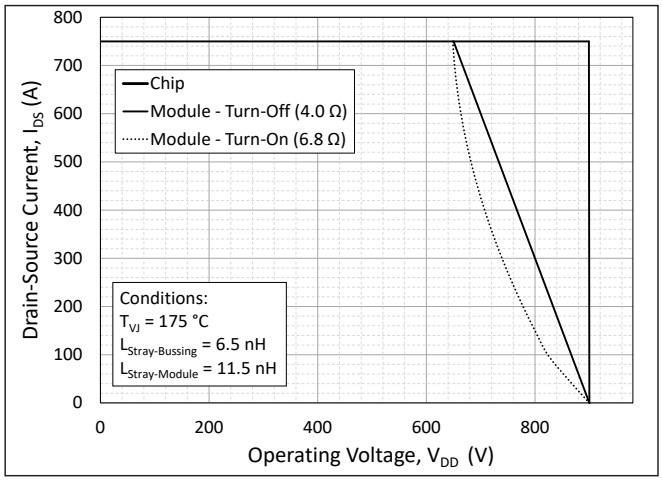


Figure 19. Reverse-Bias Safe Operating Area (RBSOA)

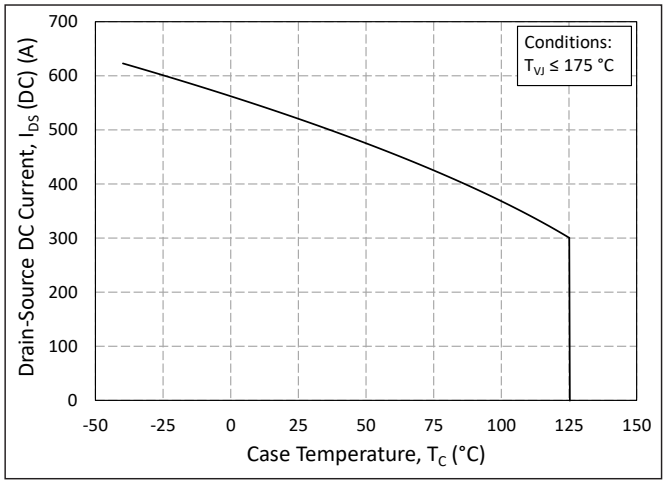


Figure 20. Continuous Drain Current Derating vs. Case Temperature

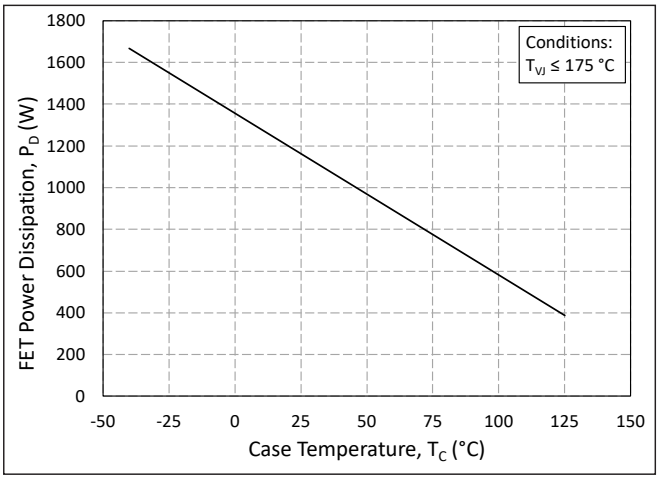


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

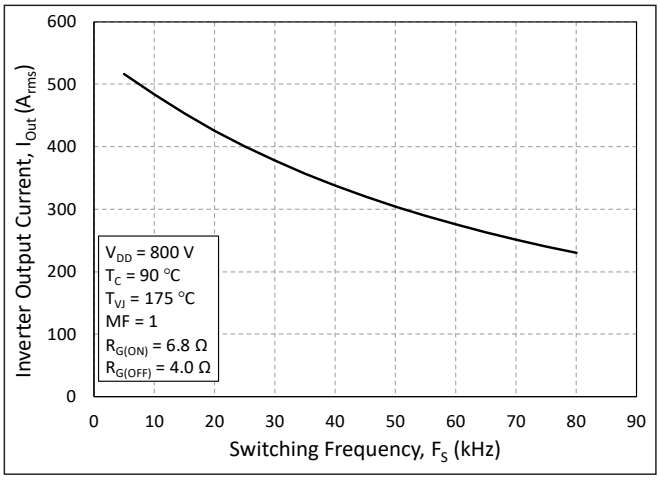


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

Timing Characteristics

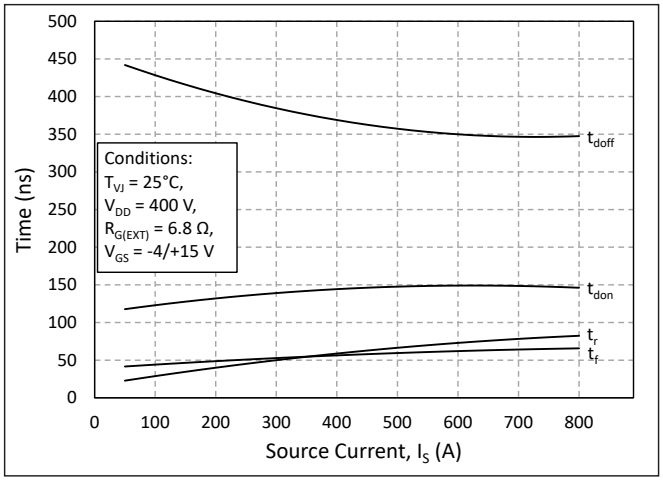


Figure 23. Timing vs. Source Current

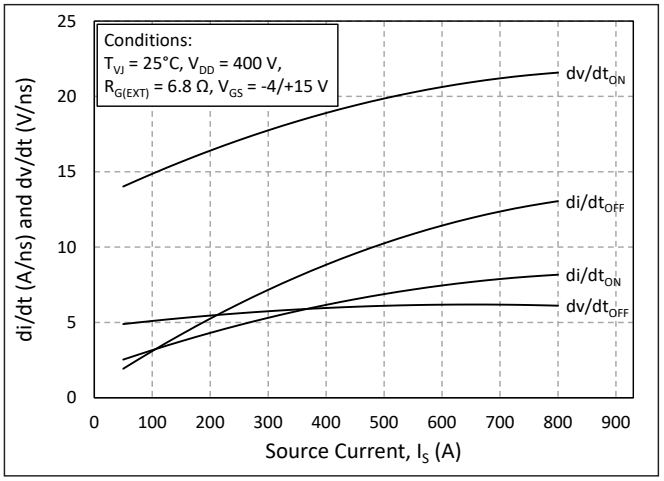


Figure 24. dv/dt and di/dt vs. Source Current

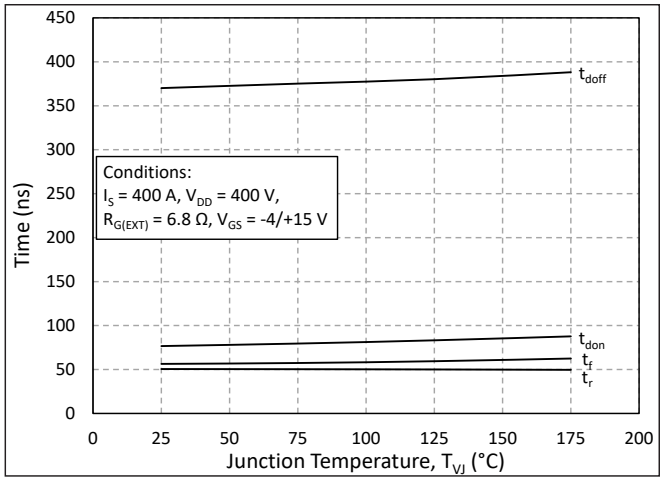


Figure 25. Timing vs. Junction Temperature

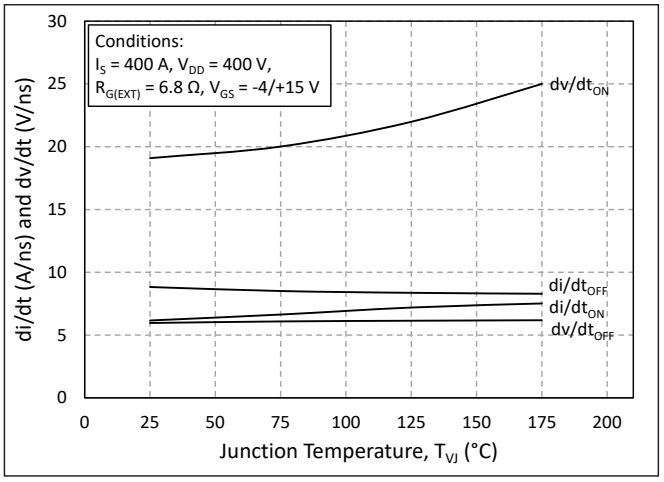


Figure 26. dv/dt and di/dt vs. Junction Temperature

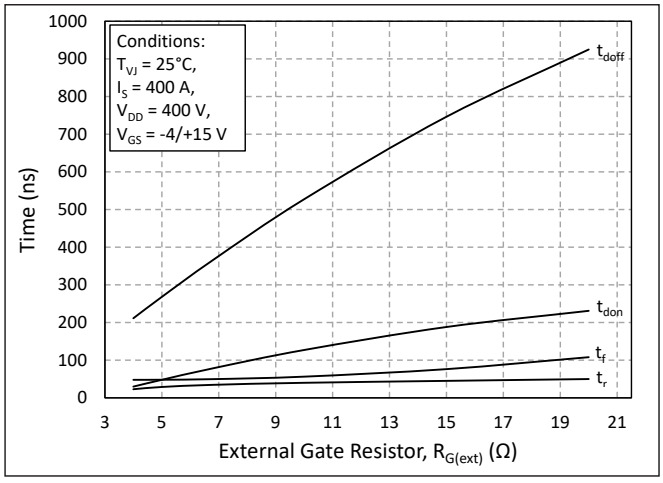


Figure 27. Timing vs. External Gate Resistance

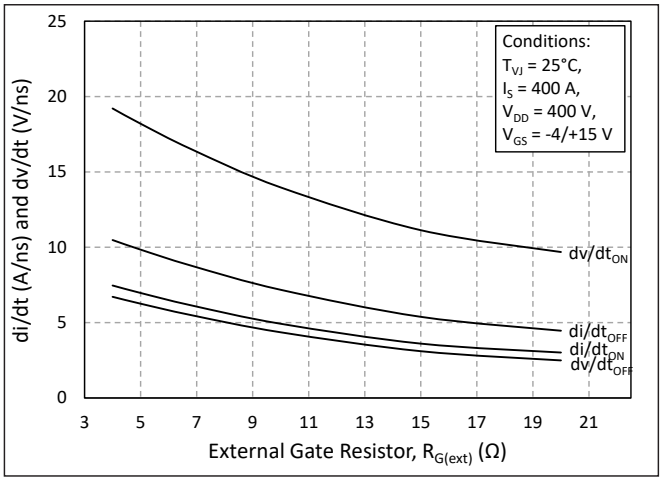


Figure 28. dv/dt and di/dt vs. External Gate Resistance

Definitions

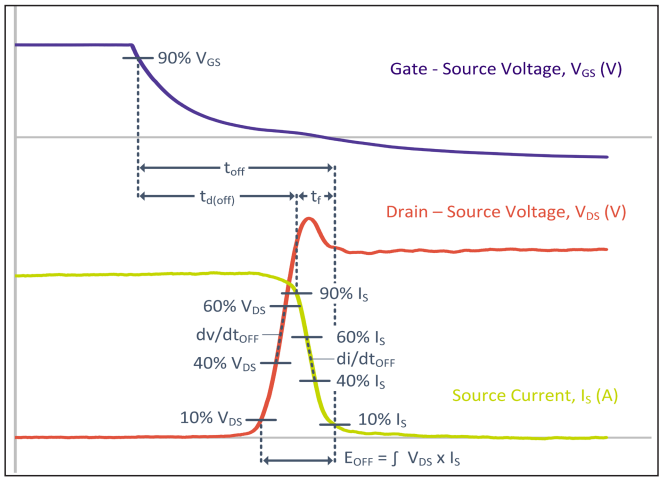


Figure 29. Turn-off Transient Definitions

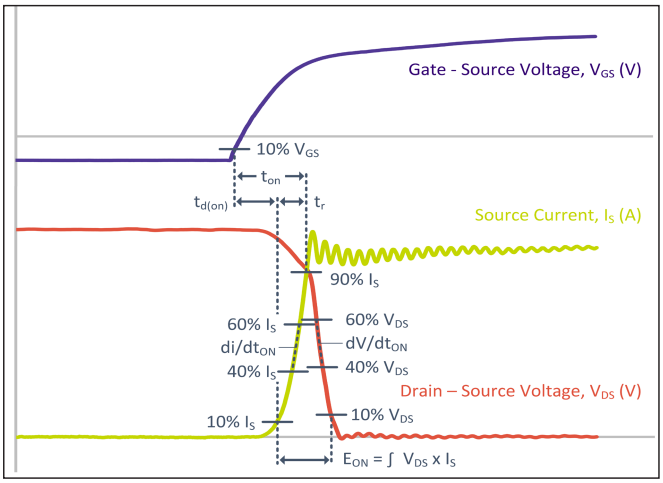


Figure 30. Turn-on Transient Definitions

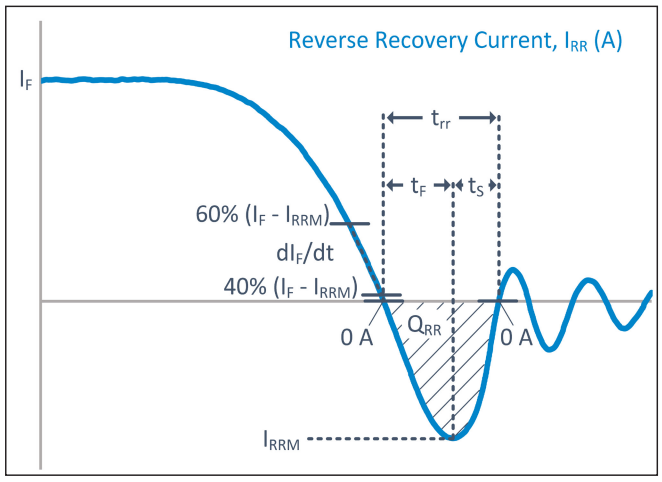


Figure 31. Reverse Recovery Definitions

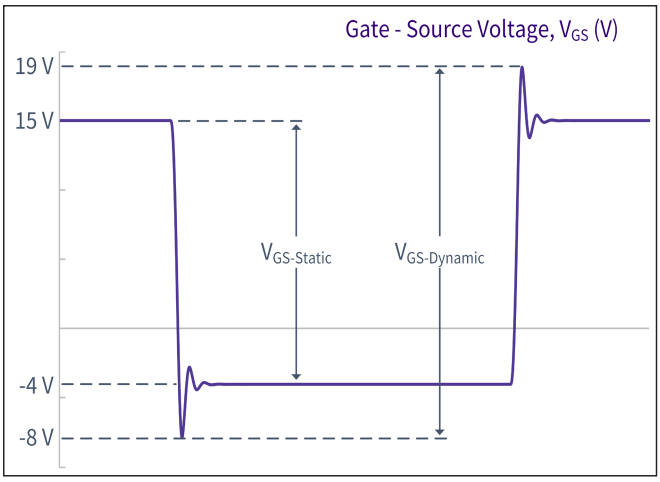
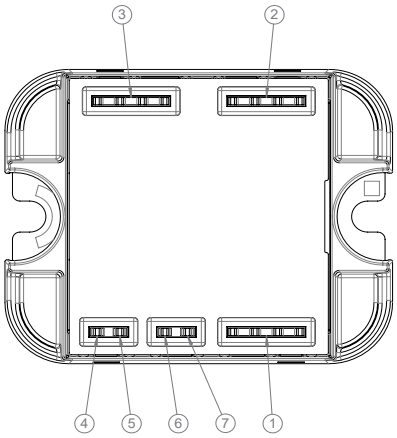
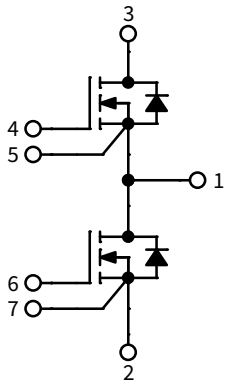


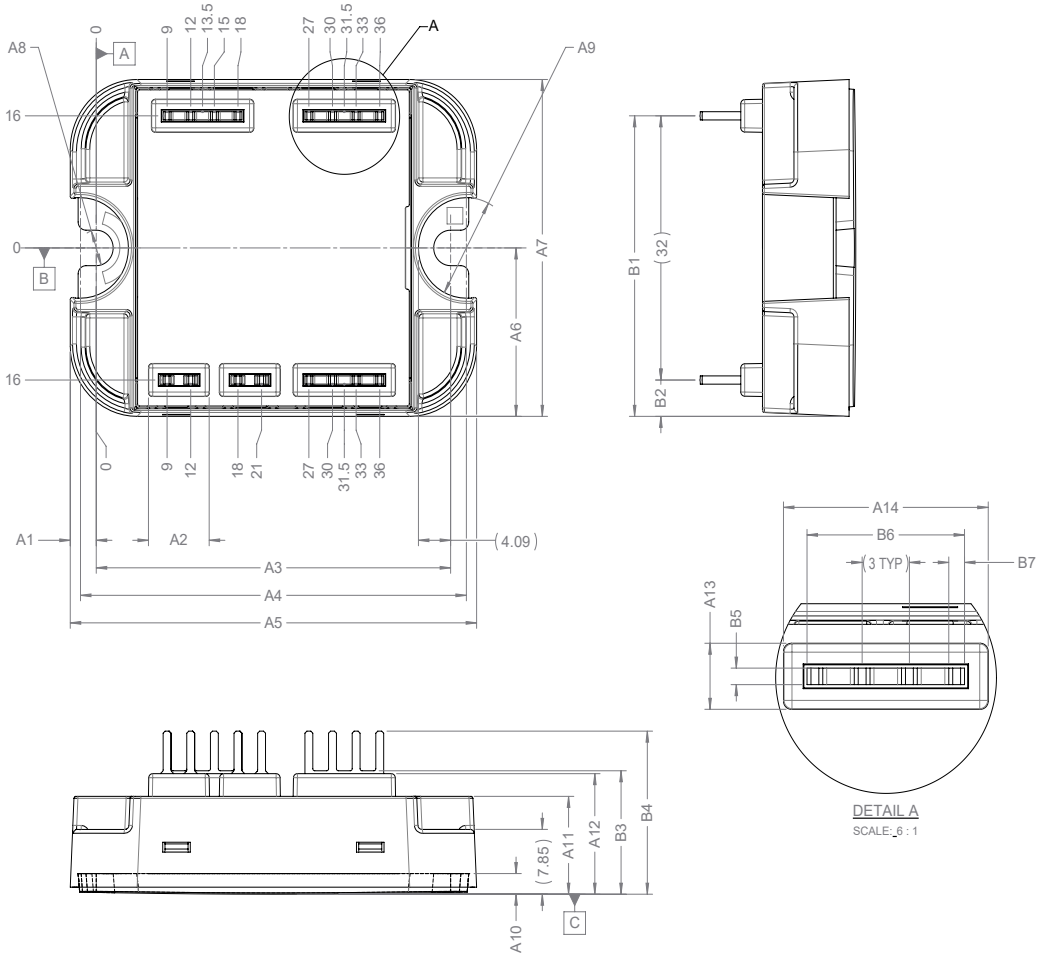
Figure 32. V_{GS} Transient Definitions

Schematic and Pin Out





Package Dimensions (mm)



SYMBOL	DIMENSION	TOLERANCE
A1	3.3	±0.65
A2	7.75	±0.50
A3	45	±0.30
A4	49	±0.50
A5	51.6	±0.50
A6	20.4	±0.65
A7	40.8	±0.20
B1	36.4	±0.50
B2	4.4	±0.50
A8	∅4.3	±0.20
A9	∅12.17	±0.50
A10	2.5	±0.30
A11	11.89	$^{+1}/_{-0.65}$
A12	14.64	±0.55
B3	14.99	±0.50
B4	19.79	±0.50
A13	5× 4	±0.50
B5	5× 1	±0.25
A14	3× 13	±0.50
B6	3× 10	±0.50
B7	16× 1	±0.25
ALL CONNECTORS:		±0.75

Supporting Links & Tools

Evaluation Tools & Support

- SpeedFit 2.0 Design Simulator™
- Technical Support Forum
- LTspice and PLECS Models

Dual-Channel Gate Driver Board

- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers
- CGD1700HB2M-UNA: Wolfspeed Gate Driver Board

Application Notes and User Guides

- PRD-07634: Wolfspeed DM Module Mounting User Guide
- PRD-07635: Impact of PCB Design on Wolfspeed DM Module Ampacity
- PRD-07933: Wolfspeed Power Module Thermal Interface Material Application User Guide
- PRD-08333: Wolfspeed Module CIL Evaluation Kits User Guide

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