

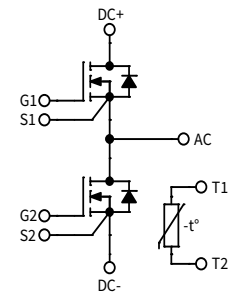
CAB004M12GM4, CAB004M12GM4T

1200 V, 4 mΩ, Silicon Carbide, Half-Bridge Module

V_{DS}	1200 V
$R_{DS(on)}$	4 mΩ

Technical Features

- Ultra-Low Loss
- High Frequency Operation
- Zero Turn-Off Tail Current from MOSFET
- Normally-Off, Fail-Safe Device Operation
- Optional Pre-Applied Thermal Interface Material
- Features Gen4 Technology with Soft Body Diode



Typical Applications

- EV Chargers
- High-Efficiency Converters / Inverters
- Renewable Energy
- Smart-Grid / Grid-Tied Distributed Generation

System Benefits

- Enables Compact, Lightweight Systems
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC
- Reduced Thermal Requirements and System Cost

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Voltage	V_{DS}			1200	V	$T_{HS} = 25\text{ }^{\circ}\text{C}$	
Maximum Gate-Source Voltage	$V_{GS(max)}$	-8		+19		Transient	Fig. 33
Operational Gate-Source Voltage	$V_{GS(op)}$		-4/15			Static	Note 1
DC Continuous Drain Current ($T_{VJ} \leq 150\text{ }^{\circ}\text{C}$)	I_D			200	A	$V_{GS} = 15\text{ V}, T_{HS} = 50\text{ }^{\circ}\text{C}, T_{VJ} \leq 150\text{ }^{\circ}\text{C}$	Notes 2,3 Fig. 20
DC Continuous Drain Current ($T_{VJ} \leq 175\text{ }^{\circ}\text{C}$)				200		$V_{GS} = 15\text{ V}, T_{HS} = 50\text{ }^{\circ}\text{C}, T_{VJ} \leq 175\text{ }^{\circ}\text{C}$	
Pulsed Drain Current	I_{DM}			400		t_{Pmax} limited by T_{VJmax} $V_{GS} = 15\text{ V}, T_{HS} = 50\text{ }^{\circ}\text{C}$	
Power Dissipation	P_D		584		W	$T_{HS} = 50\text{ }^{\circ}\text{C}, T_{VJ} \leq 175\text{ }^{\circ}\text{C}$	Note 4 Fig. 20
Virtual Junction Temperature	$T_{VJ(op)}$	-40		150	$^{\circ}\text{C}$	Operation	
		-40		175	$^{\circ}\text{C}$	Intermittent with Reduced Life	

Note (1): Recommended turn-on gate voltage is 15 V with $\pm 5\%$ regulation tolerance

Note (2): Current limit at $T_{HS} = 50\text{ }^{\circ}\text{C}$ imposed by package

Note (3): Verified by design

Note (4): $P_D = (T_{VJ} - T_{HS}) / R_{TH(JH,typ)}$

MOSFET Characteristics (Per Position) ($T_{VJ} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200				$V_{GS} = 0\text{ V}$, $T_{VJ} = -40\text{ }^{\circ}\text{C}$	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	4.0	V	$V_{DS} = V_{GS}$, $I_D = 75\text{ mA}$	
			2.0			$V_{DS} = V_{GS}$, $I_D = 75\text{ mA}$, $T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}		8	800	μA	$V_{GS} = 0\text{ V}$, $V_{DS} = 1200\text{ V}$	
Gate-Source Leakage Current	I_{GSS}		160	3200	nA	$V_{GS} = 19\text{ V}$, $V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(on)}$		4.1	5.2	m Ω	$V_{GS} = 15\text{ V}$, $I_D = 240\text{ A}$, $T_{VJ} = 25\text{ }^{\circ}\text{C}$	Fig. 2 Fig. 3
			6.4			$V_{GS} = 15\text{ V}$, $I_D = 240\text{ A}$, $T_{VJ} = 150\text{ }^{\circ}\text{C}$	
			7.2			$V_{GS} = 15\text{ V}$, $I_D = 240\text{ A}$, $T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Transconductance	g_{fs}		163		S	$V_{DS} = 20\text{ V}$, $I_D = 240\text{ A}$, $T_{VJ} = 25\text{ }^{\circ}\text{C}$	Fig. 4
			180			$V_{DS} = 20\text{ V}$, $I_D = 240\text{ A}$, $T_{VJ} = 175\text{ }^{\circ}\text{C}$	
Turn-On Switching Energy, $T_{VJ} = 25\text{ }^{\circ}\text{C}$ $T_{VJ} = 125\text{ }^{\circ}\text{C}$ $T_{VJ} = 175\text{ }^{\circ}\text{C}$	E_{On}		2.2 2.0 2.1		mJ	$V_{DD} = 600\text{ V}$, $I_D = 200\text{ A}$, $V_{GS} = -4\text{ V}/15\text{ V}$, $R_{G(OFF)} = 0\text{ }\Omega$, $R_{G(ON)} = 0\text{ }\Omega$, $L_{\sigma} = 11\text{ nH}$	Fig. 11 Fig. 13
Turn-Off Switching Energy, $T_{VJ} = 25\text{ }^{\circ}\text{C}$ $T_{VJ} = 125\text{ }^{\circ}\text{C}$ $T_{VJ} = 175\text{ }^{\circ}\text{C}$	E_{Off}		1.0 0.8 0.9				
Internal Gate Resistance	$R_{G(int)}$		0.53		Ω	$f = 100\text{ kHz}$	
Input Capacitance	C_{iss}		26.4		nF	$V_{GS} = 0\text{ V}$, $V_{DS} = 800\text{ V}$, $V_{AC} = 25\text{ mV}$, $f = 100\text{ kHz}$	Fig. 9
Output Capacitance	C_{oss}		1.0				
Reverse Transfer Capacitance	C_{rss}		83				
Gate to Source Charge	Q_{GS}		984		nC	$V_{DS} = 800\text{ V}$, $V_{GS} = -4\text{ V}/15\text{ V}$, $I_D = 240\text{ A}$, Per IEC60747-8-4 page 21	
Gate to Drain Charge	Q_{GD}		160				
Total Gate Charge	Q_G		1144				
FET Thermal Resistance, Junction to Heatsink	$R_{th\text{ JH}}$		0.214		$^{\circ}\text{C}/\text{W}$	Measured with Pre-Applied TIM	Fig. 17

Diode Characteristics (Per Position) ($T_{VJ} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Notes
Body Diode Forward Voltage	V_{SD}		5.4		V	$V_{GS} = -4\text{ V}$, $I_{SD} = 240\text{ A}$	Fig. 7
			4.8			$V_{GS} = -4\text{ V}$, $I_{SD} = 240\text{ A}$, $T_{VJ} = 175\text{ }^{\circ}\text{C}$	
DC Source-Drain Current (Body Diode)	$I_{SD\text{ BD}}$		130		A	$V_{GS} = -4\text{ V}$, $T_{HS} = 50\text{ }^{\circ}\text{C}$, $T_{VJ} \leq 175\text{ }^{\circ}\text{C}$	Note 3 Fig. 20
Reverse Recovery Time	t_{RR}		26.9		ns	$V_{GS} = -4\text{ V}$, $I_{SD} = 200\text{ A}$, $V_R = 600\text{ V}$ $di/dt = 23.2\text{ A/ns}$, $T_{VJ} = 175\text{ }^{\circ}\text{C}$	Fig. 32
Reverse Recovery Charge	Q_{RR}		5.3		μC		
Peak Reverse Recovery Current	I_{RRM}		329		A		
Reverse Recovery Energy, $T_{VJ} = 25\text{ }^{\circ}\text{C}$ $T_{VJ} = 125\text{ }^{\circ}\text{C}$ $T_{VJ} = 175\text{ }^{\circ}\text{C}$	E_{RR}		1.3 1.5 2.0		mJ	$V_{DD} = 600\text{ V}$, $I_D = 200\text{ A}$, $V_{GS} = -4\text{ V}/15\text{ V}$, $R_{G(ON)} = 0\text{ }\Omega$, $L_{\sigma} = 11\text{ nH}$	Fig. 14



Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Package Resistance, M1 (High-Side)	R_{HS}		1.37		m Ω	$T_{HS} = 125^{\circ}\text{C}$, Note 5
Package Resistance, M2 (Low-Side)	R_{LS}		1.07			
Stray Inductance	L_{Stray}		5.8		nH	Between DC- and DC+, $f = 10\text{ MHz}$
Case Temperature	T_c	-40		125	$^{\circ}\text{C}$	
Mounting Torque	M_s		2.0	2.3	N-m	M4 bolts
Weight	W		39		g	
Case Isolation Voltage	V_{isol}	3			kV	AC, 50 Hz, 1 minute
Comparative Tracking Index	CTI	200				
Clearance Distance			5.0		mm	Terminal to Terminal
			10.0			Terminal to Heatsink
Creepage Distance			6.3			Terminal to Terminal
			11.5			Terminal to Heatsink

Note (5): Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(on)}$ + Switch Position Package Resistance

Temperature Sensor (NTC) Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Rated Resistance	R_{NTC}		5.0		k Ω	$T_{NTC} = 25^{\circ}\text{C}$
Resistance Tolerance at 25 $^{\circ}\text{C}$	$\Delta R/R$	-5		5	%	
Beta Value ($T_2 = 50^{\circ}\text{C}$)	$\beta_{25/50}$		3380		K	
Beta Value ($T_2 = 80^{\circ}\text{C}$)	$\beta_{25/80}$		3468		K	
Beta Value ($T_2 = 100^{\circ}\text{C}$)	$\beta_{25/100}$		3523		K	
Power Dissipation	P_{Max}			10	mW	$T_{NTC} = 25^{\circ}\text{C}$



Typical Performance

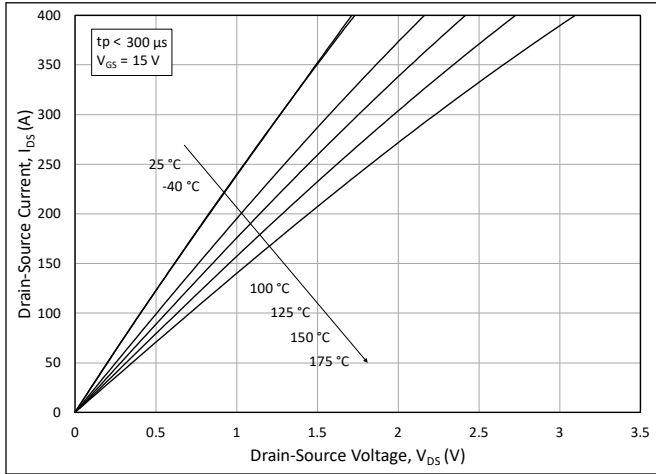


Figure 1. Output Characteristics for Various Junction Temperatures

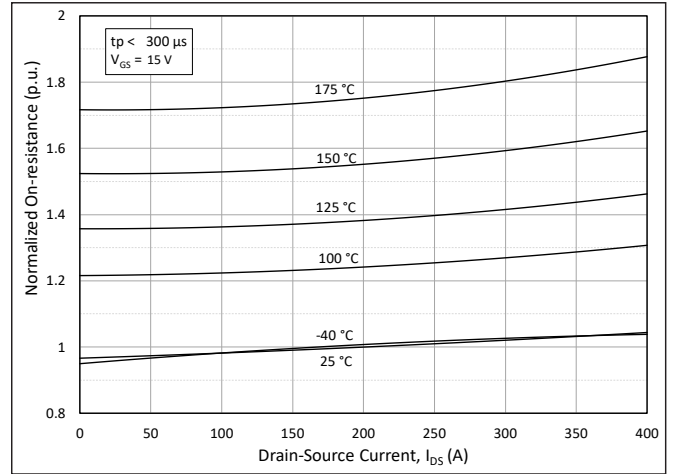


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

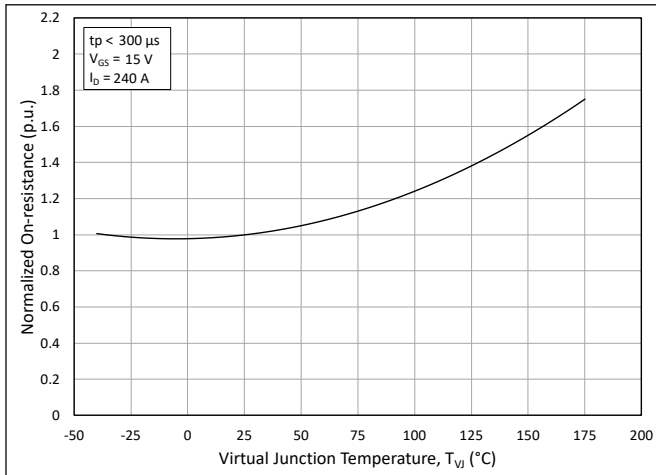


Figure 3. Normalized On-State Resistance vs. Junction Temperature

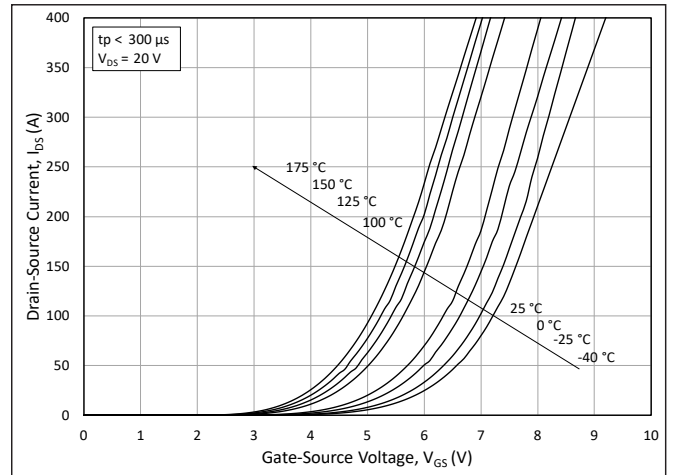


Figure 4. Transfer Characteristic for Various Junction Temperatures

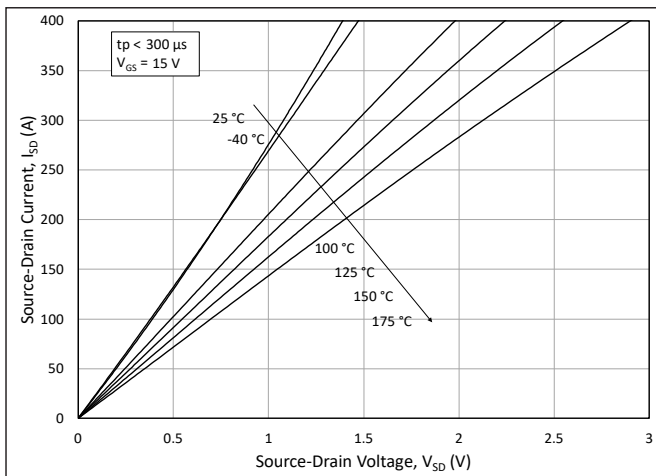


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 15\text{ V}$

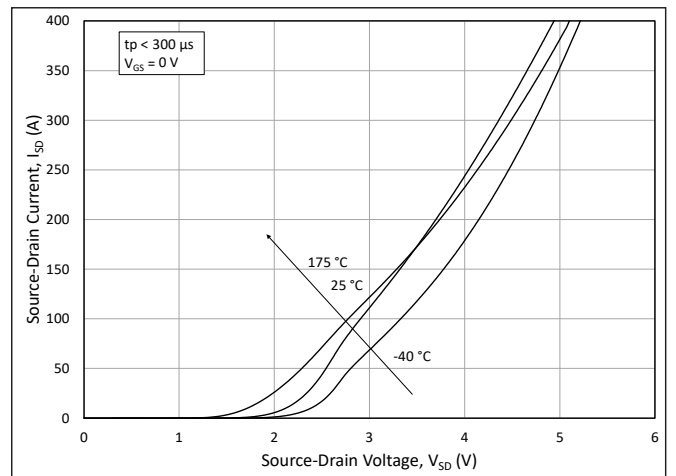


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 0\text{ V}$ (Body Diode)



Typical Performance

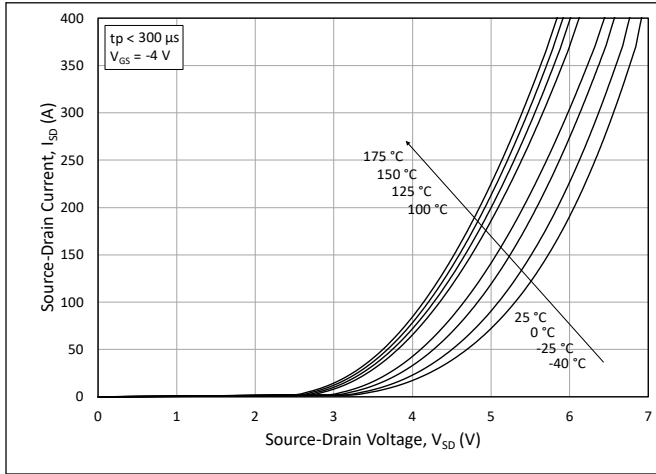


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = -4\text{ V}$ (Body Diode)

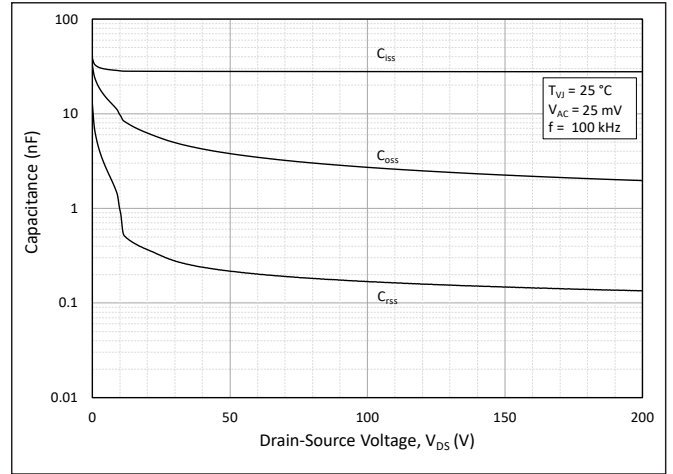


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200V)

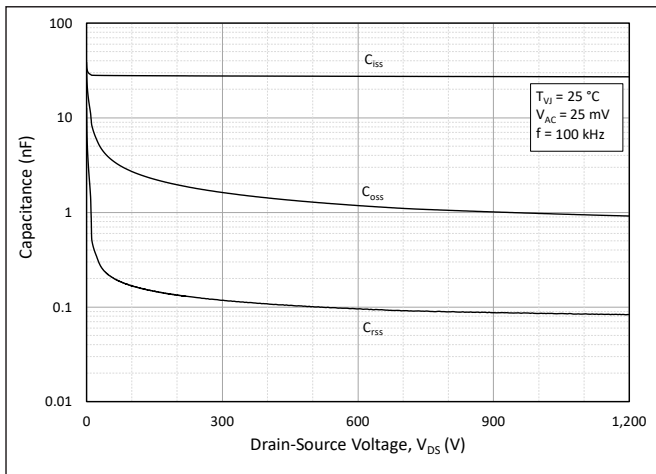


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200V)

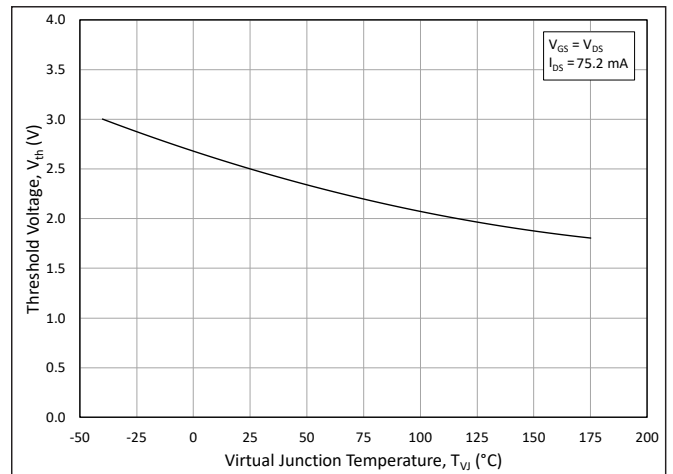


Figure 10. Threshold Voltage vs. Junction Temperature

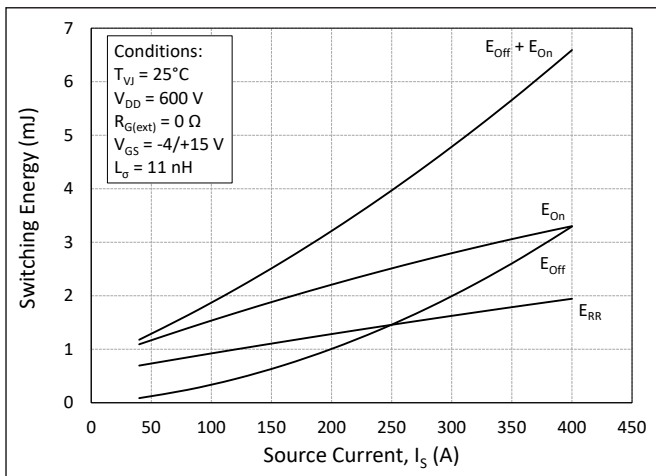


Figure 11. Switching Energy vs. Drain Current ($V_{DD} = 600\text{ V}$)

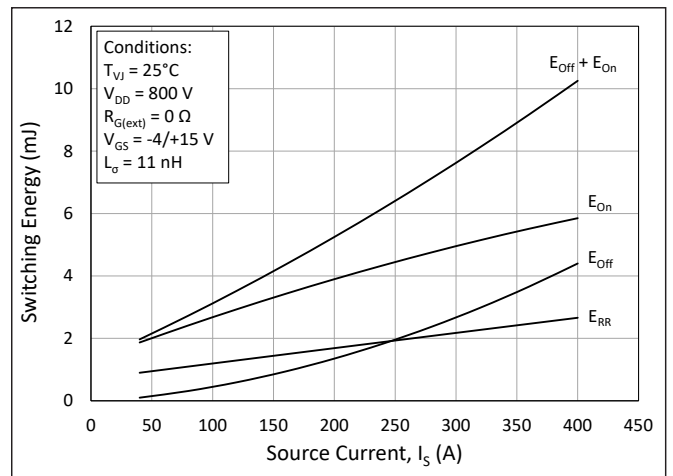


Figure 12. Switching Energy vs. Drain Current ($V_{DD} = 800\text{ V}$)



Typical Performance

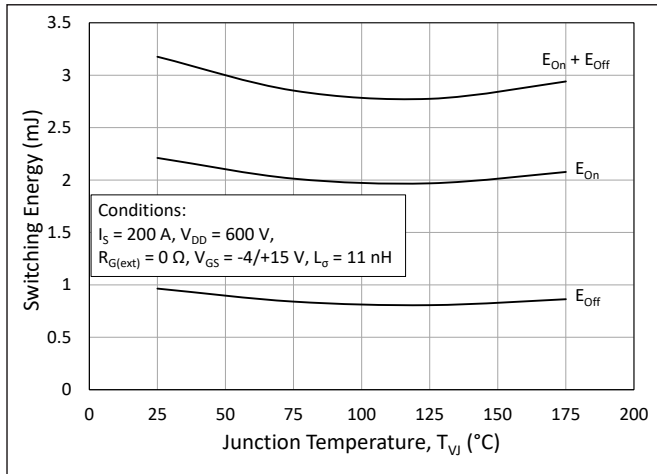


Figure 13. MOSFET Switching Energy vs. Junction Temperature

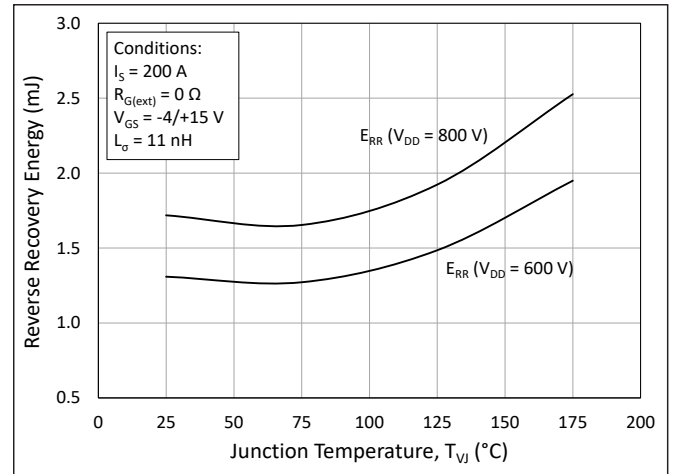


Figure 14. Reverse Recovery Energy vs. Junction Temperature

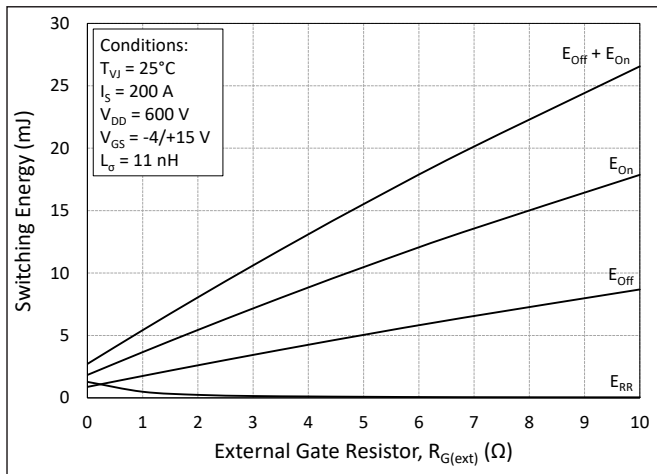


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

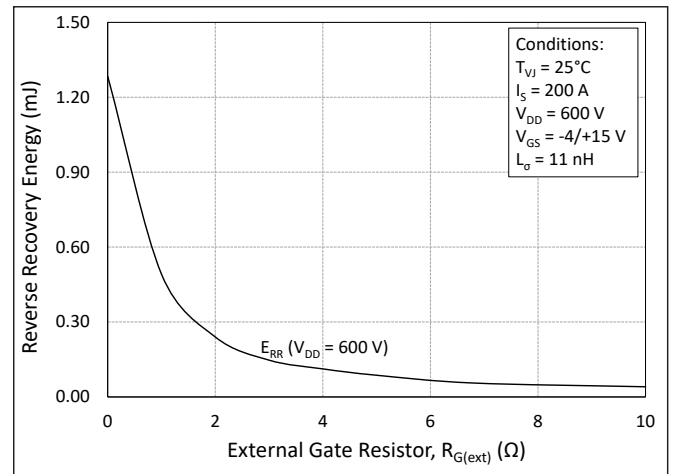


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

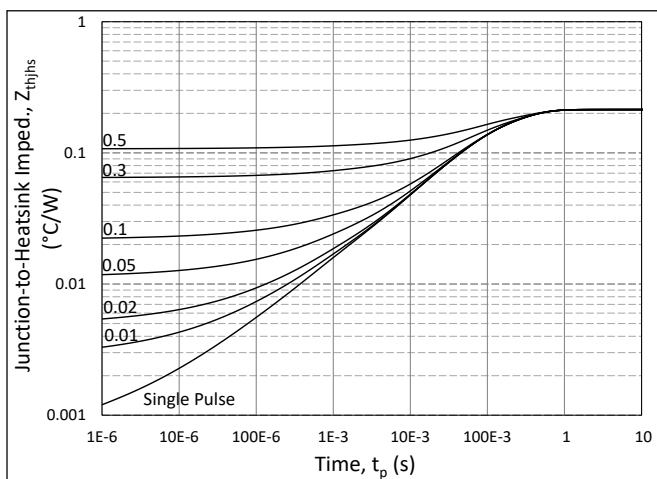


Figure 17. MOSFET Junction to Heatsink Transient Thermal Impedance, Z_{thJHS} (°C/W)

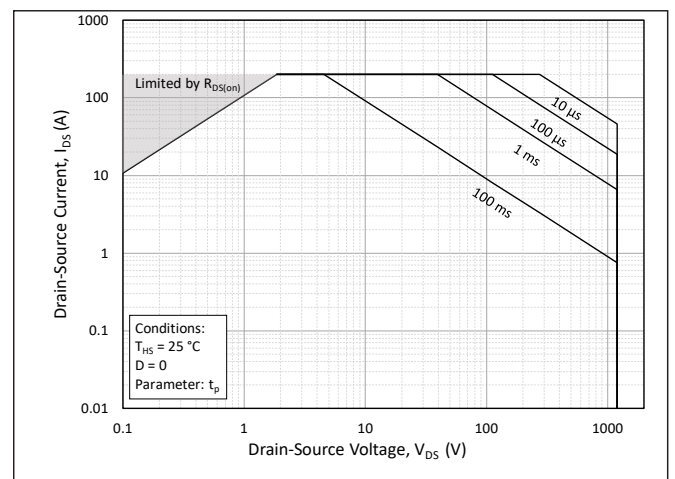


Figure 18. Forward Bias Safe Operating Area (FBSOA)



Typical Performance

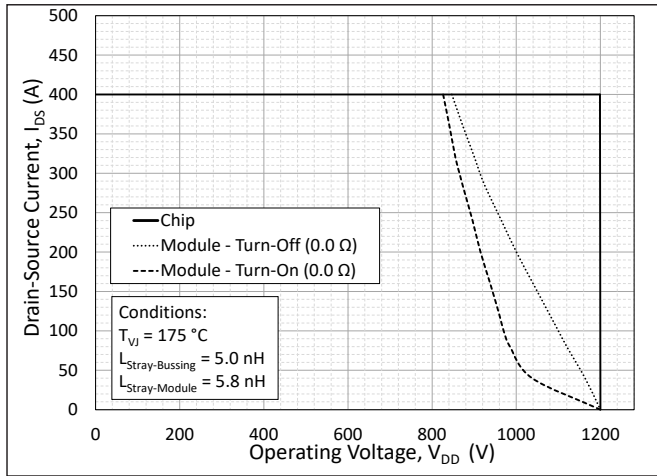


Figure 19. Switching Safe Operating Area

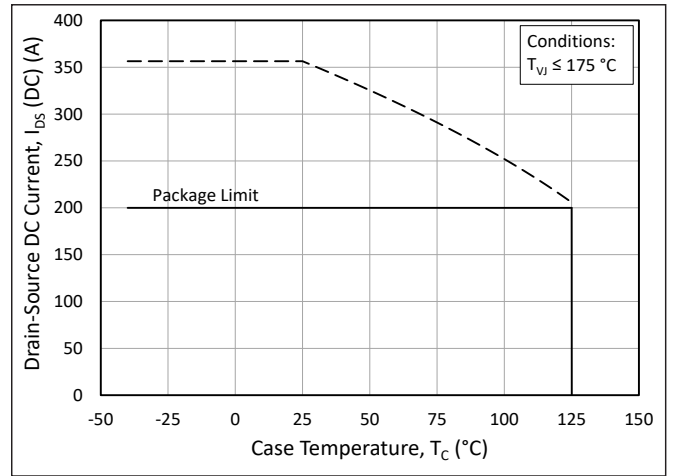


Figure 20. Continuous Drain Current Derating vs. Heatsink Temperature

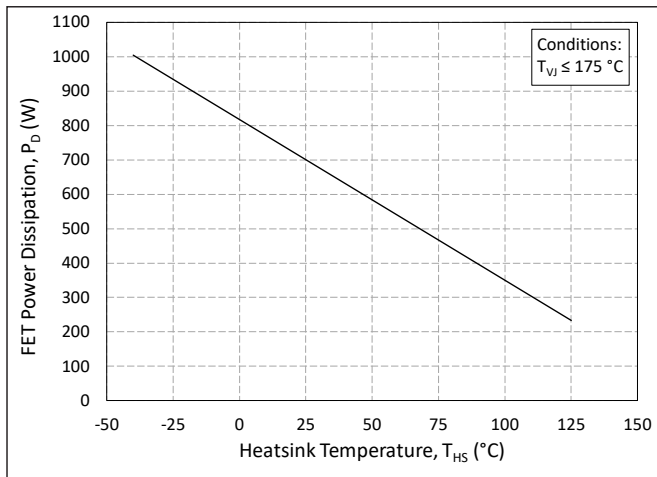


Figure 21. Maximum Power Dissipation Derating vs. Heatsink Temperature

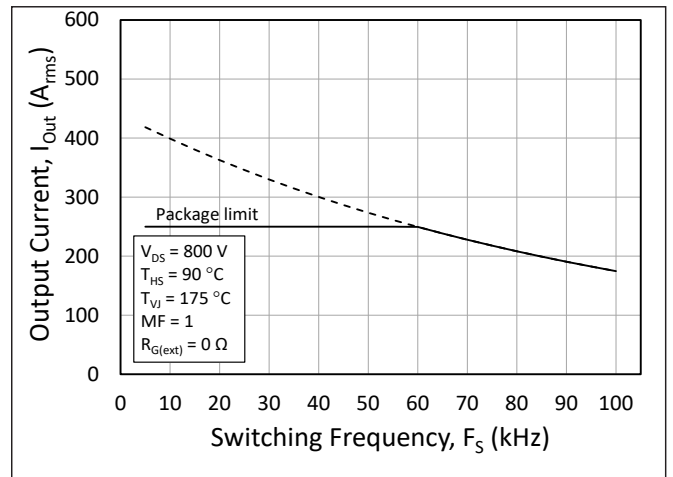


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

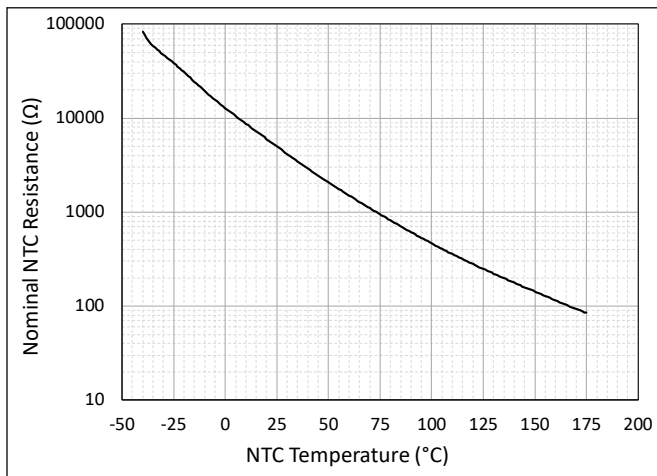


Figure 23. Nominal NTC Resistance vs. NTC Temperature



Timing Characteristics

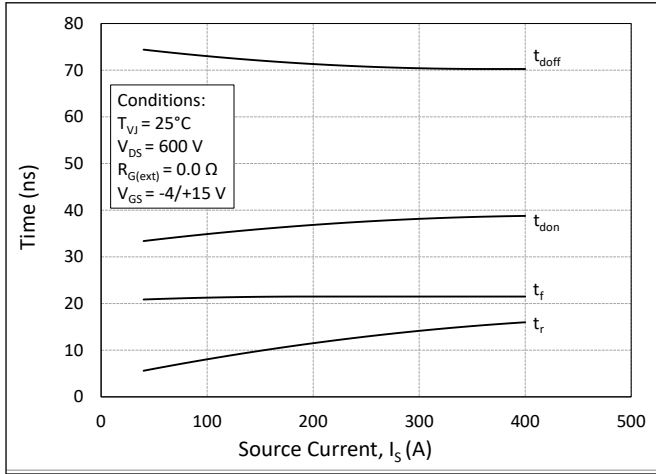


Figure 24. Timing vs. Source Current

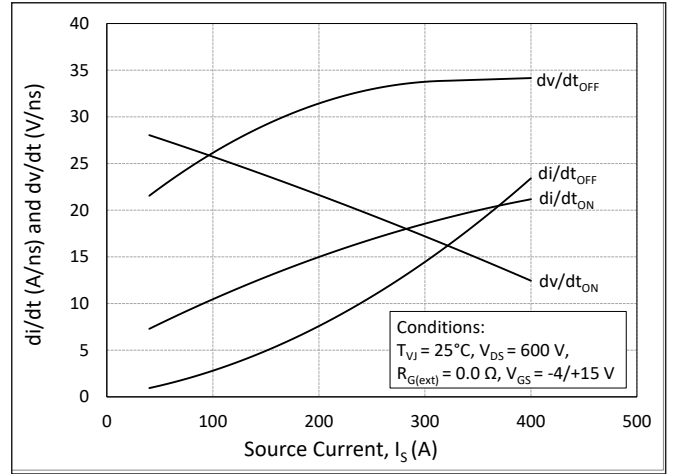


Figure 25. dv/dt and di/dt vs. Source Current

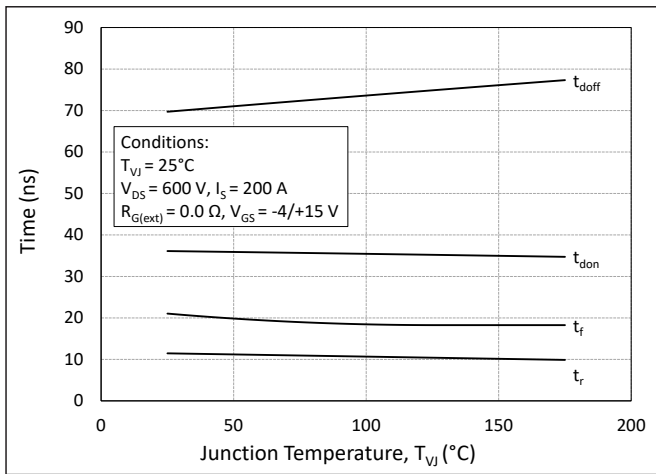


Figure 26. Timing vs. Junction Temperature

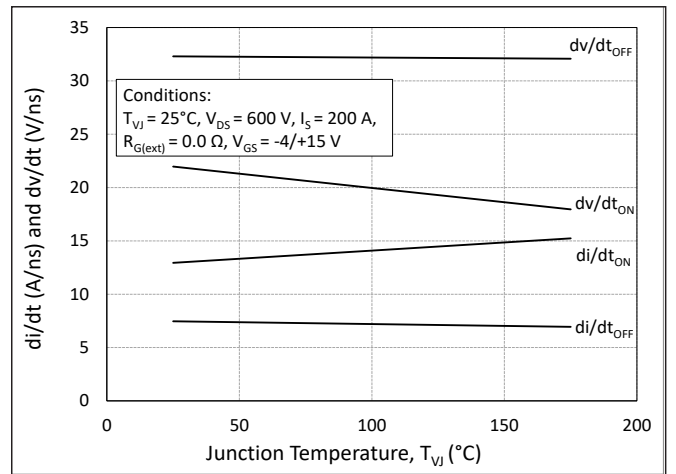


Figure 27. dv/dt and di/dt vs. Junction Temperature

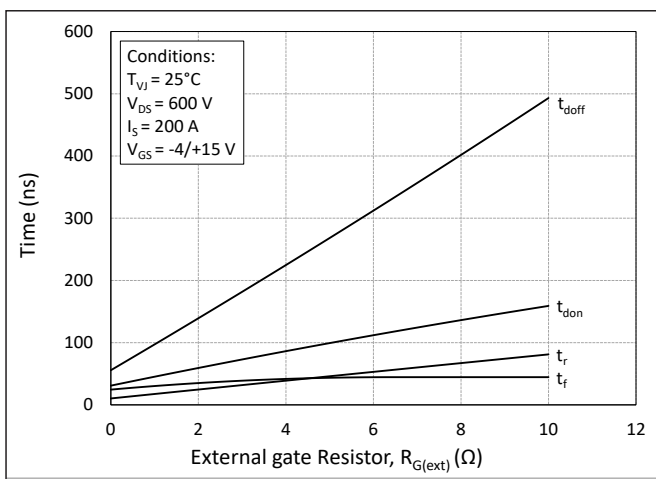


Figure 28. Timing vs. External Gate Resistance

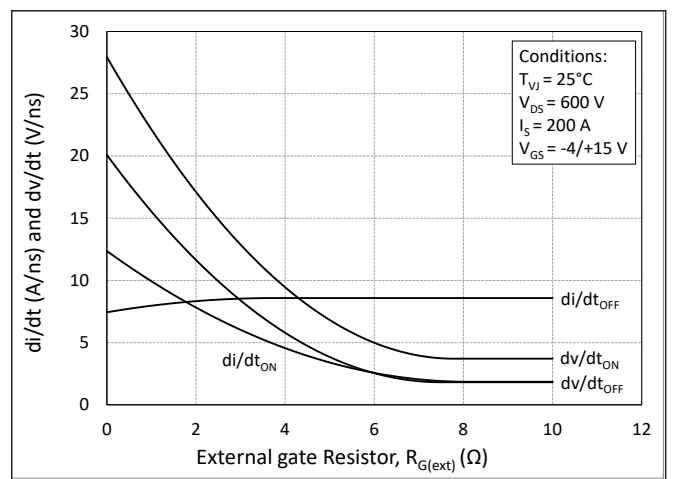


Figure 29. dv/dt and di/dt vs. External Gate Resistance



Definitions

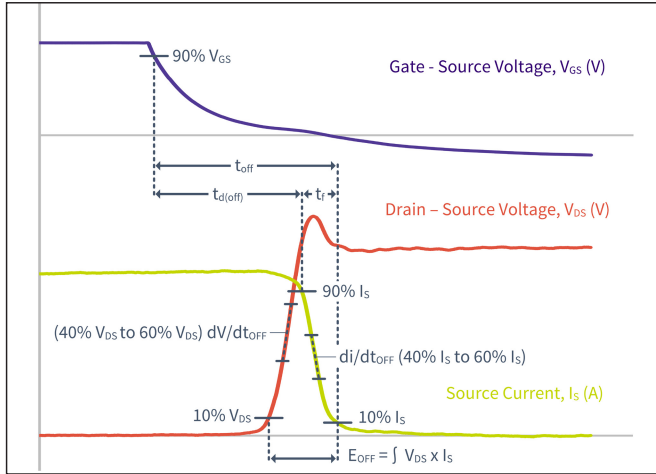


Figure 30. Turn-off Transient Definitions

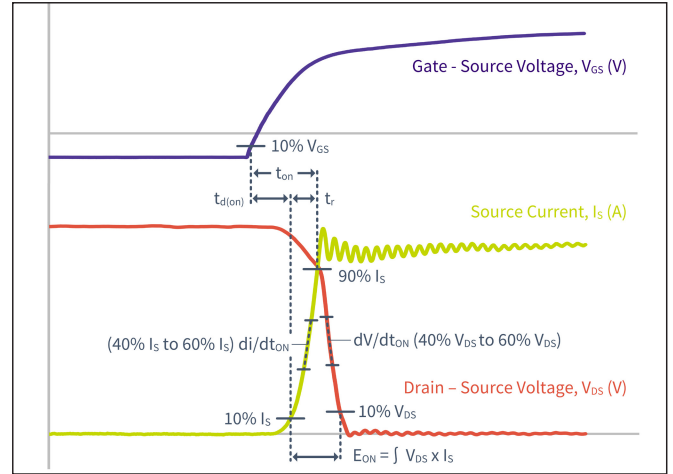


Figure 31. Turn-on Transient Definitions

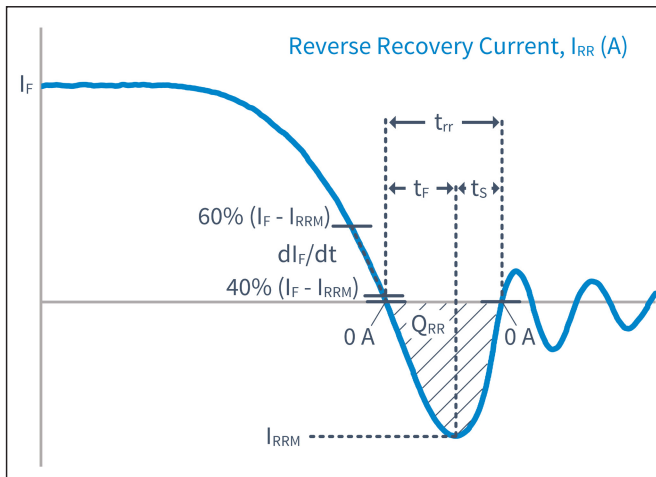


Figure 32. Reverse Recovery Definitions

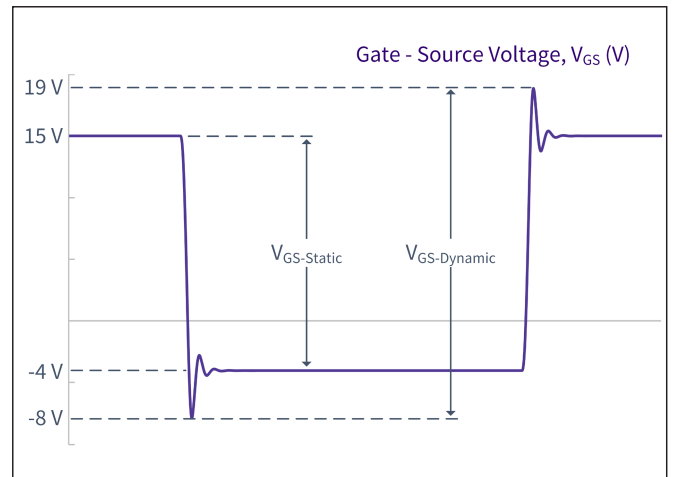
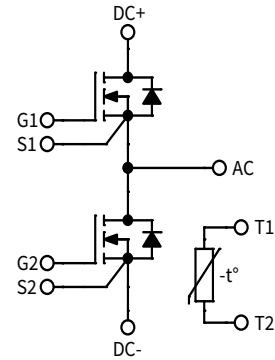
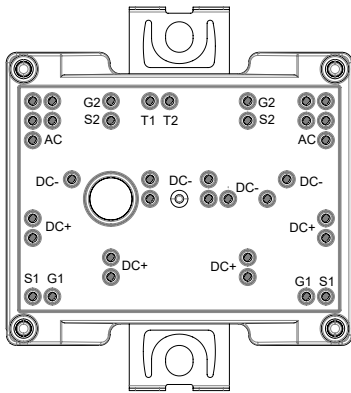


Figure 33. V_{GS} Transient Definitions

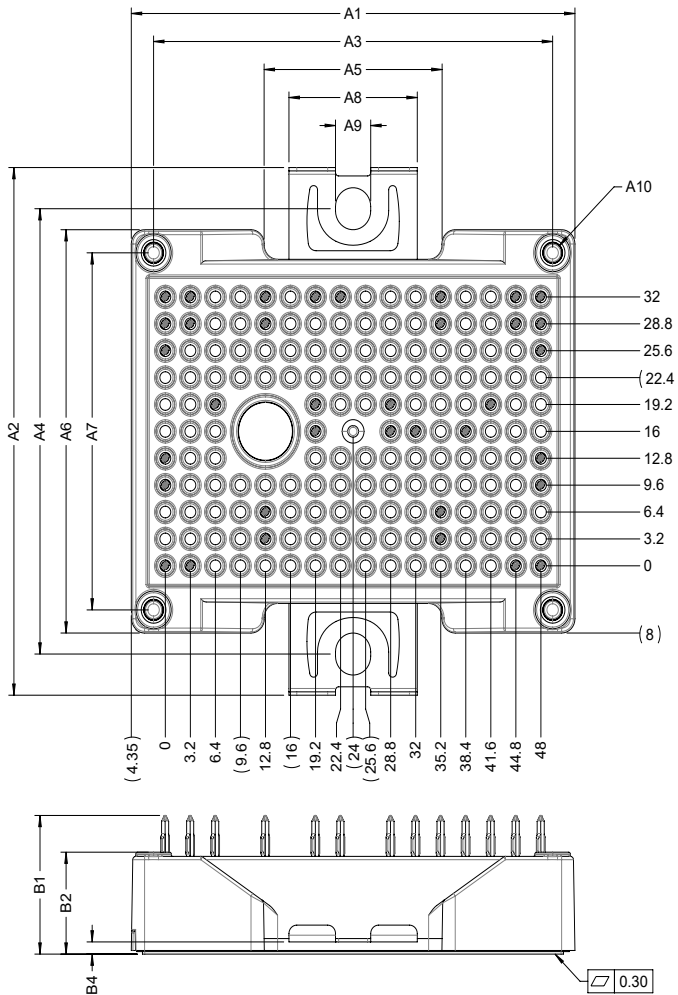
Note (6): The CGD1700HB2M-UNA, which features the UCC21710 gate driver IC from Texas Instruments, was used to evaluate dynamic performance. The typical parasitic turn-on resistance of 2.5Ω and the parasitic turn-off resistance of 0.3Ω are not included in the $R_{G(ext)}$ values on this datasheet.



Schematic and Pin out



Package Dimension (mm)



DIMENSION TABLE		
SYMBOL	DIMENSION	TOLERANCE
A1	56.7	±0.30
A2	62.8	±0.50
A3	51	±0.15
A4	(53)	REF.
A5	22.7	±0.30
A6	48	±0.30
A7	42.5	±0.15
A8	16.4	±0.20
A9	4.5	±0.10
A10	∅ 2.3 √ 8.5	∅: ⁺⁰ _{-0.10} √: ±0.30
B1	16.4	±0.50
B2	12.33	±0.35
B4	1.65	±0.20
ALL PIN LOCATIONS		±0.40



Product Ordering Code

Part Number	Description
CAB004M12GM4	Without Pre-Applied Phase Change Thermal Interface Material
CAB004M12GM4T	With Pre-Applied Phase Change Thermal Interface Material

Supporting Links & Tools

Evaluation Tools & Support

- [All LTSpice Models](#)
- [All PLECS Models](#)
- [SpeedFit 2.0 Design Simulator™](#)
- [Technical Support Forum](#)

Dual-Channel Gate Driver Board

- [EVAL-ADUM4146WHB1Z: Analog Devices® Gate Driver Board](#)
- [Si823H-AxWA-KIT: Skyworks® Gate Driver Board](#)
- [ACPL-355JC: Broadcom® Gate Driver Board](#)
- [CGD1700HB2M-UNA: Wolfspeed Gate Driver Board](#)
- [CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers](#)

Application Notes

- [CPWR-AN41: Mounting Instructions and PCB Requirements](#)
- [CPWR-AN42: Thermal Interface Material Application Note](#)
- [CPWR-AN45: Dynamic Performance Application Note](#)



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The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfsppeed representative or from the Product Documentation sections of www.wolfsppeed.com.

REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfsppeed representative to ensure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

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