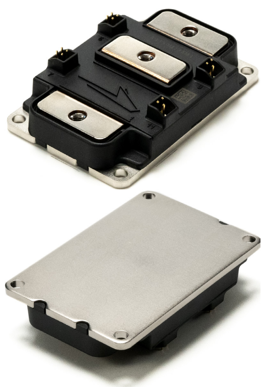
CAB320M17XM3

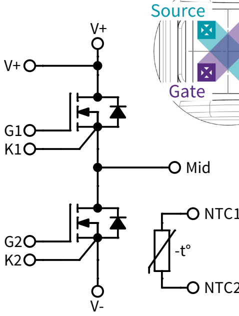
1700 V, 3.5 mΩ, Silicon Carbide, Half-Bridge Module

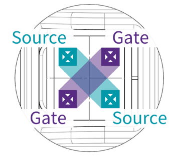
V_{DS}	**1700 V**
I_{DS}	**320 A**

Technical Features

- High Power Density Footprint
- High Junction Temperature (175 °C) Operation
- Low-Inductance (6.7 nH) Design
- Implements Wolfspeed's Third Generation SiC MOSFET Technology
- Silicon Nitride Insulator and Copper Baseplate
- 1700 V Drain-Source Voltage
- Cross-pin Gate-Source Signal Pinout







Typical Applications

- Energy
- Medical
- Motor & Motion Control
- Test and Production Equipment
- Transportation
- Traction Inverters

System Benefits

- Terminal layout allows for direct bus bar connection without bends or bushings enabling a simple, low-inductance design.
- Isolated, integrated temperature sensing enables high-level temperature protection.
- Dedicated high-side Kelvin-drain pin enables direct voltage sensing for gate driver overcurrent protection.
- 1700 V_{DS} allows use with higher bus voltage (typically up to 1.4 kV).

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Drain-Source Voltage	V_{DS}			1700	V	T_C = 25 °C	
Maximum Gate-Source Voltage	$V_{GS\ max}$	-8		+19		Transient	Note 1 Fig. 33
Operational Gate-Source Voltage	$V_{GS\ op}$		-4/+15			Static	
DC Continuous Drain Current (T_{VJ} ≤ 175 °C)	I_D		438		A	V_{GS} = 15 V, T_C = 25 °C, T_{VJ} ≤ 175 °C	Notes 2,3 Fig. 20
			333			V_{GS} = 15 V, T_C = 90 °C, T_{VJ} ≤ 175 °C	
Pulsed Drain Current	I_{DM}		640			t_{Pmax} limited by $T_{VJ\ op}$ V_{GS} = 15 V, T_C = 25 °C	
Power Dissipation	P_D		1546		W	T_C = 25 °C, T_{VJ} ≤ 175 °C	Note 4 Fig. 21
Operational Virtual Junction Temperature	$T_{VJ\ op}$	-40		175	°C		

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance
Note (2): Current Limit calculated by $I_{D(max)} = \sqrt{(P_D / R_{DS(typ)}(T_{VJ(max)}, I_{D(max)}))}$
Note (3): Verified by design
Note (4): $P_D = (T_{VJ} - T_C) / R_{TH(JC,\ Typ)}$

MOSFET Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1700			V	V_{GS} = 0 V, T_{VJ} = -40 °C	
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6	V	V_{DS} = V_{GS}, I_{DS} = 127 mA	
			2.0		V	V_{DS} = V_{GS}, I_{DS} = 127 mA, T_{VJ} = 175 °C	
Zero Gate Voltage Drain Current	I_{DSS}		5	200	μA	V_{GS} = 0 V, V_{DS} = 1700 V	
Gate-Source Leakage Current	I_{GSS}		5	1250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance (MOSFET Only)	$R_{DS(on)}$		3.5	4.6	mΩ	V_{GS} = 15 V, I_D = 320 A	Fig. 2 Fig. 3
			8.0			V_{GS} = 15 V, I_D = 320 A, T_{VJ} = 175 °C	
Transconductance	g_{fs}		256		S	V_{DS} = 20 V, I_D = 320 A	Fig. 4
			250			V_{DS} = 20 V, I_D = 320 A, T_{VJ} = 175 °C	
Turn-On Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{On}		28.4 27.8 30.5		mJ	V_{DD} = 900 V, I_D = 320 A, V_{GS} = -4 V/15 V, $R_{G-ON(ext)}$ = 6.8 Ω, $R_{G-OFF(ext)}$ = 0.0 Ω, $L_σ$ = 10.2 nH	Fig. 11 Fig. 13
Turn-Off Switching Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{Off}		6.9 6.9 6.3				
Internal Gate Resistance	$R_{G(int)}$	1.0	1.5	1.9	Ω	f = 100 kHz	
Input Capacitance	C_{iss}		37.6		nF	V_{GS} = 0 V, V_{DS} = 1000 V, V_{AC} = 25 mV, f = 100 kHz	Fig. 9
Output Capacitance	C_{oss}		1.0				
Reverse Transfer Capacitance	C_{rss}		46		pF		
Gate to Source Charge	Q_{GS}		400		nC	V_{DS} = 1200 V, V_{GS} = -4 V/15 V, I_D = 461 A, Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		350				
Total Gate Charge	Q_G		1245				
FET Thermal Resistance, Junction to Case	$R_{th JC}$		0.097		°C/W		Fig. 17

Diode Characteristics (Per Position) (T_{VJ} = 25 °C unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Notes
Body Diode Forward Voltage	V_{SD}		5.5		V	V_{GS} = -4 V, I_{SD} = 320 A	Fig. 7
			4.7			V_{GS} = -4 V, I_{SD} = 320 A, T_{VJ} = 175 °C	
Reverse Recovery Time	t_{RR}		95		ns	V_{GS} = -4 V, I_{SD} = 320 A, V_R = 900 V, di/dt = 5 A/ns, $R_{G-ON(ext)}$ = 6.8 Ω, T_{VJ} = 175 °C	
Reverse Recovery Charge	Q_{RR}		9.5		μC		
Peak Reverse Recovery Current	I_{RRM}		158		A		
Reverse Recovery Energy, T_{VJ} = 25 °C T_{VJ} = 125 °C T_{VJ} = 175 °C	E_{RR}		0.3 2.0 3.7		mJ	V_{DD} = 900 V, I_D = 320 A, V_{GS} = -4 V/15 V, $R_{G-ON(ext)}$ = 6.8 Ω, $L_σ$ = 10.2 nH	Fig. 14

Temperature Sensor (NTC) Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Resistance at 25°C	R_{25}		4700		Ω	T_{NTC} = 25 °C
Tolerance of R_{25}				±1	%	
Beta Value for 25 °C to 85 °C	$B_{25/85}$		3435		K	
Beta Value for 0 °C to 100 °C	$B_{0/100}$		3399		K	
Tolerance of $B_{25/85}$				±1	%	
Maximum Power Dissipation	P_{25}			50	mW	

Steinhart & Hart Coefficients for NTC Resistance & NTC Temperature Computation (T in K)

$$\ln\left(\frac{R}{R_{25}}\right) = A + \frac{B}{T} + \frac{C}{T^2} + \frac{D}{T^3}$$

A	B	C	D
-1.289E+01	4.245E+03	-8.749E+04	-9.588E+06

$$\frac{1}{T} = A_1 + B_1 \ln\left(\frac{R}{R_{25}}\right) + C_1 \ln^2\left(\frac{R}{R_{25}}\right) + D_1 \ln^3\left(\frac{R}{R_{25}}\right)$$

A_1	B_1	C_1	D_1
3.354E-03	3.001E-04	5.085E-06	2.188E-07

Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Package Resistance, M1 (High-Side)	R_{3-1}		0.72		mΩ	T_C = 125 °C, Note 5 & 6
Package Resistance, M2 (Low-Side)	R_{1-2}		0.63			T_C = 125 °C, Note 5 & 6
Stray Inductance	L_{Stray}		6.7		nH	Between terminals 2 & 3, f = 10 MHz
Case Temperature	T_C	-40		125	°C	
Mounting Torque	M_S	2.0	3.0	4.0	N-m	Baseplate, M4 bolts
		2.0	4.0	5.0		Power Terminals, M5 bolts
Weight	W		175		g	
Case Isolation Voltage	V_{Isol}	4.0			kV	AC, 50 Hz, 1 minute
Comparative Tracking Index	CTI	600				
Clearance Distance		12.5			mm	From 2 to 3, Note 6
		11.5				From 1 to Baseplate, Note 6
		5.7				From 2 to 5, Note 6
		13.7				From 5 to Baseplate, Note 6
Creepage Distance		14.7				From 2 to 3, Note 6
		14.0				From 1 to Baseplate, Note 6
		14.7				From 2 to 5, Note 6
		14.3				From 5 to Baseplate, Note 7

Note (5): Total Effective Resistance (Per Switch Position) = MOSFET $R_{DS(ON)}$ + Switch Position Package Resistance
Note (6): Numbers reference the connections from the Schematics and Pin Out section of this document

Typical Performance

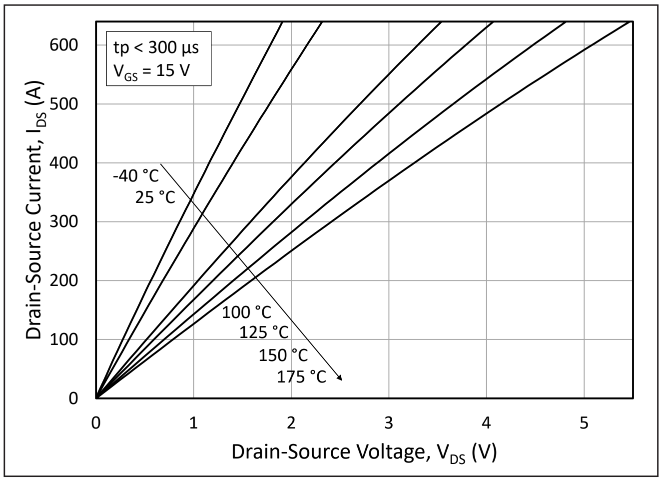


Figure 1. Output Characteristics for Various Junction Temperatures

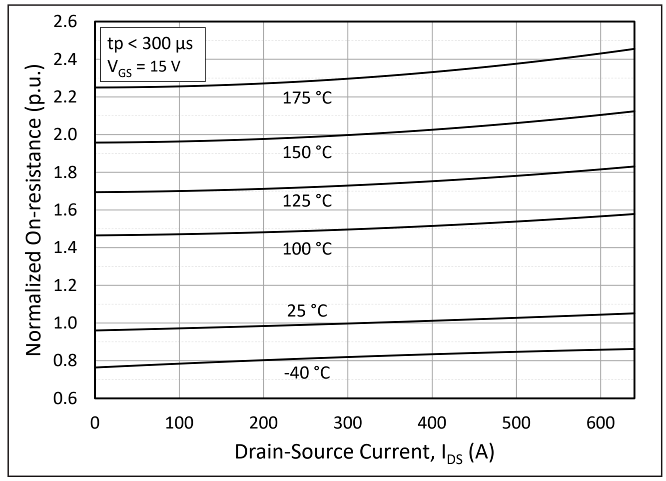


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

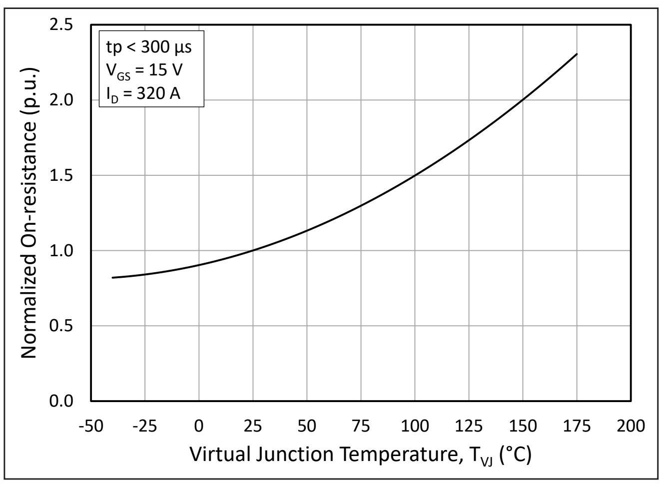


Figure 3. Normalized On-State Resistance vs. Junction Temperature

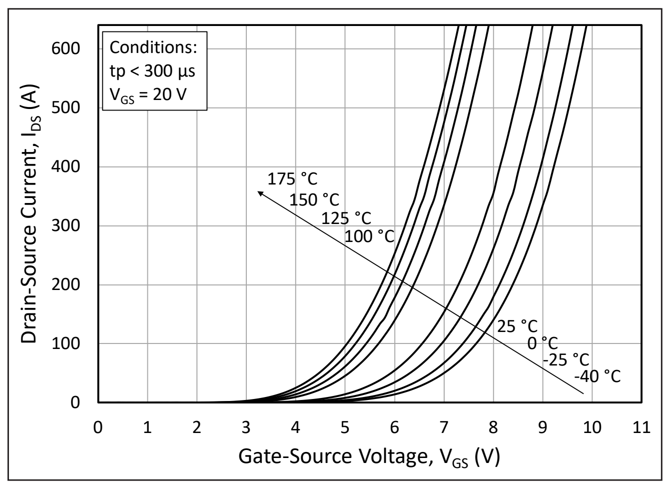


Figure 4. Transfer Characteristic for Various Junction Temperatures

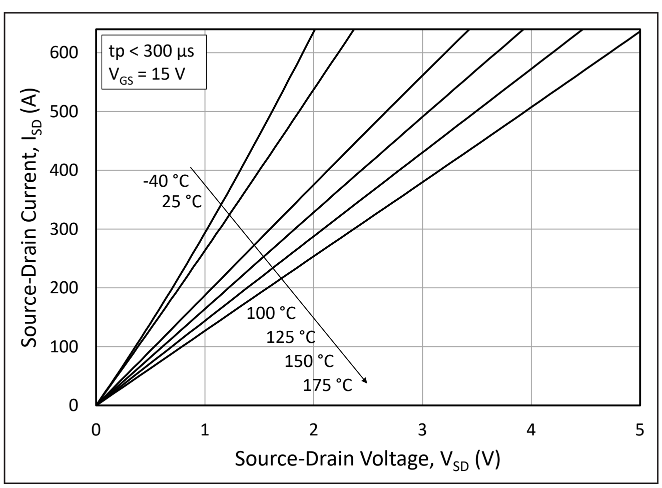


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 15 V

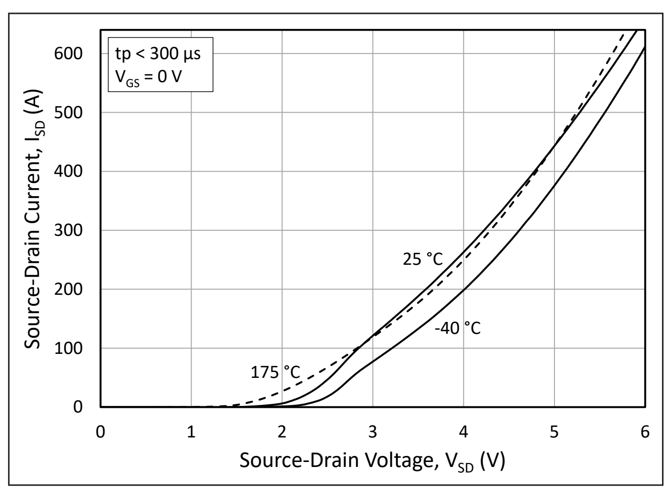


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = 0 V

Typical Performance

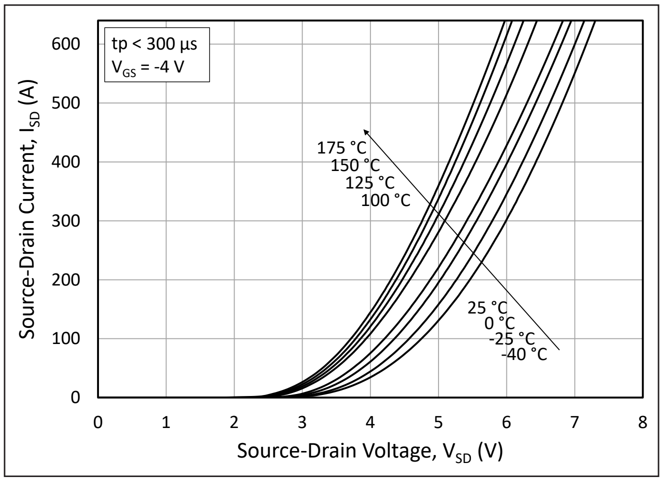


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at V_{GS} = -4 V (Body Diode)

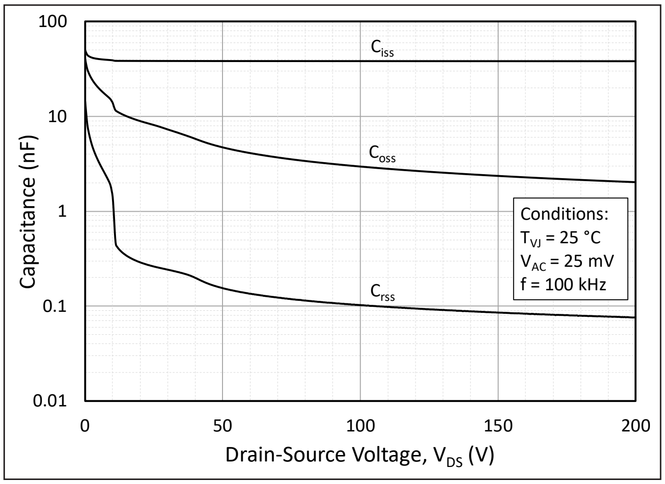


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200 V)

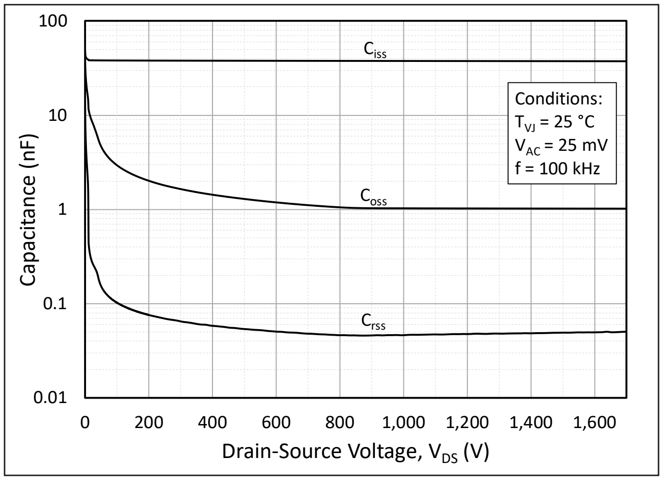


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1700 V)

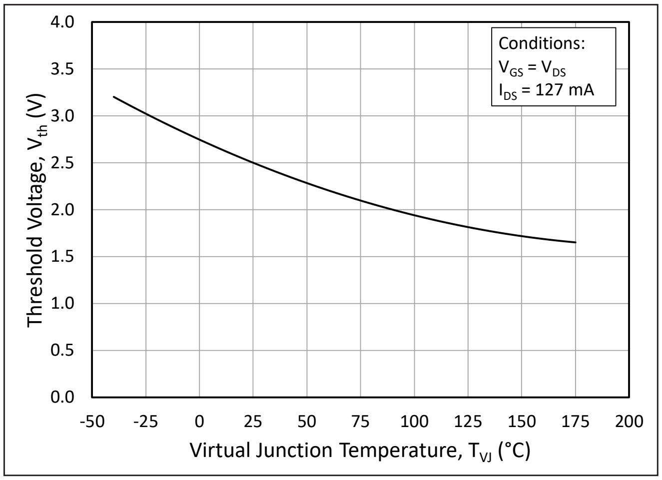


Figure 10. Threshold Voltage vs. Junction Temperature

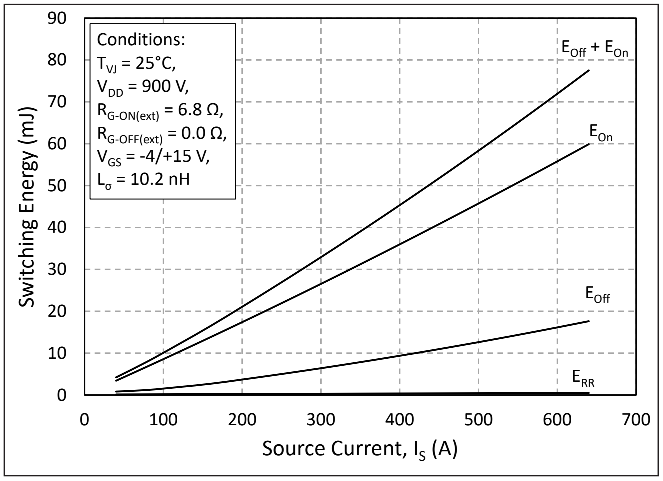


Figure 11. Switching Energy vs. Drain Current (V_{DD} = 900 V)

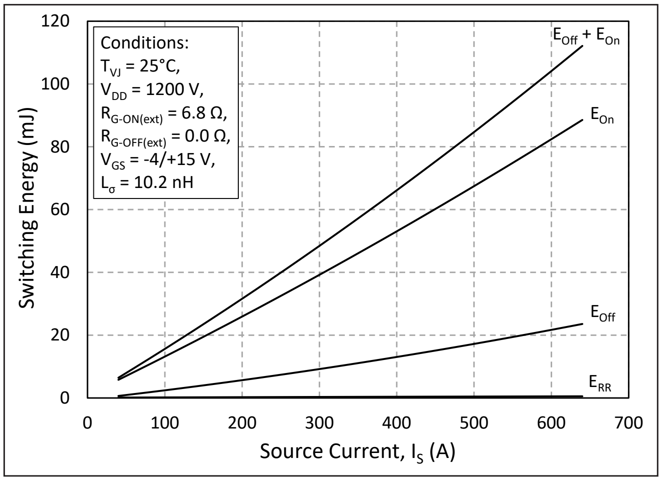


Figure 12. Switching Energy vs. Drain Current (V_{DD} = 1200 V)

Typical Performance

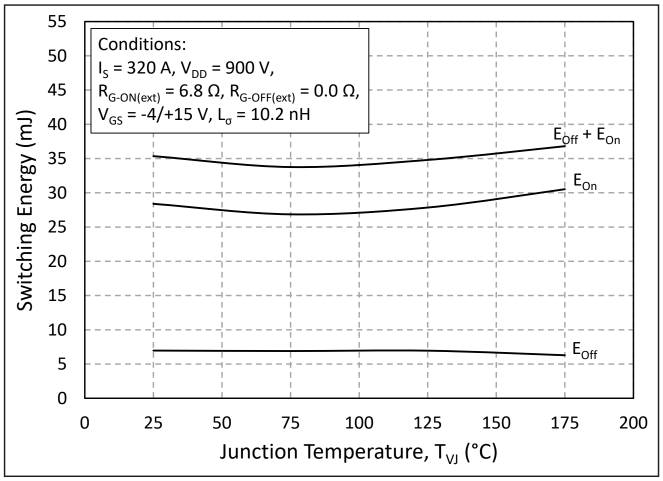


Figure 13. MOSFET Switching Energy vs. Junction Temperature

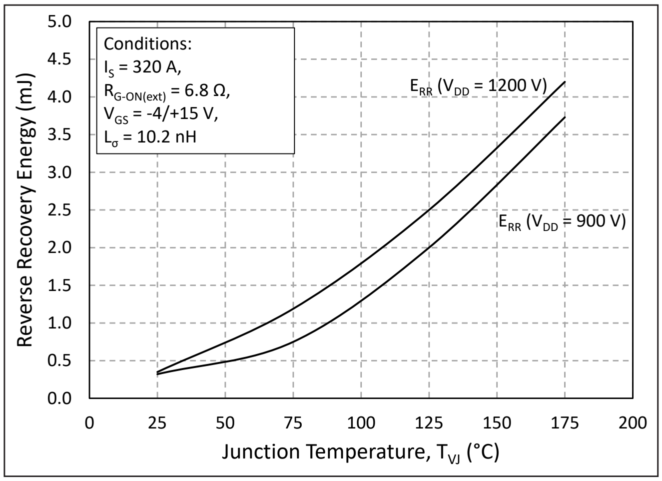


Figure 14. Reverse Recovery Energy vs. Junction Temperature

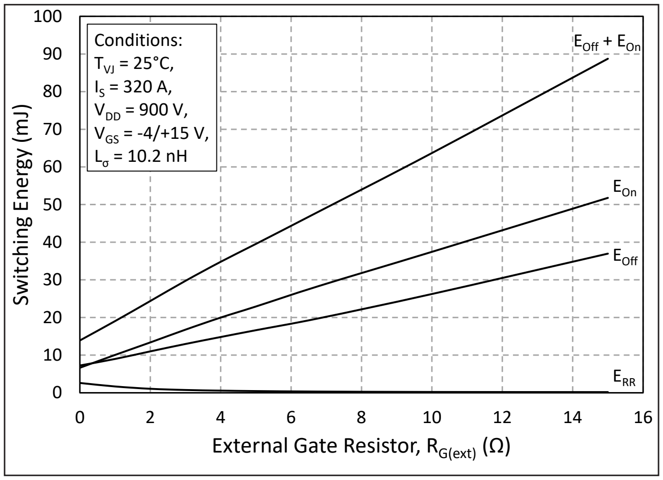


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

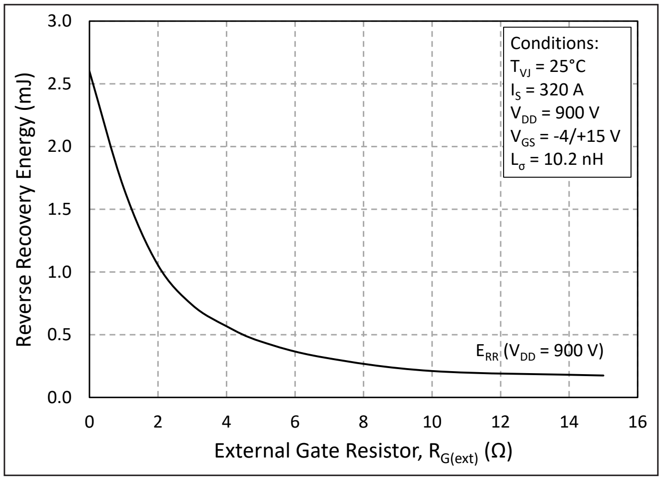


Figure 16. Reverse Recovery Energy vs. External Gate Resistance

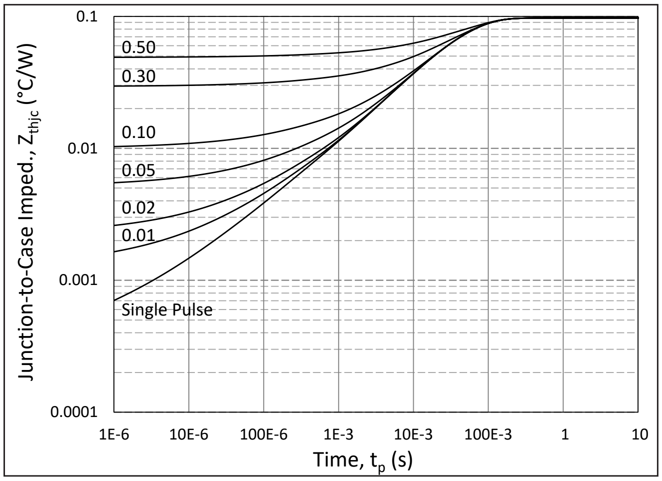


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, $Z_{th\ JC}$ (°C/W)

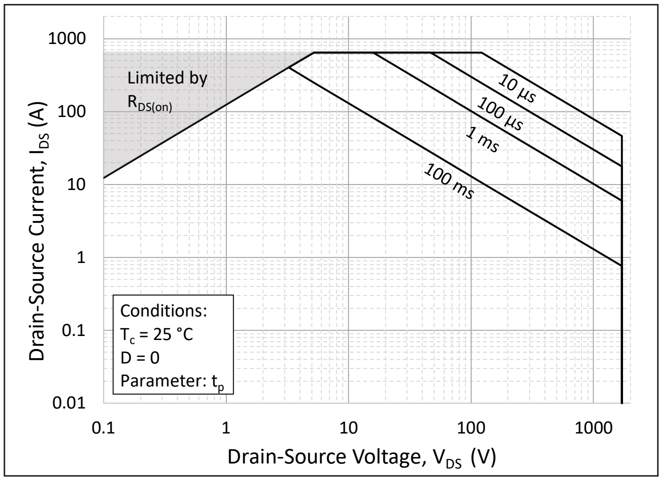


Figure 18. Forward Bias Safe Operating Area (FBSOA)

Typical Performance

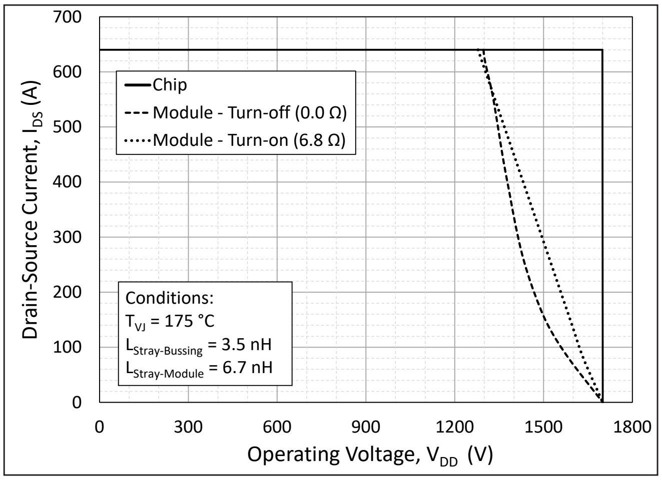


Figure 19. Switching Safe Operating Area

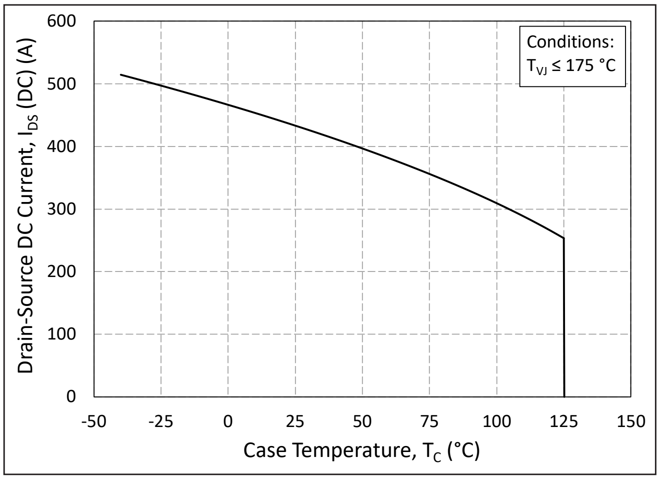


Figure 20. Continuous Drain Current Derating vs. Case Temperature

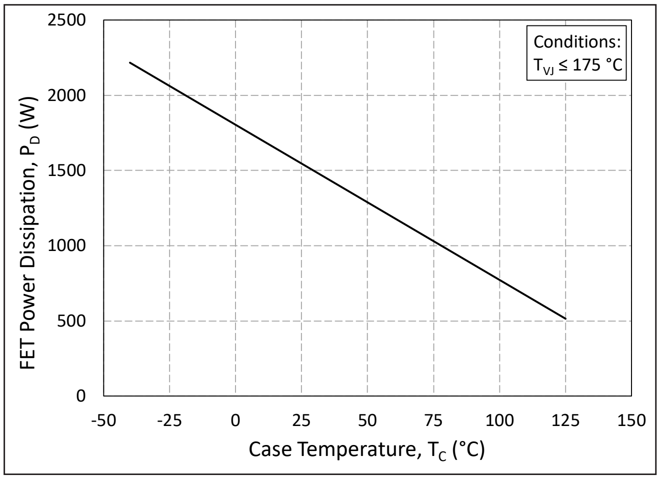


Figure 21. Maximum Power Dissipation Derating vs. Case Temperature

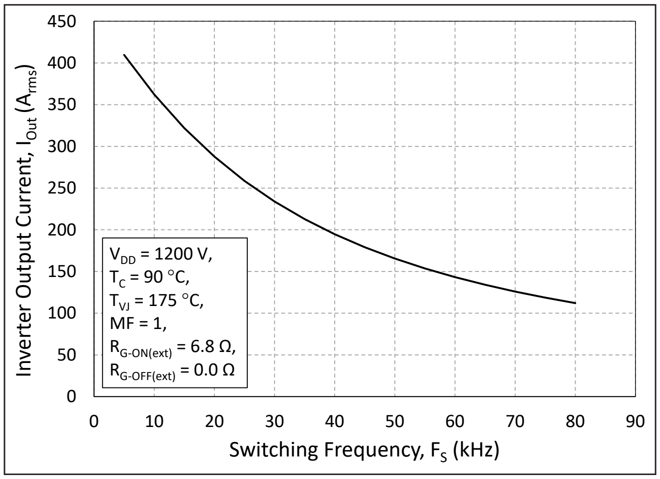


Figure 22. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

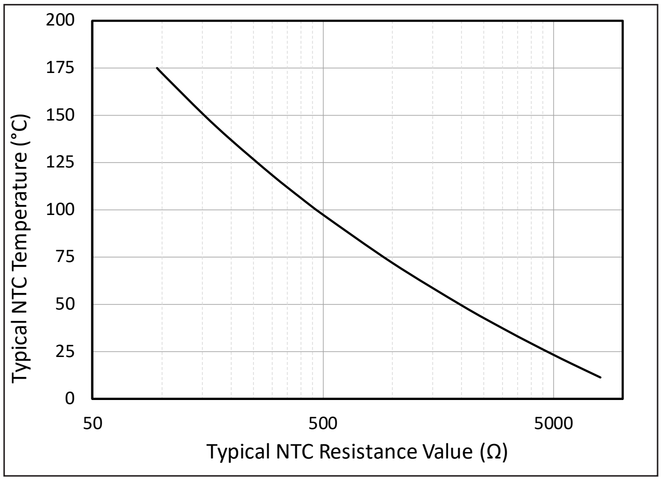


Figure 23. NTC Resistance vs. NTC Temperature

Timing Characteristics

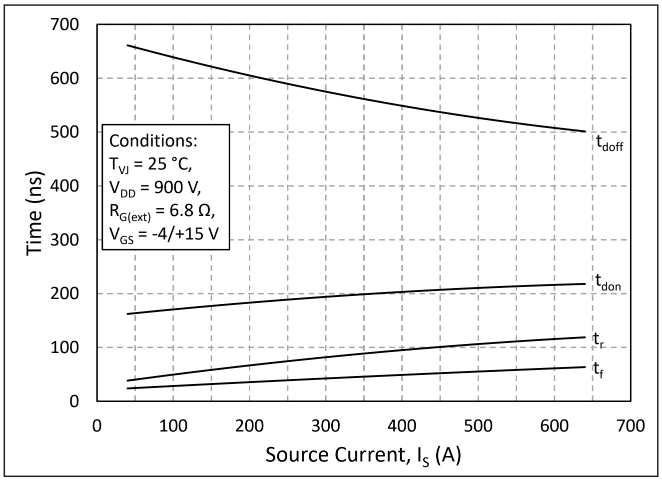


Figure 24. Timing vs. Source Current

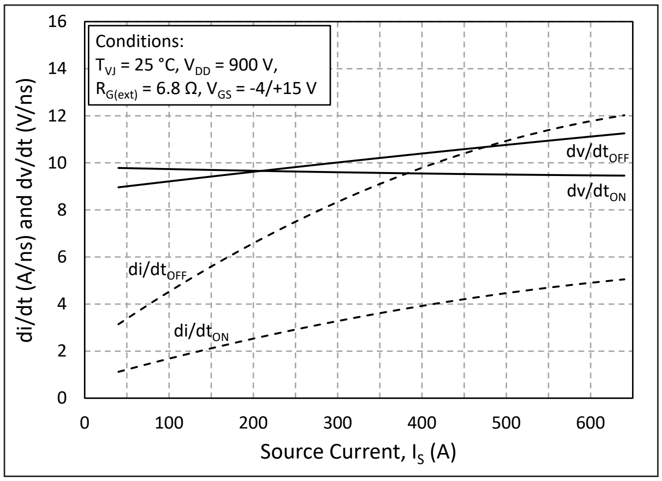


Figure 25. dv/dt and di/dt vs. Source Current

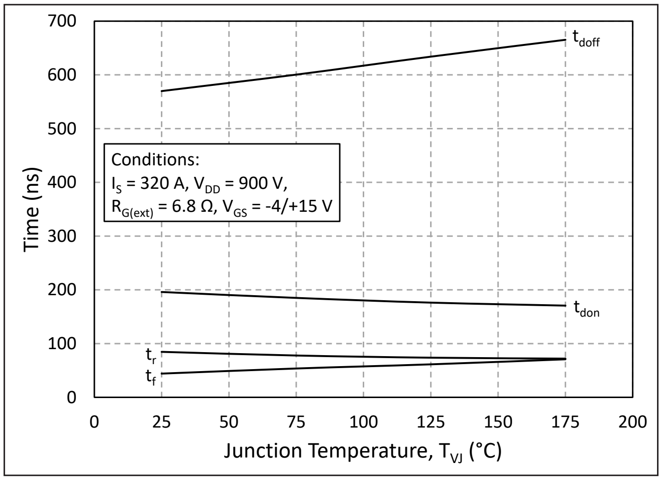


Figure 26. Timing vs. Junction Temperature

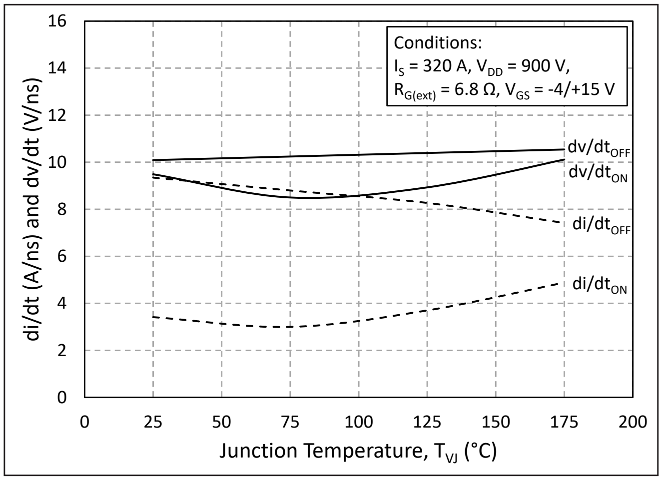


Figure 27. dv/dt and di/dt vs. Junction Temperature

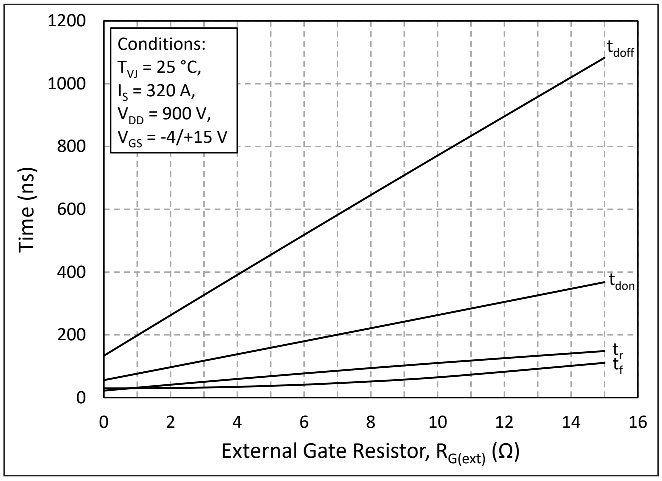


Figure 28. Timing vs. External Gate Resistance

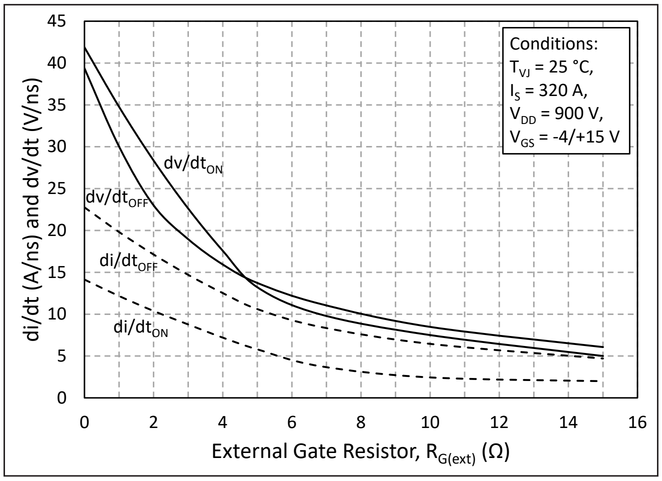


Figure 29. dv/dt and di/dt vs. External Gate Resistance

Definitions

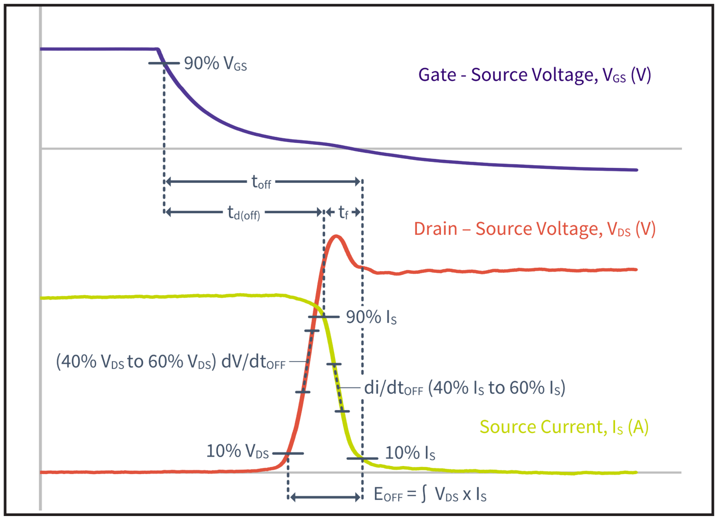


Figure 30. Turn-off Transient Definitions

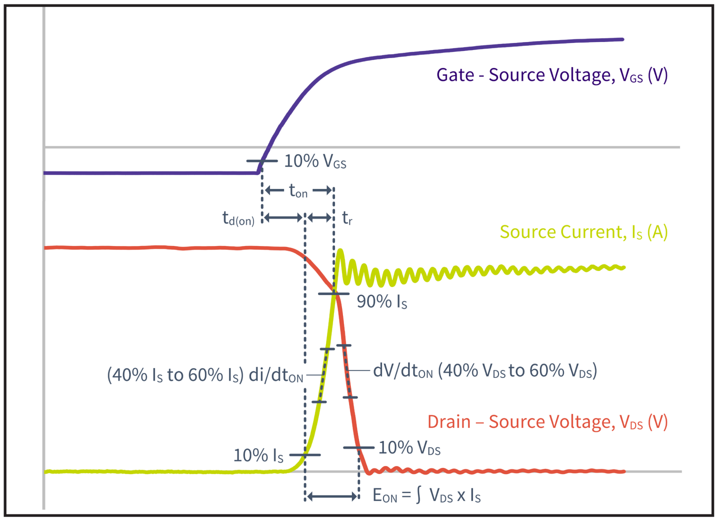


Figure 31. Turn-on Transient Definitions

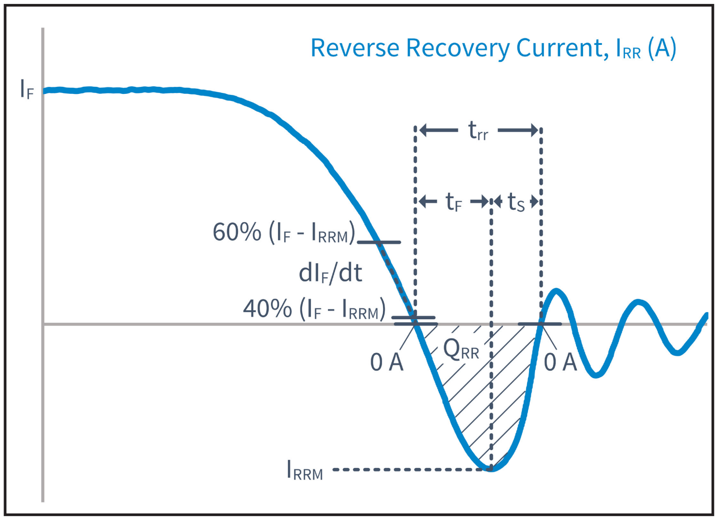


Figure 32. Reverse Recovery Definitions

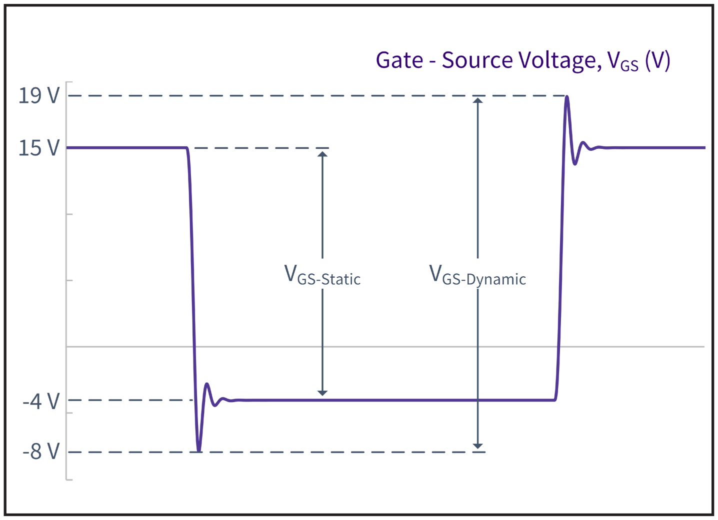
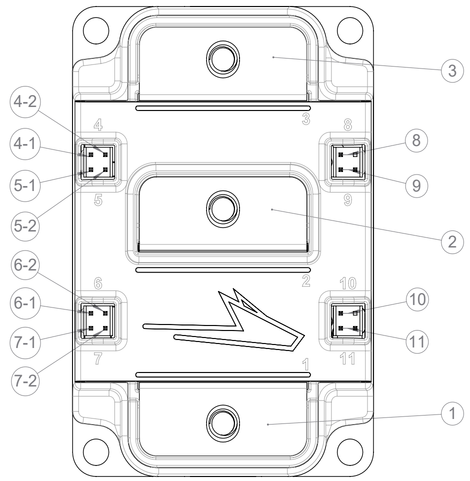
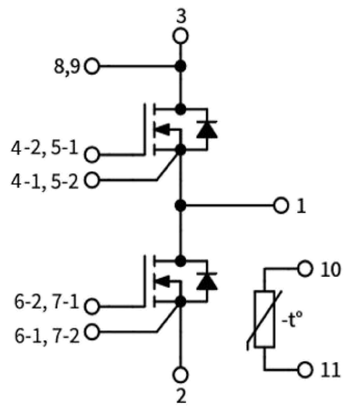


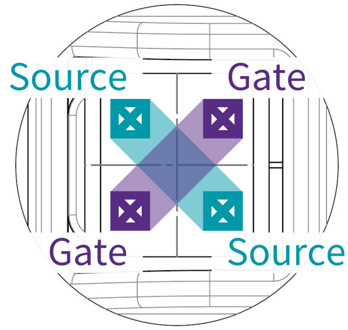
Figure 33. V_{GS} Transient Definitions

Schematic and Pinout

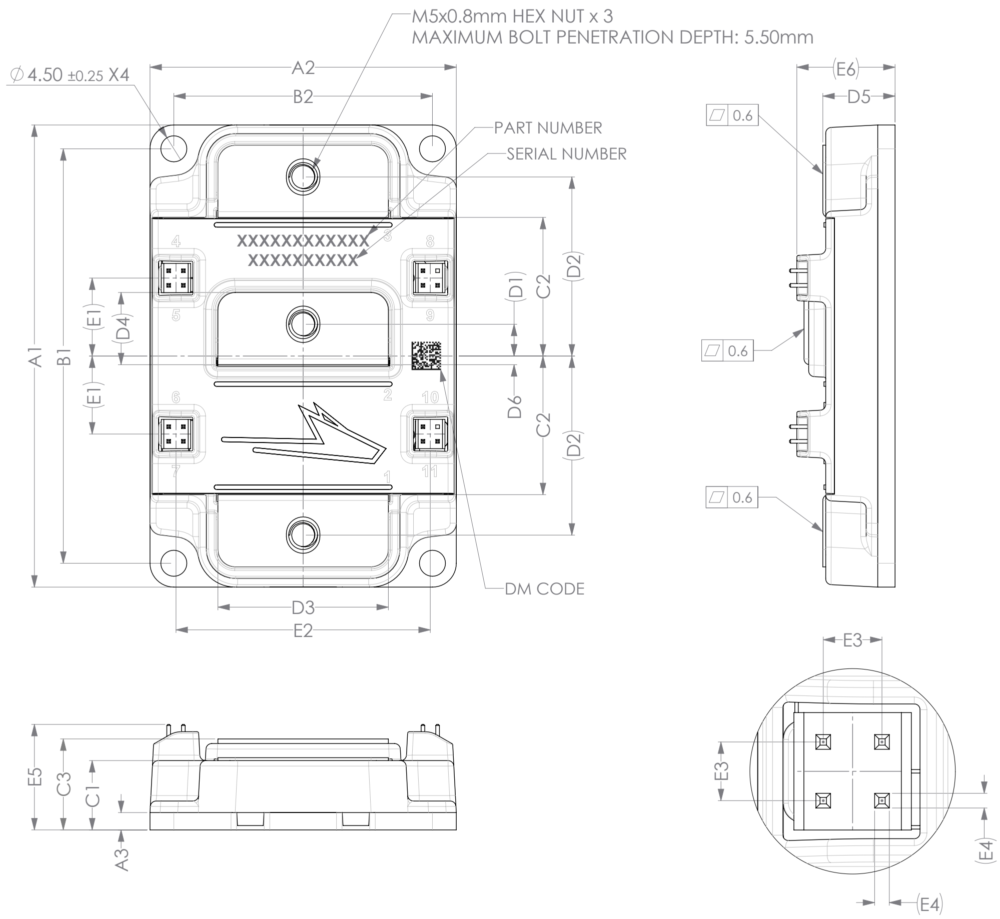




Zoom View of Signal Pinout

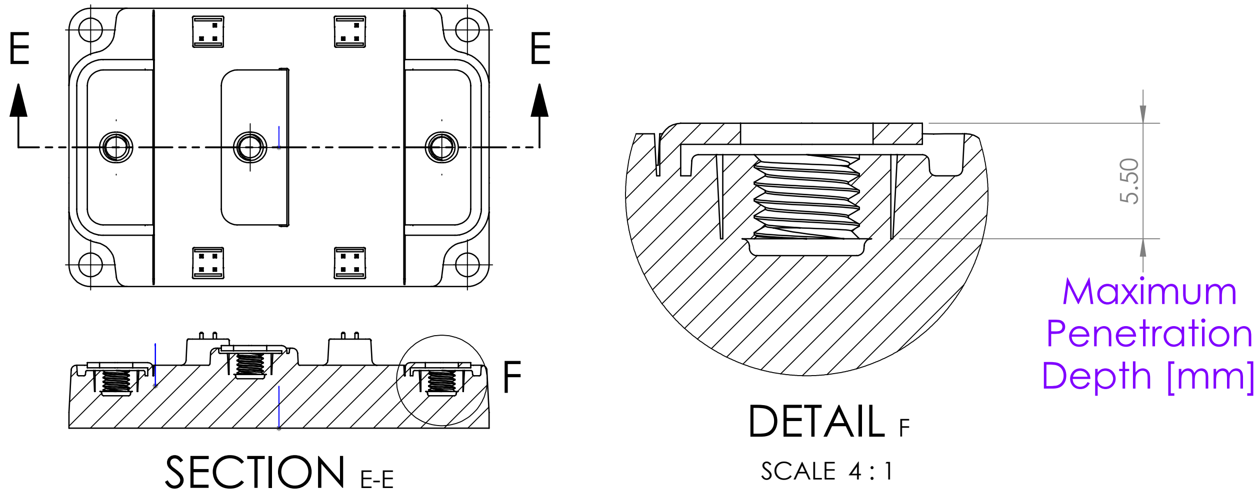


Package Dimension (mm)



DIMENSION TABLE		
SYMBOL	DIMENSION (mm)	TOLERANCE (mm)
A1	80.00	±0.30
A2	53.00	±0.30
A3	3.00	±0.30
B1	71.75	±0.30
B2	44.75	±0.30
C1	12.00	±0.50
C2	24.00	±0.50
C3	15.75	±0.40
D1	(5.50)	REF.
D2	(31.00)	REF.
D3	29.50	±0.30
D4	(12.50) TYP	REF.
D5	12.50	±0.30
D6	1.50	±0.30
E1	(13.50)	REF.
E2	44.00	±0.30
E3	2.54	±0.50
E4	(0.64)	REF.
E5	18.26	±0.30
E6	(17.00)	REF.

Package Dimensions (mm)



Supporting Links & Tools

Evaluation Tools & Support

- All SiC Module PLECS Models
- All SiC Module LTspice Models
- KIT-CRD-CIL17N-XM: Dynamic Performance Evaluation Board for the XM3 Module
- SpeedFit 2.0 Design Simulator™
- Technical Support Forum

Dual-Channel Gate Driver Board

- CGD1700HB2P-XM3: Dual Channel Differential Isolated Half Bridge Gate Driver Board
- Si828x Gate Driver Boards for Wolfspeed XM3 Modules
- CGD12HB00D: Differential Transceiver Daughter Board Companion Tool for Differential Gate Drivers

Application Notes

- XM Module Signal Pinout Clarification Guide
- XM3 Mounting Guide
- XM3 Thermal Interface Material Guide
- Thermal Characterization Methods and Applications
- PRD-06832: Design Options for Wolfspeed® Silicon Carbide MOSFET Gate Bias Power Supplies

Notes & Disclaimers

WOLFSPEED PROVIDES TECHNICAL AND RELIABILITY DATA, DESIGN RESOURCES, APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, WITH RESPECT THERETO, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, SUITABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

This document and the information contained herein are subject to change without notice. Any such change shall be evidenced by the publication of an updated version of this document by Wolfspeed. No communication from any employee or agent of Wolfspeed or any third party shall effect an amendment or modification of this document. No responsibility is assumed by Wolfspeed for any infringement of patents or other rights of third parties which may result from use of the information contained herein. No license is granted by implication or otherwise under any patent or patent rights of Wolfspeed.

The information contained in this document (excluding examples, as well as figures or values that are labeled as “typical”) constitutes Wolfspeed’s sole published specifications for the subject product. “Typical” parameters are the average values expected by Wolfspeed in large quantities and are provided for informational purposes only. Any examples provided herein have not been produced under conditions intended to replicate any specific end use. Product performance can and does vary due to a number of factors.

This product has not been designed or tested for use in, and is not intended for use in, any application in which failure of the product would reasonably be expected to cause death, personal injury, or property damage. For purposes of (but without limiting) the foregoing, this product is not designed, intended, or authorized for use as a critical component in equipment implanted into the human body, life-support machines, cardiac defibrillators, and similar emergency medical equipment; air traffic control systems; or equipment used in the planning, construction, maintenance, or operation of nuclear facilities. Notwithstanding any application-specific information, guidance, assistance, or support that Wolfspeed may provide, the buyer of this product is solely responsible for determining the suitability of this product for the buyer’s purposes, including without limitation (1) selecting the appropriate Wolfspeed products for the buyer’s application, (2) designing, validating, and testing the buyer’s application, and (3) ensuring the buyer’s application meets applicable standards and any other legal, regulatory, and safety-related requirements.

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Wolfspeed representative or from the Product Documentation sections of www.wolfspeed.com.

REACh Compliance

REACh substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact your Wolfspeed representative to ensure you get the most up-to-date REACh SVHC Declaration. REACh banned substance information (REACh Article 67) is also available upon request.

Contact info:
4600 Silicon Drive
Durham, NC 27703 USA
Tel: +1.919.313.5300
www.wolfspeed.com/power