

# 5V and 3.3V Supply Monitor, Watchdog Timer, Manual Reset, with Active High & Low Resets



## FEATURES

- **Selectable reset voltage tolerance**
  - CAT1232LP for 5V supply
  - CAT1832 for 3.3V supply
- **Selectable watchdog period:**  
150ms, 600ms or 1.2 sec
- **Two reset outputs**
  - Active high, push-pull reset output
  - Active low, open-drain reset output (CAT1232LP)
  - Active low, push-pull reset output (CAT1832)
- **Debounced manual push-button reset**
- **Compact SOIC and MSOP packages**

## APPLICATIONS

- **Microprocessor Systems**
- **Portable Equipment**
- **Controllers**
- **Single Board Computers**
- **Instrumentations**
- **Telecommunications**

For Ordering Information details, see page 11.

## DESCRIPTION

The CAT1232LP and CAT1832 microprocessor supervisors can halt and restart a “hung-up” or “stalled” microprocessor, restart a microprocessor after a power failure, and debounce a manual/push-button microprocessor reset switch. The devices are drop in replacements for the Maxim/Dallas Semiconductor DS1232LP and DS1832 supervisors

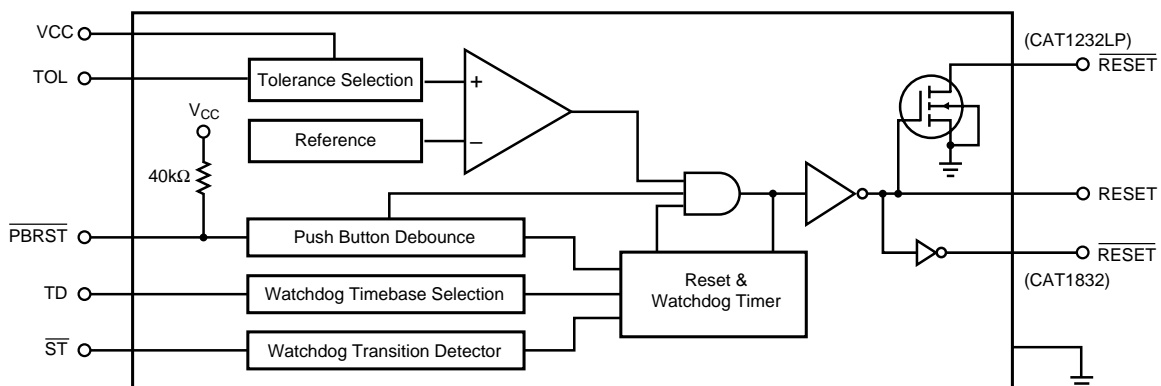
Precision reference and comparator circuits monitor the 5V or 3.3V system power supply voltage,  $V_{CC}$ . During power-up or when the power supply falls outside selectable tolerance limits, both the RESET and  $\overline{\text{RESET}}$  become active. After the power supply voltage rises above the RESET threshold voltage, the reset signals remain active for a minimum of 250ms, allowing the power supply and system processor to stabilize. The trip-point tolerance input, TOL, selects the trip level tolerance to be either 5% or 10% for the CAT1232LP 5V supply and 10% or 20% for the CAT1832 3.3V supply.

Each device has a push-pull, active HIGH reset output. The CAT1232LP also has an open drain, active LOW reset output while the CAT1832 also has a push-pull, active LOW reset output.

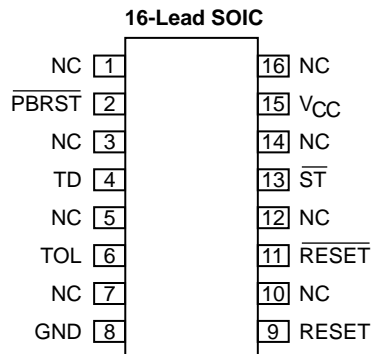
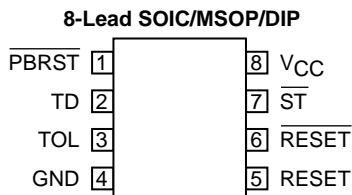
A debounced manual reset input activates the reset outputs and holds them active for a minimum period of 250ms after being released.

Also included is a watchdog timer to reset a microprocessor that has stopped due to a software or hardware failure. Three watchdog time-out periods are selectable: 150ms, 600ms and 1.2sec. If the  $\overline{\text{ST}}$  input is not strobed low before the watchdog time out period expires, the reset signals become active for a minimum of 250ms.

## FUNCTIONAL DIAGRAM



## PIN CONFIGURATION



## PIN DESCRIPTION

| Pin Number<br>8-Lead Package | Pin Number<br>16-Lead Package | Name  | Function   |
|------------------------------|-------------------------------|-------|--|
| 1                            | 2                             | PBRST | Debounced manual pushbutton reset input  |
| 2                            | 4                             | TD    | Watchdog typical time delay selection:<br>a) $t_{TD} = 150\text{ms}$ for TD = GND<br>b) $t_{TD} = 600\text{ms}$ for TD = Open<br>c) $t_{TD} = 1200\text{ms}$ for TD = VCC  |
| 3                            | 6                             | TOL   | CAT1232LP TOL selects 5% (TOL = GND) or 10% (TOL = VCC) trip point tolerance. CAT1832 TOL selects 10% (TOL = GND) or 20% TOL = VCC) trip point tolerance.  |
| 4                            | 8                             | GND   | Ground   |
| 5                            | 9                             | RESET | Active HIGH reset output. RESET is active<br>1. If VCC falls below the reset voltage trip point<br>2. If PBRST is low<br>3. If ST is not strobed low before the timeout period set by TD expires.<br>4. During power-up. |
| 6                            | 11                            | RESET | Active LOW reset output. (See RESET)   |
| 7                            | 13                            | ST    | Strobe Input   |
| 8                            | 15                            | VCC   | Power Supply   |
|                              | 1, 3, 5, 7, 10, 12, 14, 16    | NC    | No internal connection   |

## ABSOLUTE MAXIMUM RATINGS\*

|   |                          |   |                 |
|---|--------------------------|---|-----------------|
| Voltage on $V_{CC}$ .....   | -0.5V to 7.0V            | Maximum Junction Temperature .....        | 125°C           |
| Voltage on $\overline{ST}$ and TD .....                               | -0.5V to $V_{CC} + 0.5V$ | Storage Temperature Range .....           | -65°C to +150°C |
| Voltage on $\overline{PBRST}$ , $\overline{RESET}$<br>and RESET ..... | -0.5V to $V_{CC} + 0.5V$ | Lead Soldering Temperature (10 sec) ..... | 300°C           |
|   |                          | Operating Temperature Range .....         | -40°C to +85°C  |

## ELECTRICAL CHARACTERISTICS

Unless otherwise stated,  $1.0V \leq V_{CC} \leq 5.5V$  and over the operating temperature range of -40°C to +85°C. All voltages are referenced to ground.

| Symbol     | Parameter   | Conditions                   | Min             | Typ             | Max             | Units      |
|------------|---|------------------------------|-----------------|-----------------|-----------------|------------|
| $V_{CC}$   | Supply Voltage  |                              | 1.0             |                 | 5.5             | V          |
| $I_{CC1}$  | Supply Current  | $V_{CC} = 5.5V$ , CAT1232LP  |                 | 35              | 50              | $\mu A$    |
|            |   | $V_{CC} = 3.6V$ , CAT1832    |                 | 20              | 35              |            |
| $V_{IH}$   | $\overline{ST}$ and $\overline{PBRST}$ Input High Level                           | (5)                          | 2               |                 | $V_{CC} + 0.3V$ | V          |
|            |   | (6)                          | $V_{CC} - 0.4V$ |                 |                 |            |
| $V_{IL}$   | $\overline{ST}$ and $\overline{PBRST}$ Input Low Level                            | $V_{CC} = 5.5V$ , CAT1232LP  | - 0.3           |                 | 0.8             | V          |
|            |   | $V_{CC} = 3.6V$ , CAT1832    |                 |                 | 0.5             |            |
| $V_{CCTP}$ | $V_{CC}$ Trip Point (TOL = GND)   | CAT1232LP                    | 4.50            | 4.62            | 4.74            | V          |
| $V_{CCTP}$ | $V_{CC}$ Trip Point (TOL = $V_{CC}$ )   | CAT1232LP                    | 4.25            | 4.37            | 4.49            | V          |
| $V_{CCTP}$ | $V_{CC}$ Trip Point (TOL = GND)   | CAT1832                      | 2.80            | 2.88            | 2.97            | V          |
| $V_{CCTP}$ | $V_{CC}$ Trip Point (TOL = $V_{CC}$ )   | CAT1832                      | 2.47            | 2.55            | 2.64            | V          |
| $t_{TD}$   | Watchdog Time-Out Period  | TD = GND                     | 62.5            | 150             | 250             | ms         |
| $t_{TD}$   | Watchdog Time-Out Period  | TD = $V_{CC}$                | 500             | 1200            | 2000            | ms         |
| $t_{TD}$   | Watchdog Time-Out Period  | TD floating                  | 250             | 600             | 1000            | ms         |
| $V_{OH}$   | Output Voltage  | $I = - 500\mu A^{(3)}$       | $V_{CC} - 0.5V$ | $V_{CC} - 0.1V$ |                 | V          |
| $I_{OH}$   | Output Current  | Output = 2.4V <sup>(2)</sup> |                 | - 350           |                 | $\mu A$    |
| $I_{OL}$   | Output Current  | Output = 0.4V,               | 10              |                 |                 | mA         |
| $I_{IL}$   | Input Leakage   | (1)                          | - 1.0           |                 | 1.0             | $\mu A$    |
| $R_{PU}$   | Internal Pull-Up Resistor   | (1)                          | 32              | 40              | 55              | k $\Omega$ |
| $C_{IN}$   | Input Capacitance   |                              |                 |                 | 5               | pF         |
| $C_{OUT}$  | Output Capacitance  |                              |                 |                 | 7               | pF         |
| $t_{PB}$   | $\overline{PBRST}$ Manual Reset Minimum Low Time                                  | $\overline{PBRST} = V_{IL}$  | 20              |                 |                 | ms         |
| $t_{RST}$  | Reset Active Time   |                              | 250             | 600             | 1000            | ms         |
| $t_{ST}$   | $\overline{ST}$ Pulse Width   | (4)                          | 20              |                 |                 | ns         |
| $t_{RPD}$  | $V_{CC}$ Fail Detect to $\overline{RESET}$ or $\overline{RESET}$                  |                              |                 | 5               | 8               | $\mu s$    |
| $t_F$      | $V_{CC}$ Slew Rate  |                              | 20              |                 |                 | $\mu s$    |
| $t_{PDLY}$ | $\overline{PBRST}$ Stable LOW to $\overline{RESET}$ and $\overline{RESET}$ Active |                              |                 |                 | 20              | ms         |
| $t_{RPU}$  | $V_{CC}$ Detect to $\overline{RESET}$ or $\overline{RESET}$ Inactive              | $t_{RISE} = 5\mu s$          | 250             | 600             | 1000            | ms         |
| $t_R$      | $V_{CC}$ Slew Rate  | 4.25V to 4.75V               | 0               |                 |                 | ns         |

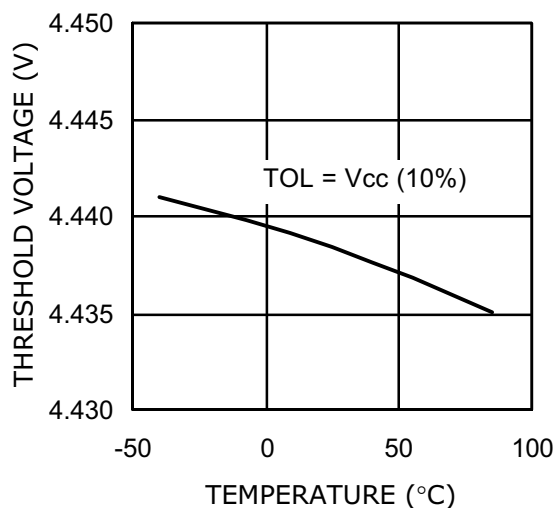
### Notes:

- |   |  |
|---|--|
| (1) $\overline{PBRST}$ is internally pulled HIGH to $V_{CC}$ through a nominal 40k $\Omega$ resistor ( $R_{PU}$ ).  | (4) Must not exceed the minimum watchdog time-out period ( $t_{TD}$ ). The watchdog circuit cannot be disabled. To avoid a reset, $\overline{ST}$ must be strobed. |
| (2) $\overline{RESET}$ is an open drain output on the CAT1232LP.  | (5) Measured with $V_{CC} \geq 2.7V$ .   |
| (3) $\overline{RESET}$ remains within 0.5V of $V_{CC}$ on power-down until $V_{CC}$ falls below 2V. $\overline{RESET}$ remains within 0.5V of ground on power-down until $V_{CC}$ falls below 2.0V. | (6) Measured with $V_{CC} < 2.7V$ .  |

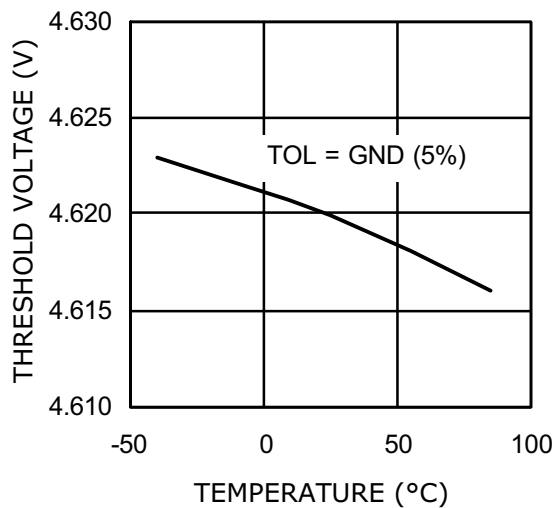
### TYPICAL CHARACTERISTICS

For the CAT1232LP,  $V_{CC} = 5V$  and  $T_{AMB} = 25^{\circ}C$  unless otherwise stated.

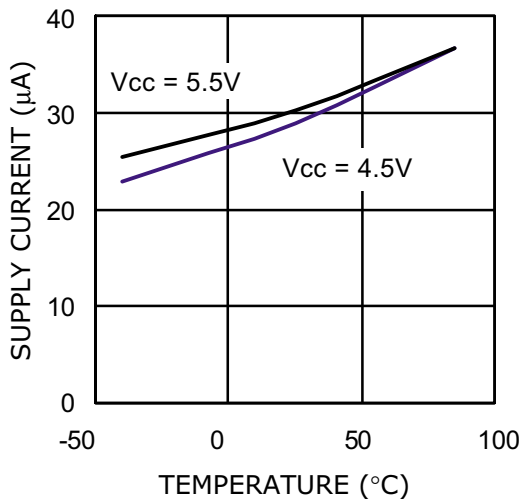
**Threshold Voltage vs. Temperature (10% TOL)**



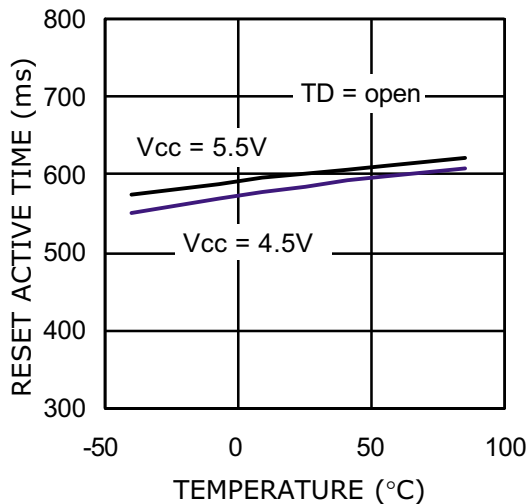
**Threshold Voltage vs. Temperature (5% TOL)**



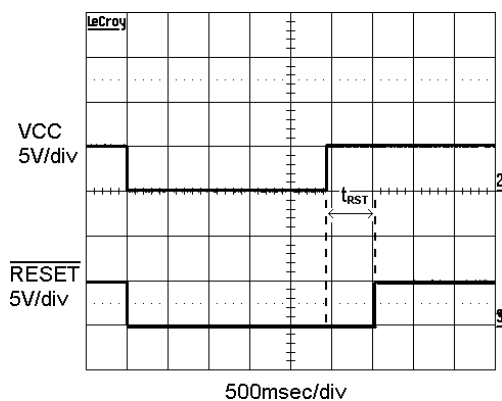
**Supply Current vs. Temperature**



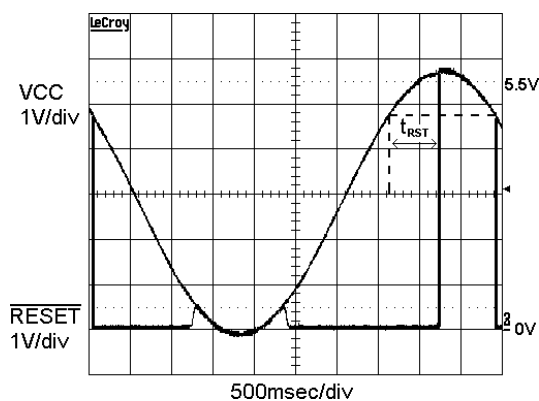
**Reset Active Time vs. Temperature**



**Reset Active Time Waveform**



**Transient Response**



## APPLICATION INFORMATION

### SUPPLY VOLTAGE MONITOR

#### Reset Signal Polarity and Output Stage Structure

$\overline{\text{RESET}}$  is an active LOW signal. It is developed with an open drain driver in the CAT1232LP. A pull-up resistor is required, typical values are 10k $\Omega$  to 50k $\Omega$ . The CAT1832 uses a CMOS push-pull output stage for the  $\overline{\text{RESET}}$ .

$\overline{\text{RESET}}$  is an active High signal developed by a CMOS push-pull output stage and is the logical opposite to  $\overline{\text{RESET}}$ .

#### Trip Point Tolerance Selection

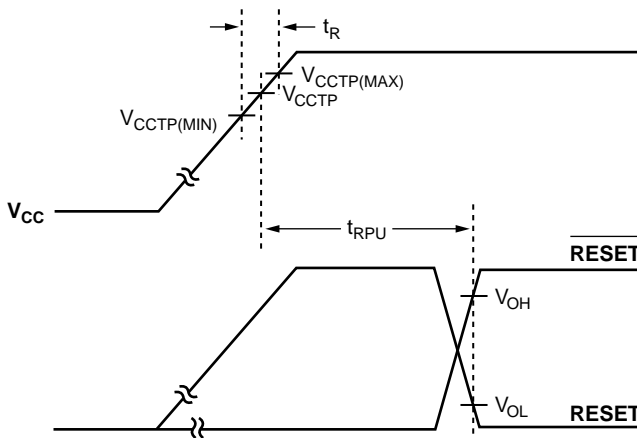
The TOL input is used to select the  $V_{CC}$  trip point threshold. This selection is made connecting the TOL input to ground or  $V_{CC}$ . Connecting TOL to Ground makes the  $V_{CC}$  trip threshold 4.62V for the CAT1232LP and 2.88V for the CAT1832.

Connecting TOL to  $V_{CC}$  makes the  $V_{CC}$  trip threshold 4.37V for the CAT1232LP and 2.55V for the CAT1832.

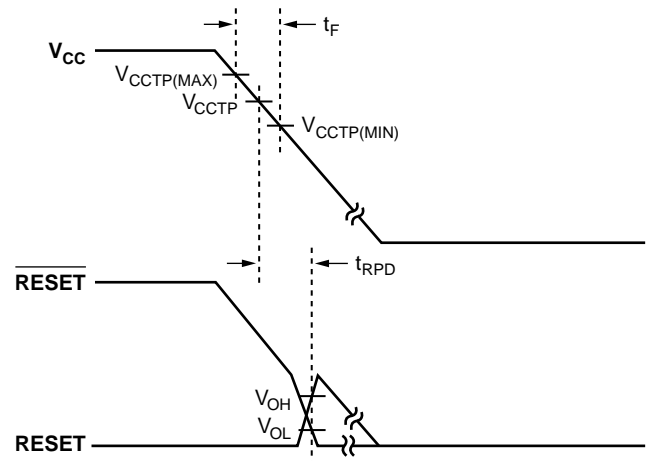
After  $V_{CC}$  has risen above the trip point set by TOL,  $\overline{\text{RESET}}$  and  $\overline{\text{RESET}}$  remain active for a minimum time period of 250ms.

On power-down, once  $V_{CC}$  falls below the reset threshold the  $\overline{\text{RESET}}$  outputs will remain active and are guaranteed valid down to a  $V_{CC}$  level of 1.0V.

| Tolerance Select Voltage    | Trip Point Tolerance | Trip Point Voltage (V) |         |      |
|-----------------------------|----------------------|------------------------|---------|------|
|                             |                      | MIN                    | NOMINAL | MAX  |
| CAT1232LP<br>TOL = $V_{CC}$ | 10 %                 | 4.25                   | 4.37    | 4.49 |
| CAT1232LP<br>TOL = GND      | 5 %                  | 4.50                   | 4.62    | 4.74 |
| CAT1832<br>TOL = $V_{CC}$   | 20 %                 | 2.47                   | 2.55    | 2.64 |
| CAT1832<br>TOL = GND        | 10 %                 | 2.80                   | 2.88    | 2.97 |



**Figure 1. Timing Diagram: Power Up**



**Figure 2. Timing Diagram: Power Down**

#### Manual Reset Operation

Push-button input,  $\overline{\text{PBRST}}$ , allows the user to issue reset signals. The pushbutton input is debounced and is pulled high through an internal 40k $\Omega$  resistor.

When  $\overline{\text{PBRST}}$  is held low for the minimum time of 20 ms, both resets become active and remain active for a minimum time period of 250ms after  $\overline{\text{PBRST}}$  returns high.

No external pull-up resistor is required, since  $\overline{\text{PBRST}}$  is pulled high by an internal 40k $\Omega$  resistor.

$\overline{\text{PBRST}}$  can be driven from a TTL or CMOS logic line or short-ed to ground with a mechanical switch.

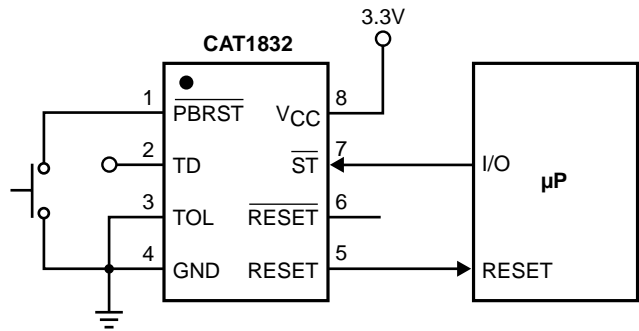
**WATCHDOG TIMER AND  $\overline{ST}$  INPUT**

A watchdog timer stops and restarts a microprocessor that has stopped proper operation or become "hung". The watchdog performs this function by monitoring the  $\overline{ST}$  input. After the reset outputs go inactive the  $\overline{ST}$  input must be strobed with a high-to-low signal transition prior to the minimum watchdog timeout period. However if the  $\overline{ST}$  input is not strobed with a high-to-low signal transition prior to a watchdog timeout the reset outputs will become active for  $T_{RST}$  resetting and restarting the microprocessor. Once the resets return to the inactive state the watchdog timer restarts the process.

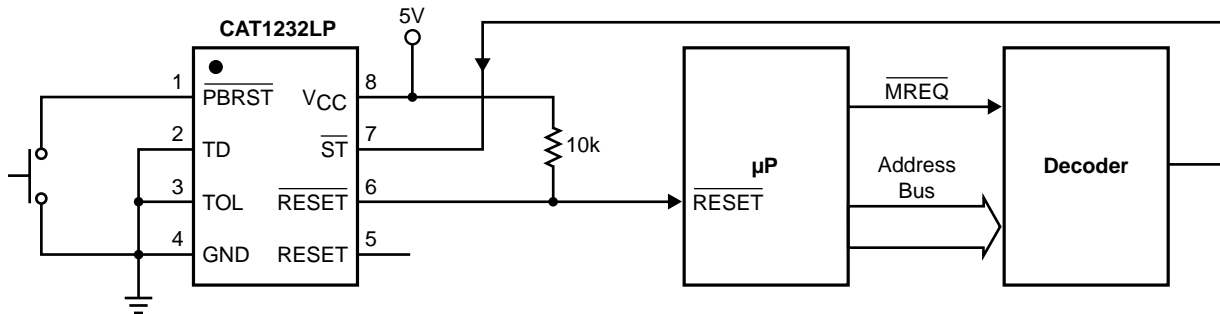
The TD input allows the user to select from three predetermined watchdog timeout periods. Always use the minimum timeout period to determine the required frequency of  $\overline{ST}$  high-to-low transitions and the maximum to determine the time prior to the reset outputs becoming active.  $\overline{ST}$  pulse widths must be 20ns or greater.

The watchdog timer cannot be disabled. It must be strobed with a high-to-low signal transition to avoid a watchdog timeout and subsequent reset.

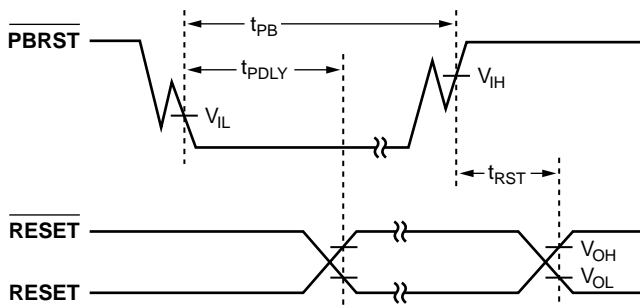
| TD Voltage Level | Watchdog Time-out Period (ms) |         |      |
|------------------|-------------------------------|---------|------|
|                  | MIN                           | NOMINAL | MAX  |
| GND              | 62.5                          | 150     | 250  |
| Floating         | 250                           | 600     | 1000 |
| V <sub>CC</sub>  | 500                           | 1200    | 2000 |



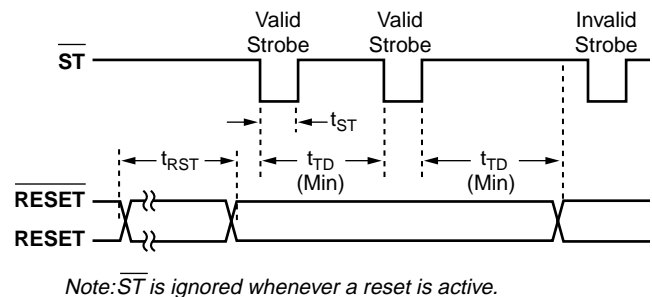
**Figure 4. CAT1832 Application Circuit: Pushbutton Reset**



**Figure 5. CAT1232LP Application Circuit: Watchdog Timer**

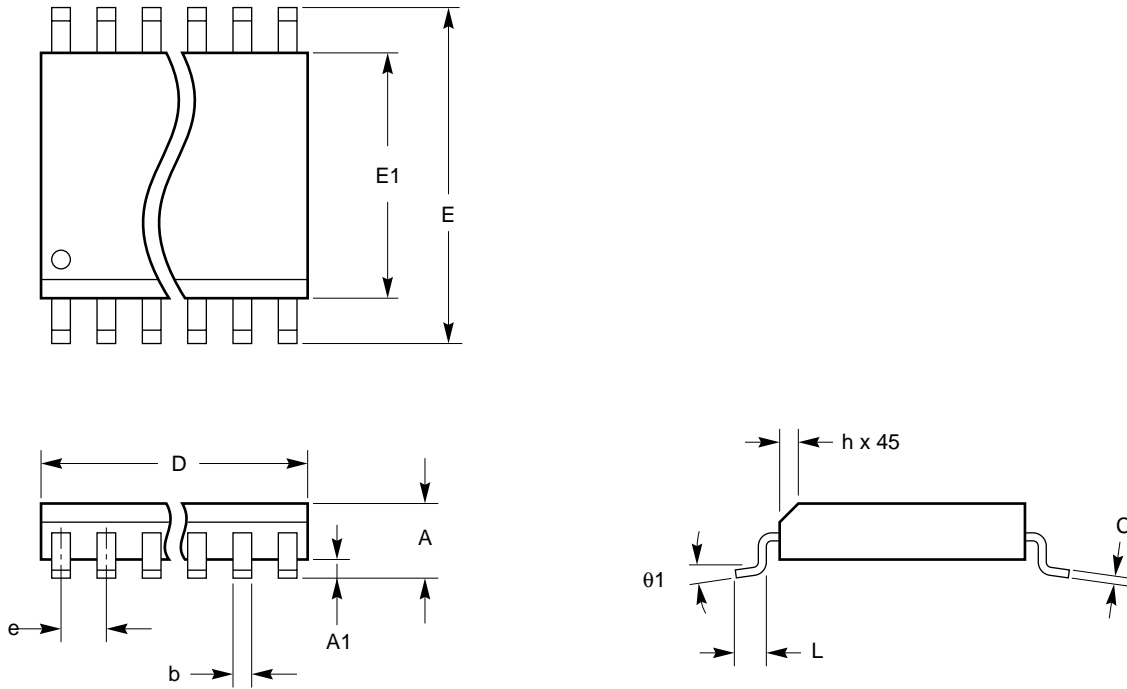


**Figure 6. Timing Diagram: Pushbutton Reset**



**Figure 7. Timing Diagram: Strobe Input**

**PACKAGE DRAWING**  
**16-LEAD WIDE BODY SOIC (300mil)**



| SYMBOL | MIN      | NOM   | MAX   |
|--------|----------|-------|-------|
| A1     | 0.10     |       | 0.30  |
| A      | 2.36     | 2.49  | 2.65  |
| b      | 0.33     | 0.41  | 0.51  |
| C      | 0.23     | 0.28  | 0.32  |
| D      | 10.10    | 10.31 | 10.50 |
| E      | 10.00    | 10.31 | 10.65 |
| E1     | 7.40     | 7.50  | 7.60  |
| e      | 1.27 BSC |       |       |
| h      | 0.25     |       | 0.75  |
| L      | 0.40     | 0.81  | 1.27  |
| θ1     | 0°       |       | 8°    |

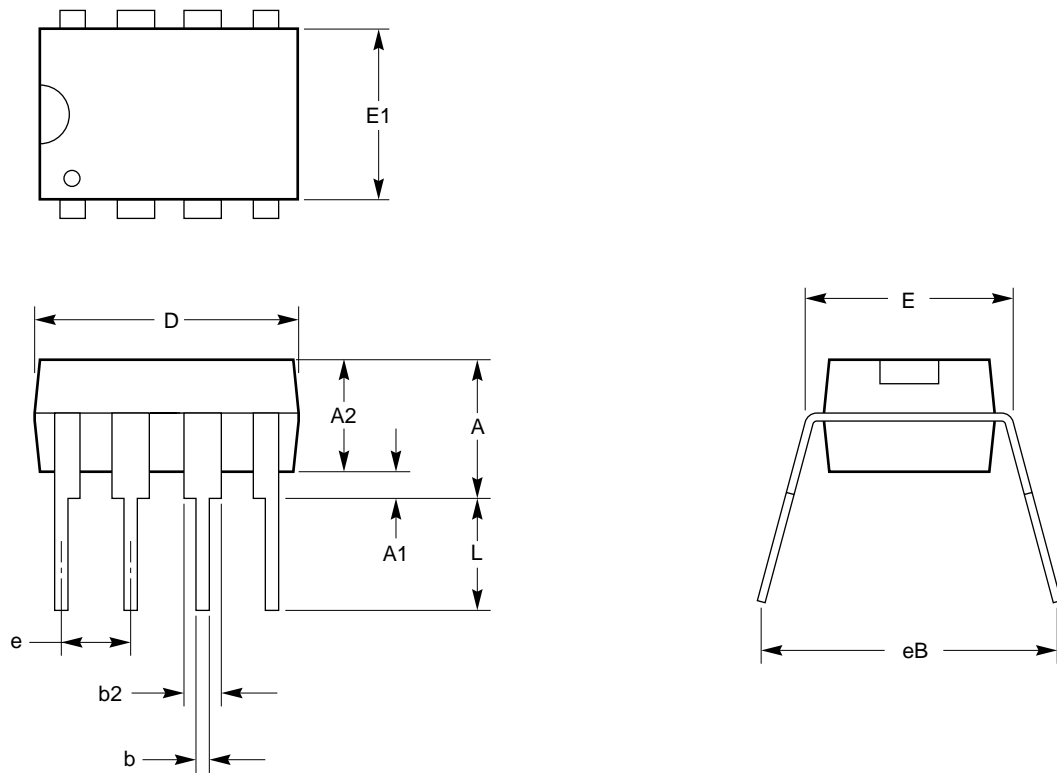
16-Lead\_SOIC\_(300mil).eps

**For current Tape and Reel information, download the PDF file from:  
<http://www.catsemi.com/documents/tapeandreeel.pdf>.**

**Notes:**

1. All dimensions are in millimeters.
2. Complies with JEDEC specification MS-013.

**PACKAGE DRAWING**  
**8-LEAD DIP (300mil)**



| SYMBOL | MIN      | NOM  | MAX   |
|--------|----------|------|-------|
| A      |          |      | 4.57  |
| A1     | 0.38     |      |       |
| A2     | 3.05     |      | 3.81  |
| b      | 0.36     | 0.46 | 0.56  |
| b2     | 1.14     |      | 1.52  |
| D      | 9.02     |      | 10.16 |
| E      | 7.62     | 7.87 | 8.26  |
| E1     | 6.17     | 6.35 | 7.49  |
| e      | 2.54 BSC |      |       |
| eB     | 7.87     |      | 9.65  |
| L      | 2.79     |      | 3.81  |

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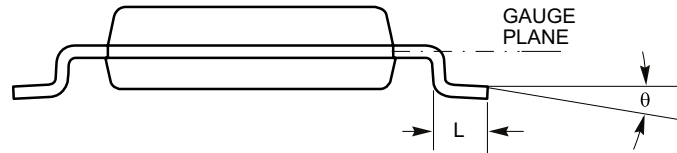
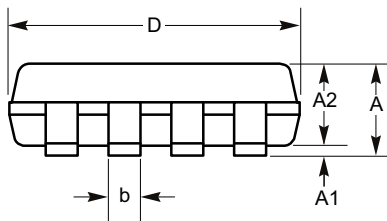
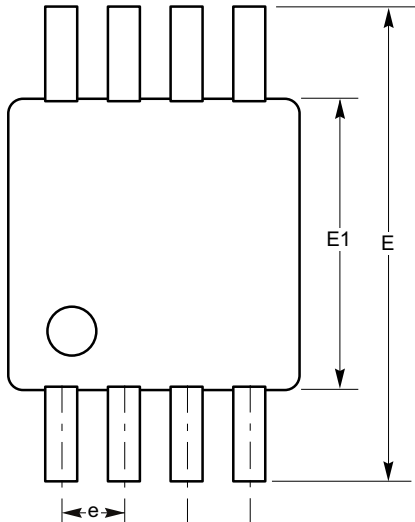
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<http://www.catsemi.com/documents/tapeandreel.pdf>

Notes:

1. All dimensions are in millimeters.
2. Complies with JEDEC Standard MS001.
3. Dimensioning and tolerancing per ANSI Y14.5M-1982



**PACKAGE DRAWING**  
**8-LEAD MSOP**



| SYMBOL   | MIN      | NOM  | MAX  |
|----------|----------|------|------|
| A        |          |      | 1.10 |
| A1       | 0.00     |      | 0.15 |
| A2       | 0.75     |      | 0.95 |
| b        | 0.22     |      | 0.38 |
| D        | 2.90     | 3.00 | 3.10 |
| E        | 4.80     | 4.90 | 5.00 |
| E1       | 2.90     | 3.00 | 3.10 |
| e        | 0.65 BSC |      |      |
| L        | 0.40     |      | 0.8  |
| $\theta$ | 0°       |      | 8°   |

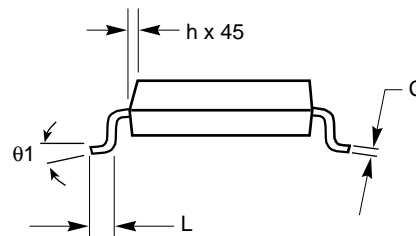
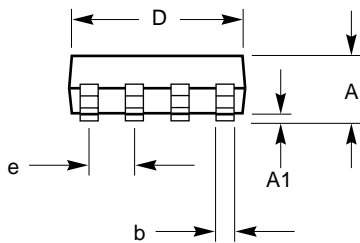
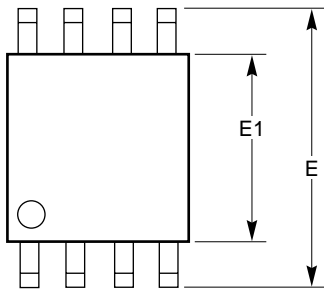
8-lead\_MSOP1.eps

**For current Tape and Reel information, download the PDF file from:**  
**<http://www.catsemi.com/documents/tapeandreeel.pdf>**

**Notes:**

1. All dimensions are in millimeters. Angles in degrees.
2. Complies with JEDEC Specification MO-187.
3. Stand off height/coplanarity are considered as special characteristics.

**PACKAGE MECHANICAL**  
**8-LEAD Narrow Body SOIC (150mil)**



| SYMBOL | MIN      | NOM | MAX  |
|--------|----------|-----|------|
| A1     | 0.10     |     | 0.25 |
| A      | 1.35     |     | 1.75 |
| b      | 0.33     |     | 0.51 |
| C      | 0.19     |     | 0.25 |
| D      | 4.80     |     | 5.00 |
| E      | 5.80     |     | 6.20 |
| E1     | 3.80     |     | 4.00 |
| e      | 1.27 BSC |     |      |
| h      | 0.25     |     | 0.50 |
| L      | 0.40     |     | 1.27 |
| θ1     | 0°       |     | 8°   |

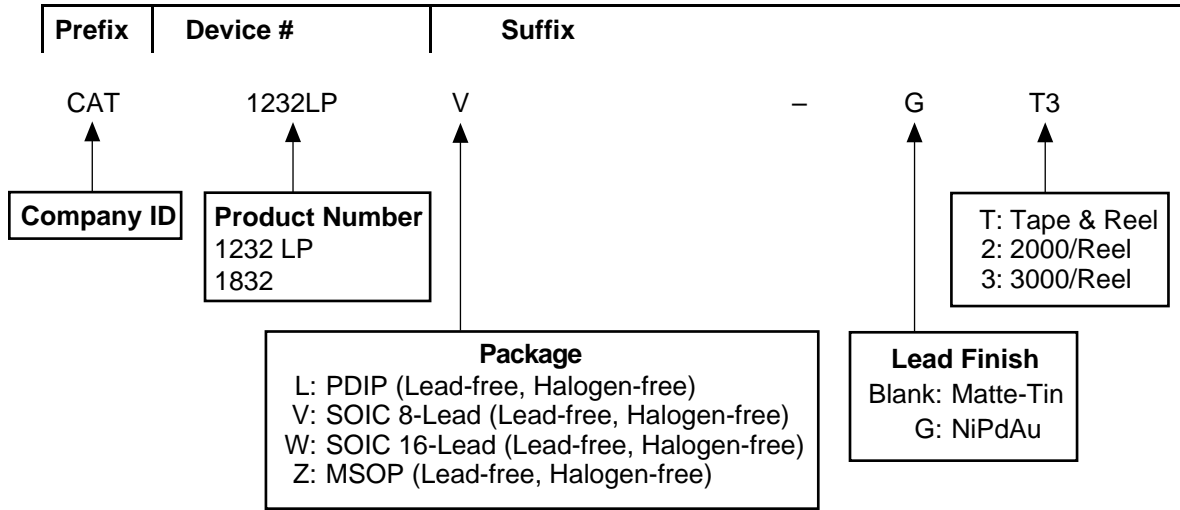
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**For current Tape and Reel information, download the PDF file from:**  
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Notes:

1. All dimensions are in millimeters. Angles in degrees.
2. Complies with JEDEC Specification MS-012.

**SAMPLE OF ORDERING INFORMATION**



Notes:

- (1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- (2) The standard lead finish is NiPdAu.
- (3) The device used in the above example is a CAT1232LPV-GT3 (SOIC, NiPdAu, Tape & Reel).
- (4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

| <b>Green NiPdAu Lead Finish</b> |               |                |                |                  |
|---------------------------------|---------------|----------------|----------------|------------------|
| Ordering Part Number            | Package       | Parts per Tube | Parts Per Reel | Reel Size (inch) |
| CAT1232LPL-G                    | 8-lead, DIP   | 50             | —              | —                |
| CAT1232LPV-GT3                  | 8-lead, SOIC  | —              | 3,000          | 13               |
| CAT1232LPZ-GT3                  | MSOP          | —              | 3,000          | 13               |
| CAT1232LPW-GT2                  | 16-lead, SOIC | —              | 2,000          | 13               |
|                                 |               |                |                |                  |
| CAT1832L-G                      | 8-lead, DIP   | 50             | —              | —                |
| CAT1832V-GT3                    | 8-lead, SOIC  | —              | 3,000          | 13               |
| CAT1832Z-GT3                    | MSOP          | —              | 3,000          | 13               |

## REVISION HISTORY

| Date       | Revision | Comments   |
|------------|----------|--|
| 06/13/2005 | 00       | Initial Issue  |
| 07/26/2005 | 0A       | Update Electrical Characteristics<br>Add Typical Characteristics                   |
| 03/27/2006 | 0B       | Update Document Title<br>Update Ordering Information                               |
| 08/21/2006 | 0C       | Add Ordering Information detail to page 1<br>Update Sample of Ordering Information |

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