Voltage Supervisor with I²C Serial CMOS EEPROM

HALOGEN FREE LEAD FREE™ RoHS Compliance

FEATURES

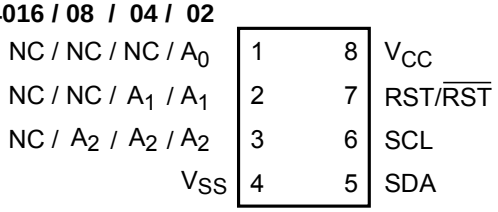
- **Precision Power Supply Voltage Monitor**
  - **5V, 3.3V, 3V & 2.5V systems**
  - **7 threshold voltage options**
- **Active High or Low Reset**
  - **Valid reset guaranteed at V_{CC} = 1 V**
- **Supports Standard and Fast I²C Protocol**
- **16-Byte Page Write Buffer**
- **Low power CMOS technology**
- **1,000,000 Program/Erase cycles**
- **100 year data retention**
- **Industrial temperature range**
- **RoHS-compliant 8-pin SOIC package**

For Ordering Information details, see page 14.

PIN CONFIGURATION

SOIC (W)

CAT14016 / 08 / 04 / 02



PIN FUNCTION

Pin Name	Function
A0, A1, A2	Device Address Inputs
SDA	Serial Data Input/Output
SCL	Serial Clock Input
RST/$\overline{RST}$	Reset Output
V_{CC}	Power Supply
V_{SS}	Ground
NC	No Connect

DESCRIPTION

The CAT140xx (see table below) are memory and supervisory solutions for microcontroller based systems. A CMOS serial EEPROM memory and a system power supervisor with brown-out protection are integrated together. Memory interface is via both the standard (100kHz) as well as fast (400kHz) I²C protocol.

The CAT140xx provides a precision V_{CC} sense circuit with two reset output options: CMOS active low output or CMOS active high. The RESET output is active whenever V_{CC} is below the reset threshold or falls below the reset threshold voltage.

The power supply monitor and reset circuit protect system controllers during power up/down and against brownout conditions. Seven reset threshold voltages support 5V, 3.3V, 3V and 2.5V systems. If power supply voltages are out of tolerance reset signals become active, preventing the system microcontroller, ASIC or peripherals from operating. Reset signals become inactive typically 240ms after the supply voltage exceeds the reset threshold level.

MEMORY SIZE SELECTOR

Product	Memory density
14002	2-Kbit
14004	4-Kbit
14008	8-Kbit
14016	16-Kbit

THRESHOLD SUFFIX SELECTOR

Nominal Threshold Voltage	Threshold Suffix Designation
4.63V	L
4.38V	M
4.00V	J
3.08V	T
2.93V	S
2.63V	R
2.32V	Z

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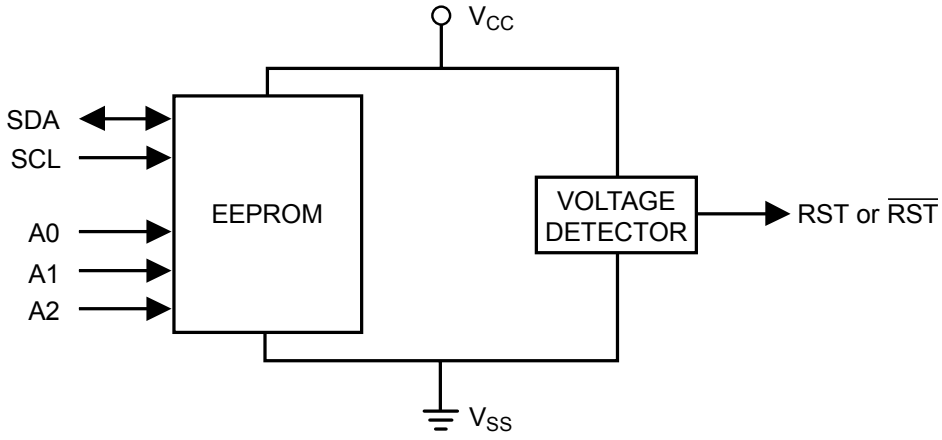
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground[2]	-0.5 to +6.5	V

RELIABILITY CHARACTERISTICS[3]

Symbol	Parameter	Min	Units
NEND[4]	Endurance	1,000,000	Program/ Erase Cycles
TDR	Data Retention	100	Years

D.C. OPERATING CHARACTERISTICS

V_{CC} = +2.5V to +5.5V unless otherwise specified.

Symbol	Parameter	Limits			Test Condition	Units
		Min.	Typ.	Max.		
I_{CC}	Supply Current			1	Read or Write at 400kHz	mA
I_{SB}	Standby Current		10	22	V_{CC} < 5.5V; All I/O Pins at V_{SS} or V_{CC}	µA
			8	17	V_{CC} < 3.6V; All I/O Pins at V_{SS} or V_{CC}	
I_L	I/O Pin Leakage			2	Pin at GND or V_{CC}	µA
V_{IL}	Input Low Voltage	-0.5		V_{CC} x 0.3		V
V_{IH}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 0.5		V
V_{OL}	Output Low Voltage SDA			0.4	$V_{CC} \geq$ 2.5 V, I_{OL} = 3.0 mA	V

Notes:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) The DC input voltage on any pin should not be lower than -0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than -1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

(3) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

(4) Page Mode, V_{CC} = 5 V, 25°C

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A.C. CHARACTERISTICS (MEMORY)[1]

V_{CC} = 2.5V to 5.5V, T_A = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Standard		Fast		Units
		Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		µs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		µs
t_{HIGH}	High Period of SCL Clock	4		0.6		µs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		µs
$t_{SU:DAT}$	Data In Setup Time	250		100		ns
t_R[2]	SDA and SCL Rise Time		1000		300	ns
t_F[2]	SDA and SCL Fall Time		300		300	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		µs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		µs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9	µs
t_{DH}	Data Out Hold Time	100		100		ns
T_i[2]	Noise Pulse Filtered at SCL and SDA Inputs		100		100	ns
t_{WR}	Write Cycle Time		5		5	ms
t_{PU}[2, 3]	Power-up to Ready Mode		1		1	ms

Notes:

(1) Test conditions according to “A.C. Test Conditions” table.

(2) Tested initially and after a design or process change that affects this parameter.

(3) t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

A.C. TEST CONDITIONS

Input Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Times	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Levels	0.5 x V_{CC}
Output Load	Current Source: I_{OL} = 3 mA; C_L = 100 pF

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ELECTRICAL CHARACTERISTICS (SUPERVISORY FUNCTION)

V_{CC} = Full range, T_A = -40ºC to +85ºC unless otherwise noted. Typical values at T_A = +25ºC and V_{CC} = 5V for L/M/J versions, V_{CC} = 3.3V for T/S versions, V_{CC} = 3V for R version and V_{CC} = 2.5V for Z version.

Symbol	Parameter	Threshold	Conditions	Min	Typ	Max	Units
V_{TH}	Reset Threshold Voltage	L	T_A = +25ºC	4.56	4.63	4.70	V
			T_A = -40ºC to +85ºC	4.50		4.75	
		M	T_A = +25ºC	4.31	4.38	4.45	
			T_A = -40ºC to +85ºC	4.25		4.50	
		J	T_A = +25ºC	3.93	4.00	4.06	
			T_A = -40ºC to +85ºC	3.89		4.10	
		T	T_A = +25ºC	3.04	3.08	3.11	
			T_A = -40ºC to +85ºC	3.00		3.15	
		S	T_A = +25ºC	2.89	2.93	2.96	
			T_A = -40ºC to +85ºC	2.85		3.00	
		R	T_A = +25ºC	2.59	2.63	2.66	
			T_A = -40ºC to +85ºC	2.55		2.70	
		Z	T_A = +25ºC	2.28	2.32	2.35	
			T_A = -40ºC to +85ºC	2.25		2.38	

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Units
	Reset Threshold Tempco			30		ppm/ºC
t_{RPD}	V_{CC} to Reset Delay[2]	V_{CC} = V_{TH} to (V_{TH} -100mV)		20		µs
t_{PURST}	Reset Active Timeout Period	T_A = -40ºC to +85ºC	140	240	460	ms
V_{OL}	$\overline{\text{RESET}}$ Output Voltage Low (Push-pull, active LOW, CAT140xx9)	V_{CC} = V_{TH} min, I_{SINK} = 1.2 mA R/S/T/Z			0.3	V
		V_{CC} = V_{TH} min, I_{SINK} = 3.2 mA J/L/M			0.4	
		V_{CC} > 1.0V, I_{SINK} = 50µA			0.3	
V_{OH}	$\overline{\text{RESET}}$ Output Voltage High (Push-pull, active LOW, CAT140xx9)	V_{CC} = V_{TH} max, I_{SOURCE} = -500µA R/S/T/Z	0.8V_{CC}			V
		V_{CC} = V_{TH} max, I_{SOURCE} = -800µA J/L/M	V_{CC} - 1.5			
V_{OL}	RESET Output Voltage Low (Push-pull, active HIGH, CAT140xx1)	V_{CC} > V_{TH} max, I_{SINK} = 1.2mA R/S/T/Z			0.3	V
		V_{CC} > V_{TH} max, I_{SINK} = 3.2mA J/L/M			0.4	
V_{OH}	RESET Output Voltage High (Push-pull, active HIGH, CAT140xx1)	1.8V < V_{CC} ≤ V_{TH} min, I_{SOURCE} = -150µA	0.8V_{CC}			V

Notes:

(1) Production testing done at T_A = +25ºC; limits over temperature guaranteed by design only.

(2) $\overline{\text{RESET}}$ output for the CAT140xx9; RESET output for the CAT140xx1.

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PIN DESCRIPTION

RESET/$\overline{\text{RESET}}$: RESET OUTPUT
This output is available in two versions: CMOS Active Low (CAT140xx9) and CMOS Active High (CAT140xx1). Both versions are push-pull outputs for high efficiency.

SDA: SERIAL DATA ADDRESS

The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

SCL: SERIAL CLOCK

The Serial Clock input pin accepts the Serial Clock generated by the Master.

A0, A1, A2: Device Address Inputs

The Address inputs set the device address when cascading multiple devices. When not driven, these pins are pulled LOW internally.

DEVICE OPERATION

The CAT140xx products combine the accurate voltage monitoring capabilities of a standalone voltage supervisor with the high quality and reliability of standard EEPROMs from Catalyst Semiconductor.

RESET CONTROLLER DESCRIPTION

The reset signal is asserted LOW for the CAT140xx9 and HIGH for the CAT140xx1 when the power supply voltage falls below the threshold trip voltage and remains asserted for at least 140ms (t_{PURST}) after the power supply voltage has risen above the threshold. Reset output timing is shown in Figure 1.

The CAT140xx devices protect µPs against brownout failure. Short duration V_{CC} transients of 4µsec or less and 100mV amplitude typically do not generate a Reset pulse.

Figure 2 shows the maximum pulse duration of negative-going V_{CC} transients that do not cause a reset condition. As the amplitude of the transient goes further below the threshold (increasing V_{TH} - V_{CC}), the maximum pulse duration decreases. In this test, the V_{CC} starts from an initial voltage of 0.5V above the threshold and drops below it by the amplitude of the overdrive voltage (V_{TH} - V_{CC}).

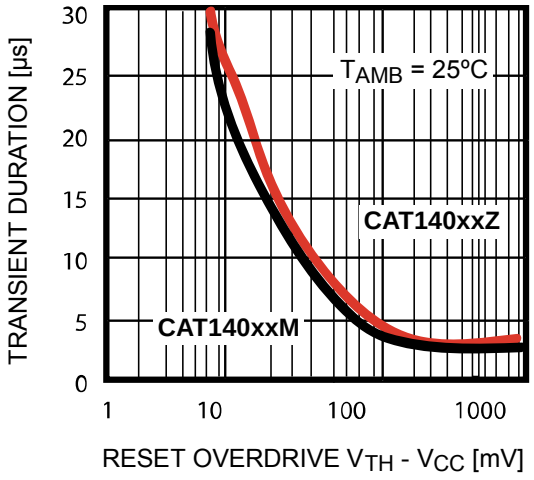

Figure 2. Maximum Transient Duration Without Causing a Reset Pulse vs. Overdrive Voltage

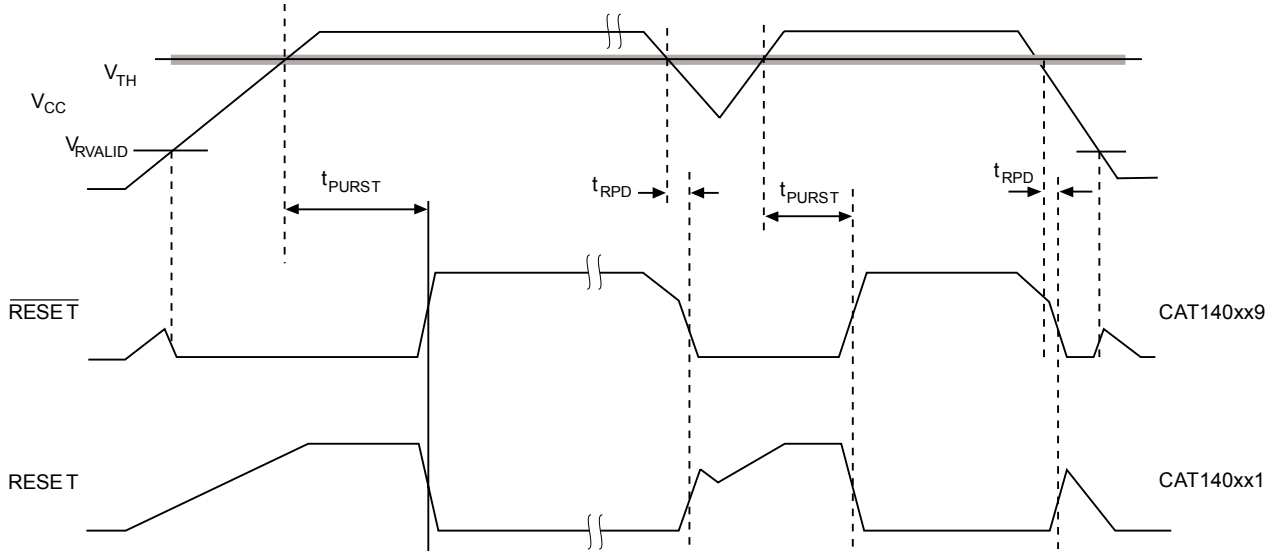

Figure 1. RESET Output Timing

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EMBEDDED EEPROM OPERATION

The CAT140xx supports the Inter-Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT140xx acts as a Slave device. Master and Slave alternate as either transmitter or receiver.

I^2C BUS PROTOCOL

The I^2C bus consists of two 'wires', SCL and SDA. The two wires are connected to the V_{CC} supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to 'transmit' a '0' and releases it to 'transmit' a '1'.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 3). The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake-up' call to all receivers. Absent a START, a Slave will not respond to commands. The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH.

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a 'wake-up' call to all receivers. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP starts the internal Write cycle (when following a Write command) or sends the Slave into standby mode (when following a Read command).

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. For normal Read/Write operations, the first 4 bits of the Slave address are fixed at 1010 (Ah). The next 3 bits are used as programmable address bits when cascading multiple devices and/or as internal address bits. The last bit of the slave address, R/$\overline{W}$, specifies whether a Read (1) or Write (0) operation is to be performed. The 3 address space extension bits are assigned as illustrated in Figure 4. A_2, A_1 and A_0 must match the state of the external address pins, and a_{10}, a_9 and a_8 are internal address bits.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 5). The Slave will also acknowledge the address byte and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. As long as the Master acknowledges the data, the Slave will continue transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by issuing a STOP condition. Bus timing is illustrated in Figure 6.

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Figure 3. START/STOP Conditions

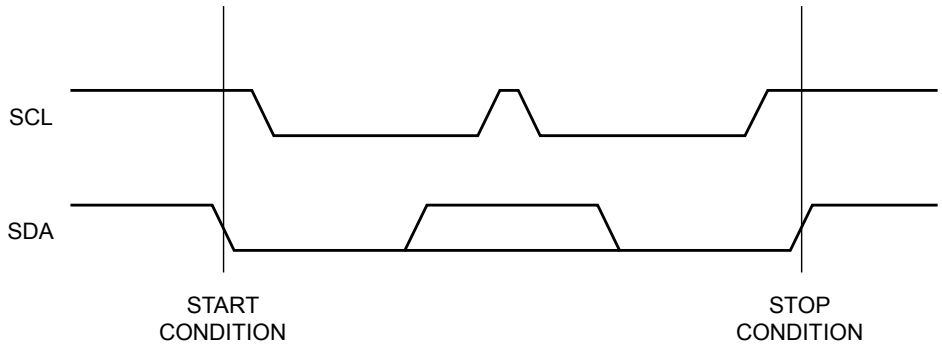


Figure 4. Slave Address Bits

1	0	1	0	A_2	A_1	A_0	R/$\overline{W}$	CAT14002
1	0	1	0	A_2	A_1	a_8	R/$\overline{W}$	CAT14004
1	0	1	0	A_2	a_9	a_8	R/$\overline{W}$	CAT14008
1	0	1	0	a_{10}	a_9	a_8	R/$\overline{W}$	CAT14016

Figure 5. Acknowledge Timing

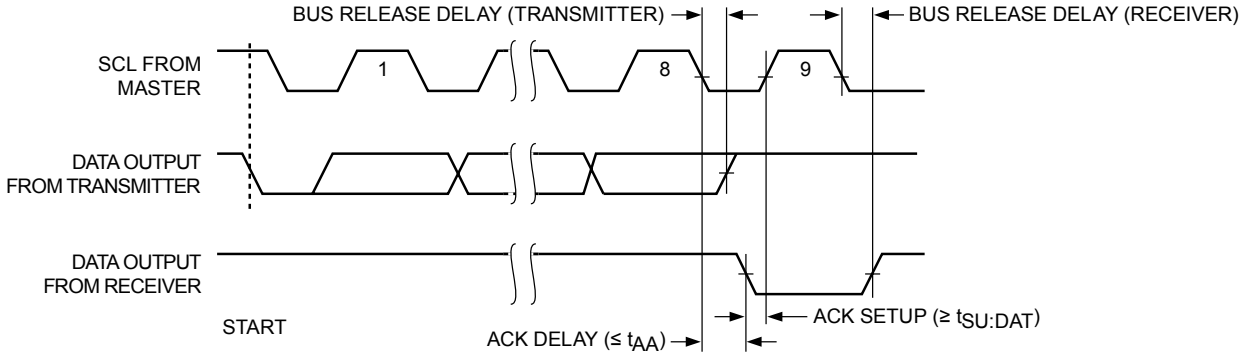
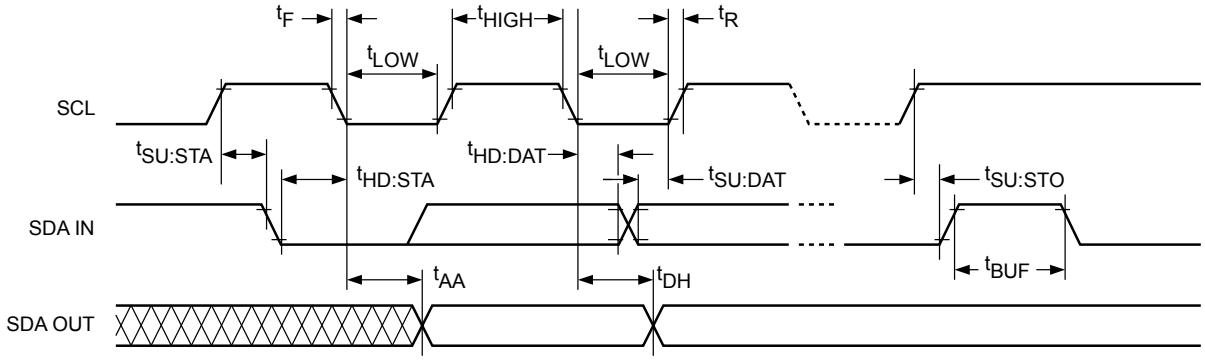


Figure 6. Bus Timing



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WRITE OPERATIONS

Byte Write

In Byte Write mode, the Master sends the START condition and the Slave address with the R/$\overline{W}$ bit set to zero to the Slave. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT140xx. After receiving another acknowledge from the Slave, the Master transmits the data byte to be written into the addressed memory location. The CAT140xx device will acknowledge the data byte and the Master generates the STOP condition, at which time the device begins its internal Write cycle to nonvolatile memory (Figure 7). While this internal cycle is in progress (t_{WR}), the SDA output will be tri-stated and the CAT140xx will not respond to any request from the Master device (Figure 8).

Page Write

The CAT140xx writes up to 16 bytes of data in a single write cycle, using the Page Write operation (Figure 9). The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the data byte is transmitted, the Master is allowed to send up to fifteen additional bytes. After each byte has been transmitted the CAT140xx will respond with an acknowledge and internally increments the four low order address bits. The high order bits that define the page address remain unchanged. If the Master transmits more than sixteen bytes prior to sending the STOP condition, the address counter 'wraps around' to the beginning of page and previously transmitted data will be overwritten. Once all sixteen bytes are received and the STOP condition has been sent by the Master, the internal Write cycle begins. At this point all received data is written to the CAT140xx in a single write cycle.

Acknowledge Polling

The acknowledge (ACK) polling routine can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT140xx initiates the internal write cycle. The ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT140xx is still busy with the write operation, NoACK will be returned. If the CAT140xx has completed the internal write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

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Figure 7. Byte Write Sequence

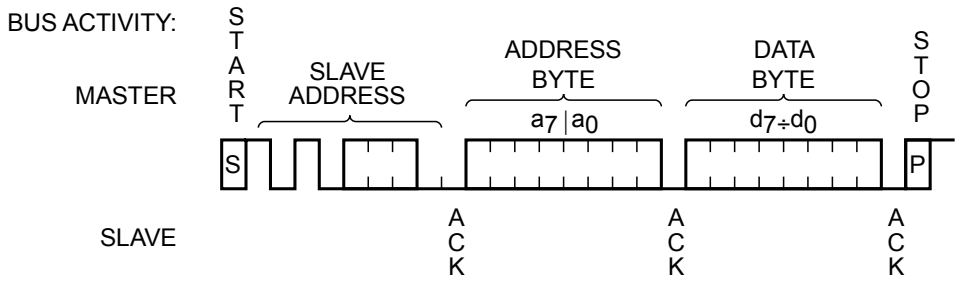


Figure 8. Write Cycle Timing

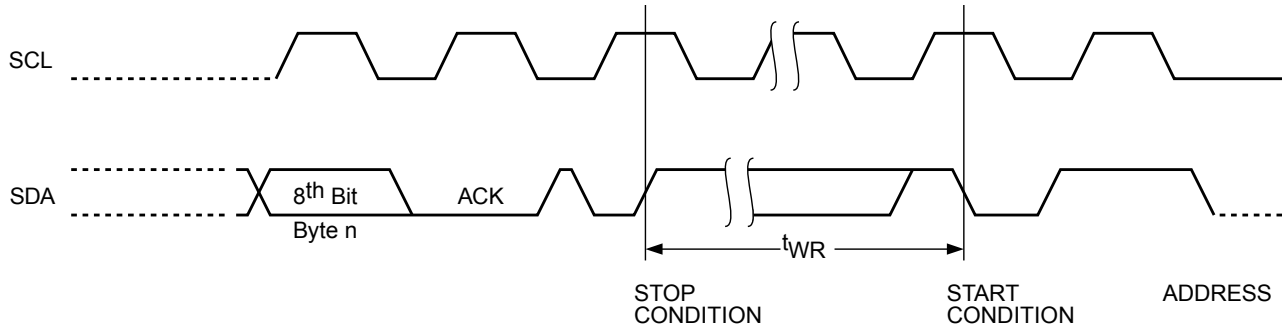
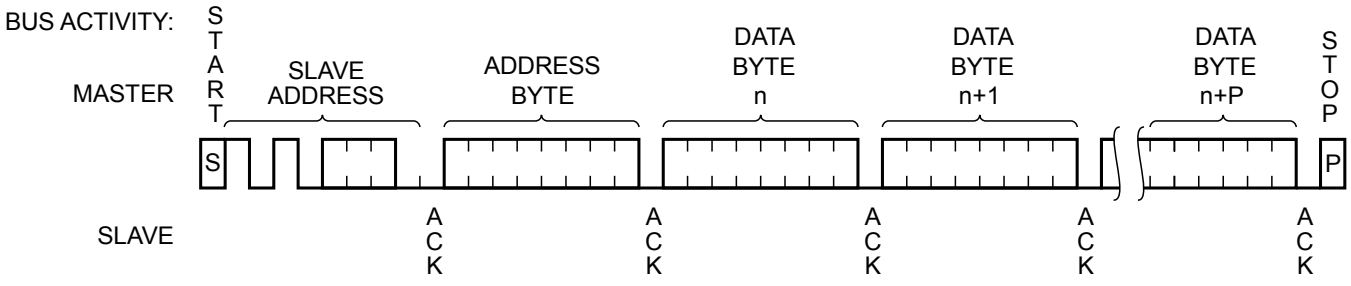


Figure 9. Page Write Timing



n = 1
P ≤ 15

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READ OPERATIONS

Immediate Read

Upon receiving a Slave address with the R/$\overline{W}$ bit set to '1', the CAT140xx will interpret this as a request for data residing at the current byte address in memory. The CAT140xx will acknowledge the Slave address, will immediately shift out the data residing at the current address, and will then wait for the Master to respond. If the Master does not acknowledge the data (NoACK) and then follows up with a STOP condition (Figure 10), the CAT140xx returns to Standby mode.

Selective Read

Selective Read operations allow the Master device to select at random any memory location for a read operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT140xx acknowledges the byte address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT140xx then responds with its acknowledge and sends the requested data byte. The Master device does not acknowledge the data (NoACK) but will generate a STOP condition (Figure 11).

Sequential Read

If during a Read session, the Master acknowledges the 1st data byte, then the CAT140xx will continue transmitting data residing at subsequent locations until the Master responds with a NoACK, followed by a STOP (Figure 12). In contrast to Page Write, during Sequential Read the address count will automatically increment to and then wrap-around at end of memory (rather than end of page).

POWER-ON RESET (POR)

Each CAT140xx incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

A CAT140xx device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level. This bi-directional POR feature protects the device against 'brown-out' failure follo–wing a temporary loss of power.

Delivery State

The CAT140xx is shipped erased, i.e., all bytes are FFh.

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Figure 10. Immediate Read Sequence and Timing

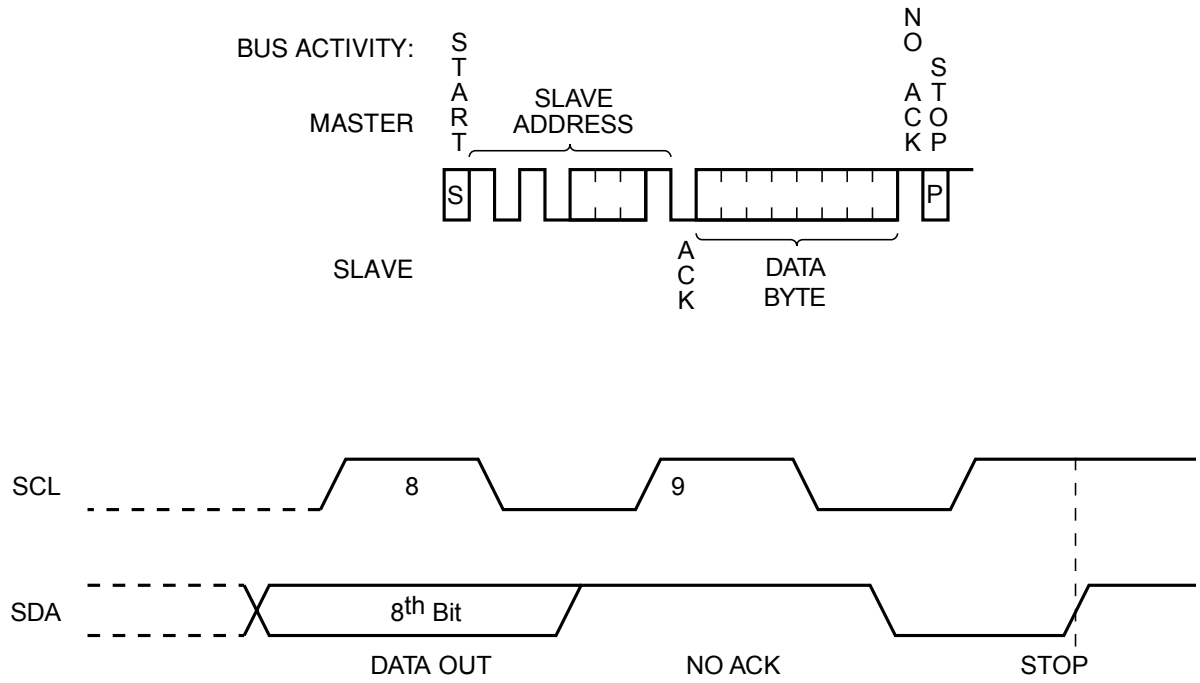


Figure 11. Selective Read Sequence

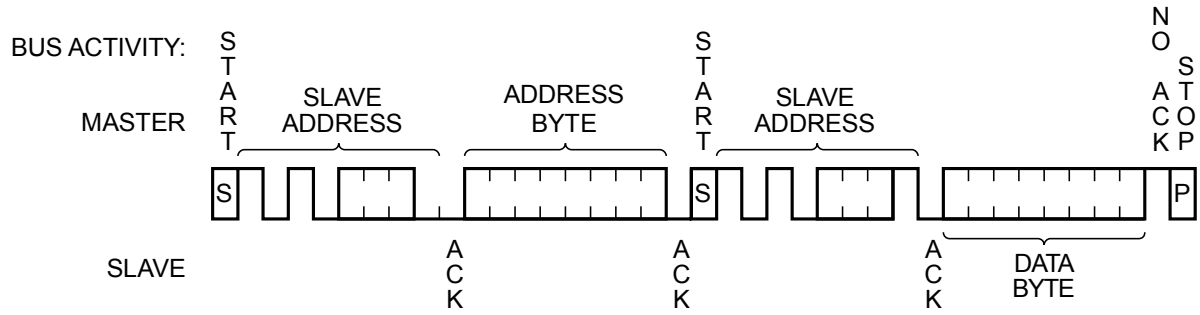
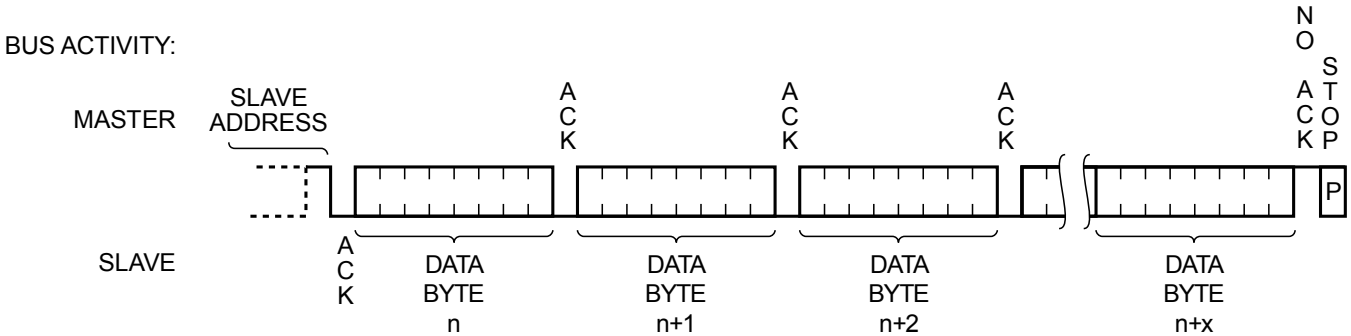


Figure 12. Sequential Read Sequence



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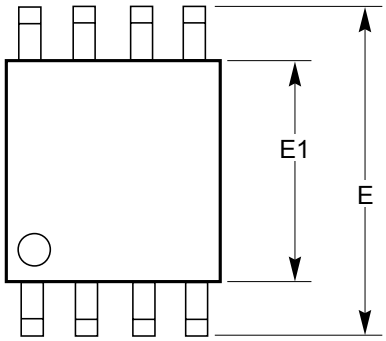
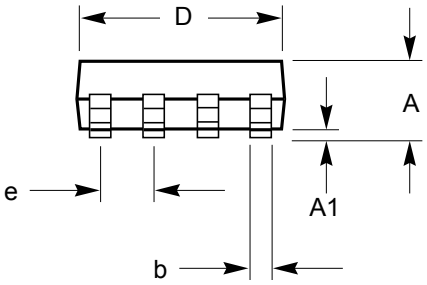
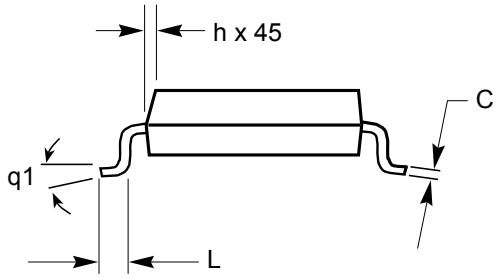
PACKAGE OUTLINES

8-LEAD 150 MIL SOIC (W)







SYMBOL	MIN	NOM	MAX
A1	0.10		0.25
A	1.35		1.75
b	0.33		0.51
C	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
q1	0°		8°

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

(1) All dimensions are in millimeters.

(2) Complies with JEDEC specification MS-012 dimensions.

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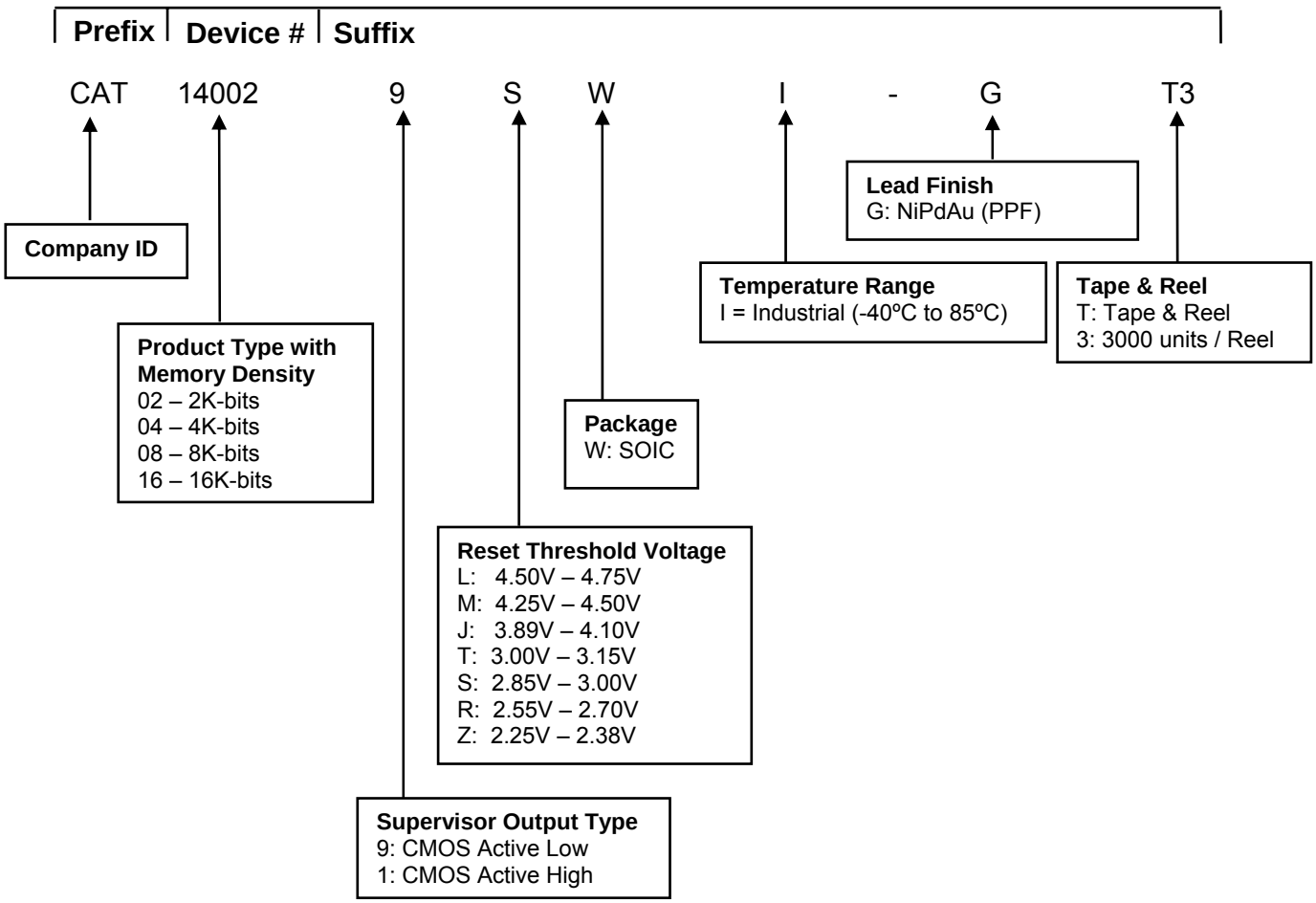
ORDERING INFORMATION



Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).

(2) The standard lead finish is NiPdAu pre-plated (PPF) lead frames.

(3) The device used in the above example is a CAT140029SWI-GT3 (2Kb EEPROM, with Active Low CMOS output, with a reset threshold between 2.85V - 3.00V, in an SOIC, Industrial Temperature, NiPdAu, Tape and Reel.

(4) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

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REVISION HISTORY

Date	Rev.	Reason
11/09/06	A	Initial Issue

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