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CAT35C904

RF SECURE ACCESS Serial E^2PROM

Preliminary Spec

DESCRIPTION

The CAT35C904 is a 4K-bit, RF version of the Secure Access Serial EEPROM devices, and a member of CATALYST Semiconductors proprietary family of intelligent memories. With this configuration, the user now has a monolithic solution to contact-less serial communication. Communication and power requirements for operation are derived from a received sinusoidal signal in the 100 to 500 KHz range. On-chip regulation and rectification of the incoming transmission provides the power necessary for operation, including the high voltages required for EEPROM programming. Instructions and data are FSK (Frequency Shift Keyed) modulated onto the incoming signal, and are demodulated on chip, while the outgoing data is passively modulated back onto the same coil used for incoming data. The memory array organization is software selectable as either a 256 X 16 or 512 X 8 array. The CAT35C904 can be operated in either a SECURE or UNPROTECTED mode, as described below.

FEATURES

- Contactless Serial Communication
- On-chip power generation
- Password READ/WRITE - protect
- Non-password WRITE - protect
- Sequential data register READ
- User definable protected area
- Password length: 1 to 8 bytes
- Data format: x8 or x16
- Low power consumption
- 10 year data retention
- 10,000 write/erase cycles

SECURE MODE

The secure mode is activated with a MACC instruction followed by 1 to 8 bytes of user access code. Once activated, the protection of the memory is under software control. Without the execution of the ENAC instruction, followed by the correct access code, the memory array is inaccessible for any operation attempted at addresses below that of the memory pointer, and is read-only for the array area above the memory pointer. This provides the user a portion of memory that is readable by users not priviledged to the access code while keeping a portion of memory invisible to them. Once an ENAC (enable access) instruction, followed by a valid access code, has been issued, the entire memory array is readable by any user.

A two tier protection scheme is provided to protect against inadvertent writing and erasure of the memory. To write to the array, the user must first issue a EWEN instruction. The CAT35C904 will now allow write/erase operations to be performed only on the portion of memory above the memory pointer. Memory locations below the memory pointer address remain protected from any write, or erase operation. To override this protection, an OVMPR (override memory pointer) instruction must be issued. This will allow a single instruction to override the protection and enable write/erase operations to that portion of memory below the memory pointer.

As shipped from the factory the device is in the unprotected mode. The length of the access code is user selectable, from a minimum of 1 byte to a maximum of 8 bytes, thus yielding a maximum of 1.84×10^{19} possible access codes. Loading a zero length access code will disable protection.

UNPROTECTED MODE

As shipped from the factory, the CAT35C904 is in the unprotected mode (Access Registers contain "FFFF FFFF FFFF FFFF" and the code length is set to "0000"). When in this mode any portion of the EEPROM array can be read or written to without an access code while the memory pointer is at address 00 Hex. Once the memory pointer is modified, via the WMPR instruction, any EEPROM address below the address of the memory pointer is protected from any write or erase operation, thereby preventing accidental erasure or overwriting of data.

AC RECTIFIER

The AC Rectifier consists of a full wave rectifier with a shunt regulator for high voltage programming generation, and a series regulator for the low voltage supply. The regulator outputs are available on external pins to allow the addition of external filter capacitors. Tables 1 and 2 show performance characteristics of the series and shunt regulators respectively.

MEMORY POINTER

The memory pointer enables the user to segment the EEPROM array. While in the unprotected mode the array can be segmented between read-only and full access. When in the secure mode, the array can be segmented between read-only or no access. There are three instructions that are dedicated to the memory pointer operation. The first of these is the WMPR (write memory pointer) instruction. This instruction, followed by an address, will reload the memory pointer register with this new address and store it in EEPROM where it can only be modified via another WMPR command. If the device is in the secure mode, this instruction must be preceded by the ENAC instruction and a valid access code. The second instruction, OVMPR, will allow a single write/erase to the array contents below the memory pointer. This allows the user to modify a segmented array without having to move the pointer. Once this instruction is completed, the array returns to its previously protected mode. The last memory pointer instruction, RMPR, will allow the current contents of the memory pointer to be put onto the serial port.

PARAMETER	CONDITIONS	VALUE
Operating Supply Current		65 µ A
Output Voltage (Adjustable to 2%)		4.99± .1
Line Regulation	DC	0.1 %
	300 KHz	20 %
Load Regulation	10 uA < IL < 100 uA	2 Ohms
	100 uA < IL < 10 mA	1 Ohm
Reference Voltage		2.53 V
Temperature Coefficent	Before Bandgap Trim	200 ppm/C
	After Bandgap Trim	30 ppm/C
Start-up Settling time	0 - 8 V Step Response	9 µ S

Table 1: Series 5 Volt Regulator

The rectifier/regulator schematiic is shown in figure 1. Devices Q3 and Q4, in conjunction with MOS transisors Q1 and Q2, form the full wave rectifier circuit. The output of the rectifier is then pre-regulated by the shunt regulator to provide the EEPROM programming voltage. This voltage is then further regulated by the series regulator to produce the 5 volt logic supply.

The shunt regulator consists of series zeners that are fabricated as a normal flow within the CATALYST BICMOS technology. The series regulator utilizes a bandgap topology that is then amplified to produce the 5 volt logic supply.

OUTGOING DATA

Data transmission is accomplished with a passive scheme that utilizes the system signal coil. Transmission is achieved by loading one side of the input coil and having the host system detect the reflected energy. It should be noted that simultaneous bidirectional transmissions are not supported.

Once the system clock is sampled at power up, a system with an initial transmission of 500 KHz would have data appearing across the coil at a 9600 Baud rate. Any deviation from the originating systems frequency would be proportionally reflected in the communication input and output transmission rates.

PARAMETER	CONDITIONS		VALUE
Output Impedance	60 μ A < I_{bias} <100 μA	DC	1 OHM
		300 KHz	5.6 OHMS
Minimum Operating Current			40 μ A
Start-up Time for 5 mA Current Step	C_L = 100 pF		20 μ S
Bandgap Voltage for Zero Tempco			2.56 V
Temperature Coefficient	-55 C to +125 C		50 ppm
Total Output Noise	10 Hz to 80 KHz		2.5 mV
Breakdown Voltage (Adjustable to 2% with EE fuse)	60μ A < I_{bias} < 80 mA		4.74 V

Table 2: RF Shunt 5 Volt Regulator

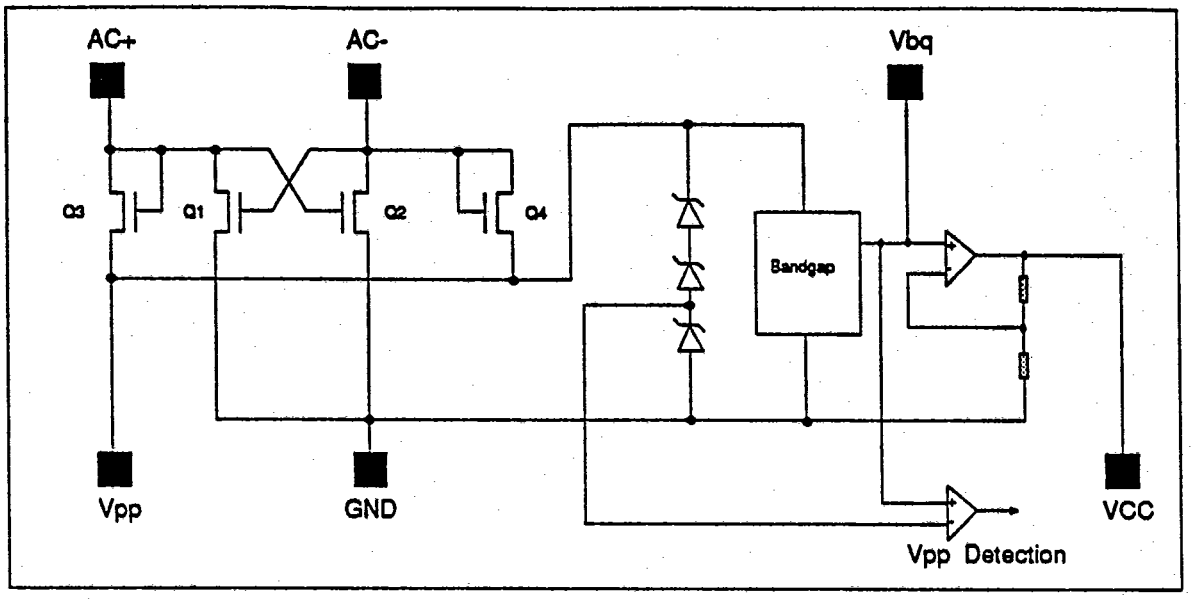


Figure 1: Rectifier - Regulator Topology

INCOMING DATA

The CAT35C904 demodulates the FSK incoming data using an internal oscillator and time base. A logic "1" is received for a 500 KHz signal, while a "0" corresponds to a 100 KHz frequency. Figure 2 shows the incoming data protocol. Only a Byte oriented protocol will be supported. This includes a start bit, eight bits of data, a parity bit and a stop bit. Resynchronization is initiated with each start bit detection, and the incoming frequency is "learned" during the initial chip power-up sequence.

As the incoming signal is first detected by the chip, the internal rectifier and regulators are first allowed to stabilize, and the incoming 500 KHz frequency is monitored for synchronizing the internal oscillator to the external system time base. The synchronization is accomplished by a unique successive digital approximation technique. This method measures the internal oscillator cycles for four periods of the external frequency, and determines if a counter overflow has occurred. If an overflow did occur, an internal divider is incremented, and the measurement is repeated. Once a count is accomplished without an overflow, the internal frequency for a 9600 Baud data rate is within 3 % of the external frequency. This "learned" frequency is then used to divide down, and establish the needed clocking for 9600 Baud communications. Once synchronization is established, the device will transmit the current Status Register content to indicate it is ready for incoming data. The CAT35C904 will be able to to rectify and demodulate signals down to (100uA)(SIN[2π(100K)t]), and will have an absolute maximum input rating of (50mA)(SIN[2π(500K)t]).

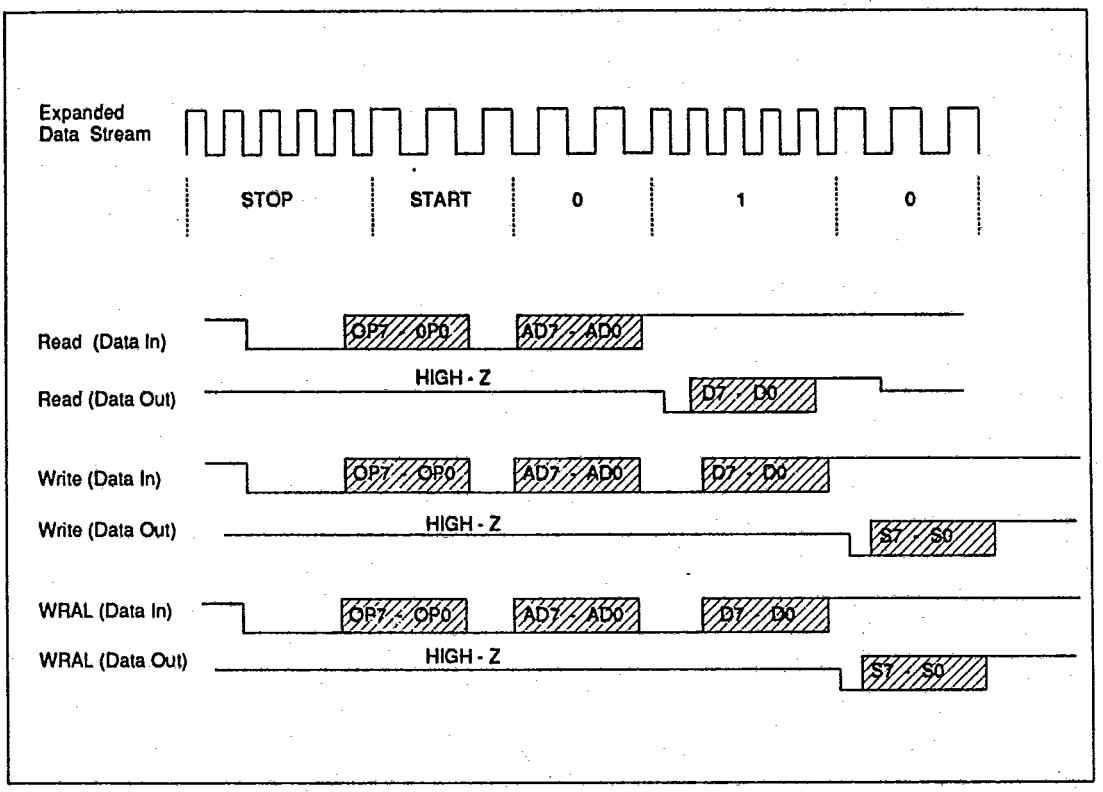


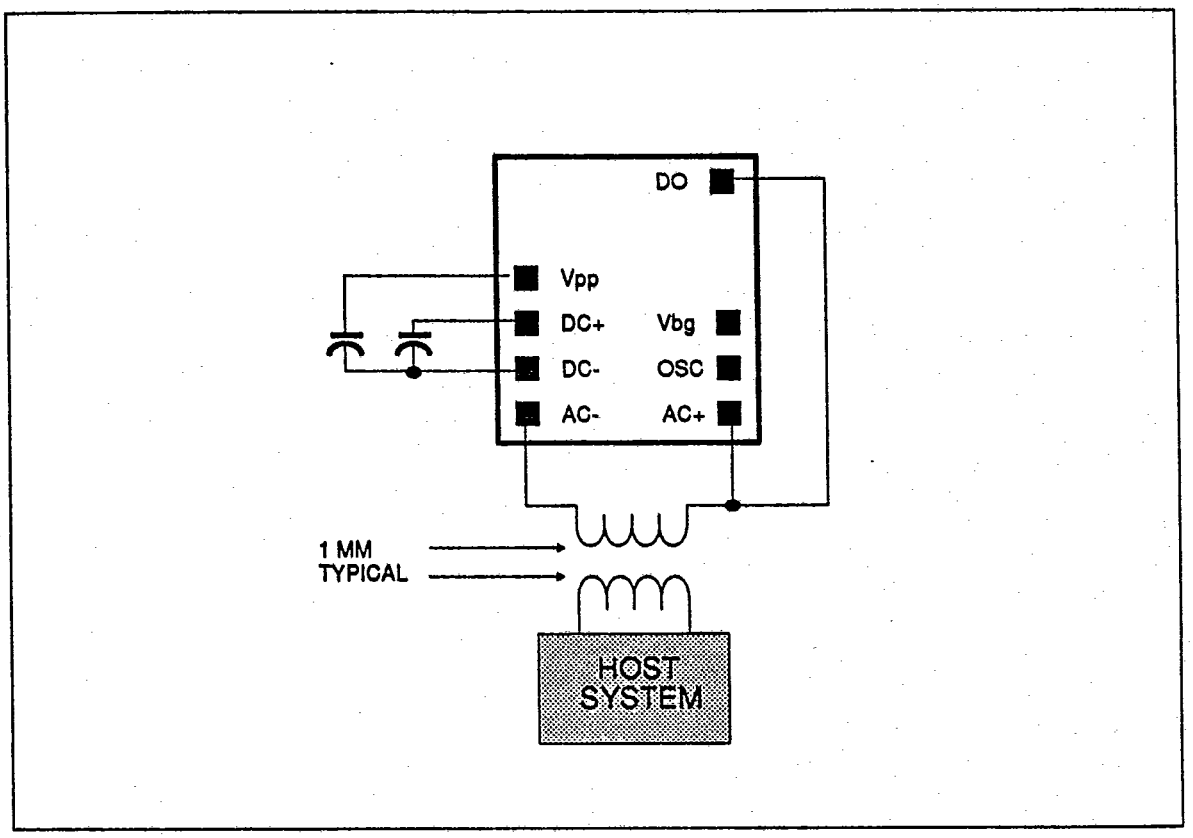
FIGURE 2: DATA PROTOCOL

PROGRAMMING

Programming of the EEPROM array is accomplished through the eight programming instructions. The V_{pp} programming voltage is generated through the received sinusoidal signal and is then rectified and regulated. During any write EEPROM operation, the CAT35C904 will first determine if the amplitude of the induced programming voltage is within a predetermined range. Once verified, this voltage will be applied to the EEPROM array and a self timed programming cycle will commence. Once programming has completed, the CAT35C904 will transmit the contents of the status register, thus indicating the completion of the programming cycle.

STATUS REGISTER

An eight bit status register is provided to allow the user to determine the status of the CAT35C904. The first three bits of this register are fixed as a "101" pattern allowing the user to quickly determine if the device is in a listening mode or is in an error condition. The next three bits give the status of parity error (for the prior instruction), instruction error (for the prior instruction), or RDY/BUSY. The last two bits are reserved for future use.



TYPICAL CONFIGURATION

INSTRUCTION SET

DISAC Disable Access
1000 1000

This instruction will lock the memory from all write/erase operations regardless of the contents of the memory pointer. A write can be accomplished only by first entering the ENAC instruction followed by a valid access code.

ENAC Enable Access
1100 0101 (to be followed by access code)

In the protected mode, this instruction, followed by a valid access code, unlocks the device for read/write/erase access.

WMPR Write Memory Pointer Register
1100 0100 Addr 15-8 Addr 7-0
(for x8 organization)
1100 0100 Add 7-0
(for x16 organization)

The WMPR instruction followed by 8 or 16 bits of address (depending on the organization) will move the pointer to the newly specified address.

MACC Modify Access Code
1101 NNNN Old access code
New access code New access code

This instruction requires the user to enter the old access code, if one was set previously, followed by the new access code and a re-entry of the new access code for verification. Within the instruction format, the variable NNNN designates the length of the access code as the following :

NNNN = 0No access code. Set device to unprotected mode
NNNN =1-8 Length of access code is 1 to 8 bytes
NNNN > 8Illegal number of bytes. The CAT35C704 will ignore the rest of the transmission

RMPR Read Memory Pointer Register
11001010

Output the content of the memory pointer register to the serial output port.

OVMPR Override Memory Pointer Register
1000 0011

Override the memory protection for the next instruction.

READ Read Memory
1100 1001[Addr 15-8][Addr 7-0]
(for x8 organization)
1100 1001[Addr 7-0]
(for x16 organization)

Output the contents of the addressed memory location to the serial port. For the UART protocol - start, stop, and parity bits are added to the data byte.

WRITE Write memory
1100 0001[Addr 15-8][Addr 7-0]
[Data 7-0]
1100 0001[Addr 7-0][Data 15-8]
[Data 7-0]

WRITE the 8-bit or 16-bit data to the addressed memory location. After the instruction, address, and data have been entered, the self-timed WRITE sequence will start. The addessed memory location will be erased before data is written. The DO pin may be used to output the RDY/BUSY status by having previously entered the ENBSY instruction. During the write cycle, DO will output a LOW for BUSY during the write cycle and a HIGH for READY after the cycle has been completed.

ERASE Erase Memory
1100 0000
Addr 15 -8 Addr 7-0
(for x8 organization)
1100 0000
Addr 7-0
(for x16 organization)

Erase data in the specified memory location (set memory to "1"). After the instruction and the address have been entered, the self-timed erase sequence will start. The DO pin may be used to output the

RDY/BUSY status by having previously entered the ENSBY instruction. During the erase cycle, DO will output a LOW for BUSY during the write cycle and a HIGH for ready after the cycle has been completed.

ERAL Erase All
1000 1001
1000 1001

Erase the data of all memory locations (all cells can be set to "1"). For protection against inadvertent chip erase, the ERAI instruction is required to be entered twice.

WRAL Write All
1000 1001
1100 0011 Data 15-8 Data 7-0
(for x16 organization)
1000 1001
1100 0011 Data 7-0
(for x8 organization)

Write one or two bytes of data to all memory locations. An ERAL will be automatically performed before the WRAL is executed. For protection against inadvertent overwriting of data, the ERAL instruction is required to be entered preceding the WRAL instruction.

RSEQ Read Sequentially
1100 1011
Addr 15-8 Addr 7-0
(for x8 organization)
1100 1011
Addr 7-0 (for x16 organization)

Read memory starting from specified address, n, then n+1, etc, to the highest address or until CS goes LOW. The instruction will be terminated when CS goes LOW.

ENBSY Enable Busy
1000 0100

Enable the status indicator on DO during write/erase cycle.

DISBSY Disable Busy
1000 0101

Disable the status indicator on DO during write/erase cycle

EWEN Erase/Write Enable
1000 0001

Enable erase/write to be performed on non-protected portion of memory. This instruction must be entered before any write/erase instruction. Once entered, it will remain valid until power-down or an EWDS (Erase/Write Disable) is executed.

EWDS Erase/Write Disable
1000 0010
Disable all erase and write functions

ORG Select Memory Organization
1000 011R (where R = 0 or 1)
Set memory organization
to 512x8 if R = 0.
Set memory organization
to 256x16 if R = 1.

RSR Read Status Register
1100 1000

Output the contents of the 8-bit status register. The contents of first three bits of the register is 101 which allows the user to quickly determine whether the device is listening or is in an error condition. The next three bits indicate the status such as ready/busy or, if an error existed in the previous instruction, instruction error or parity error. The last two bits are reserved for future use.

NOP No Operation
1000 0000
No operation.