CAT4026

6-Channel LED Controller with Fault Diagnostics for Large Panel LED Backlighting

ON Semiconductor®

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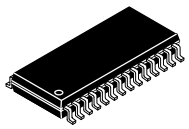


SOIC−28
V SUFFIX
CASE 751BM

Description

The CAT4026 is a high performance, large panel LED controller designed to control six constant current high voltage LED strings. Added control circuitry monitors the lowest cathode voltage and generates a feedback control signal to an external Switch Mode Power Supply (SMPS) to provide a low cost and efficient solution for large panel high voltage LED backlighting.

Each LED channel current is accurately matched and controlled by sensing an external resistor in series with a low cost bipolar power transistor. This allows current and heat dissipation concerns to be mitigated from the CAT4026 device package.

For added system reliability, both Open−Cathode−Anode (OCA) and Shorted−Cathode−Anode (SCA) fault detection circuitry has been included along with independent Fault flag logic outputs for diagnostic purposes.

LED current dimming in all six channels can be precisely controlled by either a Pulse Width Modulation signal via the PWM input pin or by an analog dimming voltage applied at the ANLG pin. In addition the ANLG pin provides a convenient method for limiting the overall maximum power dissipation in the event of excessive LED shorting within any LED string.

The device will automatically enter low current shutdown mode by taking the PWM pin low for an extended length of time.

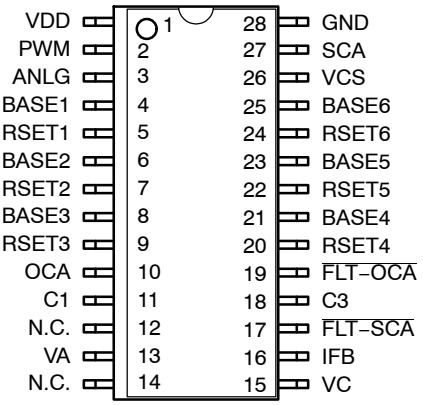
Features

- 6 Channel LED Controller
- Adaptive Feedback Control to External SMPS for Better Efficiency
- PWM and Analog Mode Dimming
- Short Cathode−Anode (SCA) Fault Protection
- Open Cathode−Anode (OCA) Fault Protection
- Over−Voltage Protection
- Thermal Shutdown Protection
- Automatic Inactivity Power Down Mode
- SOIC−28L Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- LCD−TV LED Backlighting
- LED General Lighting

PIN CONNECTIONS



(Top View)

MARKING DIAGRAM

L = Assembly Location Code
3 = Mark “3” for (lead finish Matte−Tin)
A = Product Revision: Fixed as “A”
CAT4026V = Specific Device Code
YY = Production Year (Last Two Digits)
WW = Production Week (Two Digits)
XXXX = Last Four Digits of Assembly Lot Number

ORDERING INFORMATION

Device	Package	Shipping
CAT4026V−T1 (Note 1)	SOIC−28 (Pb−Free)	1,000/ Tape & Reel

1. Matte Tin Plated Finish (RoHS−compliant)

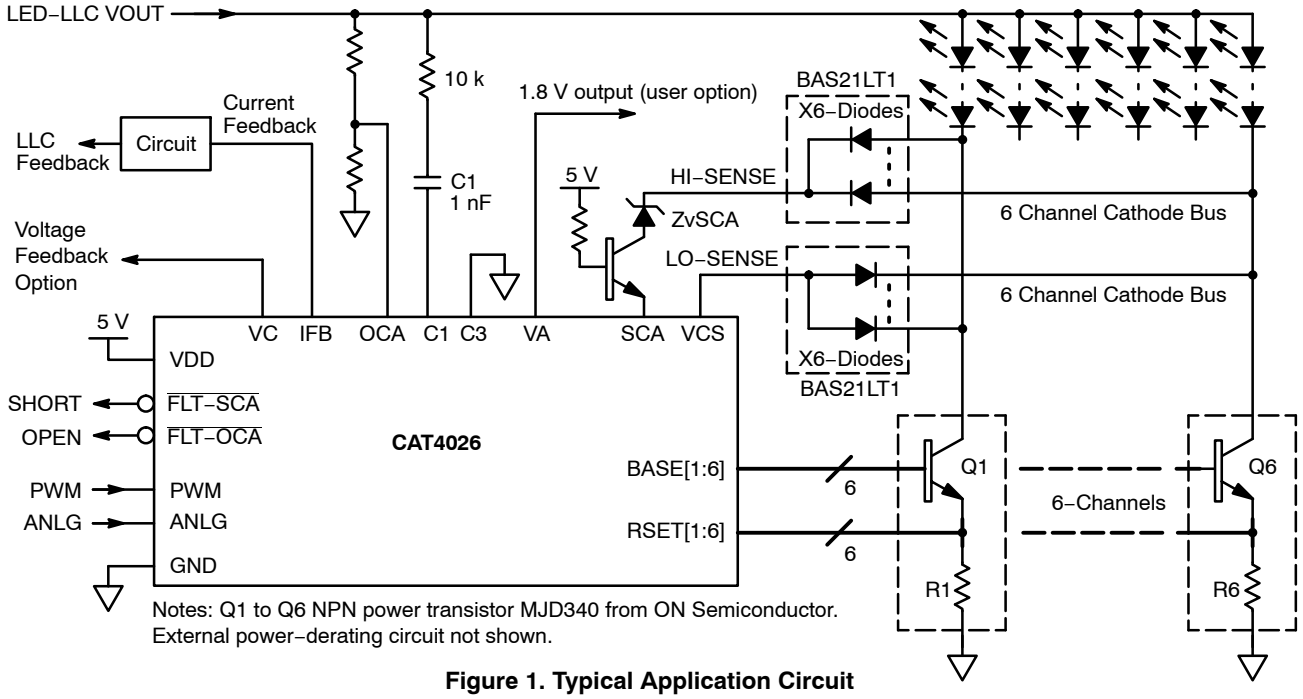


Figure 1. Typical Application Circuit

Table 1. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
VDD Voltage Range	V_{in}	−0.3 to 7	V
PWM, ANLG, $\overline{\text{FLT−OCA}}$, $\overline{\text{FLT−SCA}}$ Voltage Range	PWM	−0.3 to 7 V or (V_{in} + 0.3), whichever is lower	V
RSET[x], BASE[x]		−0.3 to 7 V or (V_{in} + 0.3), whichever is lower	V
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   This device meets latchup tests defined by JEDEC Standard JESD78.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

Table 2. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOIC−28			°C/W
Thermal Resistance, Junction−to−Air (Note 4)	$R_{\theta JA}$	79	
Thermal Resistance, Junction−to−Case (Note 4)	$R_{\psi JC}$	23	

4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

Table 3. OPERATING RANGES

Rating	Symbol	Min	Max	Rating
Input Voltage	V_{in}	4.5	5.5	V
Ambient Temperature	T_A	−40	85	°C

Table 4. ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, V_{PWM} = V_{DD}, V_{ANLG} = 3.3 V, for typical values T_A = 25°C, for min/max values T_A = −40°C to +85°C; unless otherwise noted.)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
RSET[x] pin voltage		V_{RSET}	0.97	1.00	1.03	V
RSET channel to channel voltage matching	(V_{RSET} − $V_{RSETAVR}$) / $V_{RSETAVR}$, Nominal current 100 mA per channel	$V_{RSET-MAT}$		±0.6	±2.0	%
RSET device to device matching		V_{RSET-D}		±0.6	±2.5	%
IFB sink current	V_{VCS} = 3.6 V	I_{IFB}		0.5		mA
VA output voltage	VA pin no load	V_{VA}		1.8		V
VA output resistance	100 μA load	R_{VA}		250		Ω
VC output voltage	VC pin no load, VCS pin = 3.6 V	V_{VC}		1.8		V
VC output resistance	100 μA load	R_{VC}		360		Ω
VCS pull−up resistance to V_{DD}	V_{PWM} = 5 V	R_{VCS}		50		kΩ
SHUTDOWN, DISABLE, QUIESCENT CURRENTS						
Shutdown Current	Shutdown mode (PWM low for > 50 ms)	I_{OFF}	−	50		μA
Disable Current	V_{PWM} = 0 V, all channels off (PWM low for < 20 ms)	I_{DIS}	−	1.5		mA
Quiescent Current (Note 5)	V_{PWM} = 5 V, R1 to R6 = 10 Ω (100 mA load per channel), application circuit as shown with 0.8 mA BASE pin current per channel	I_Q	−	16		mA
	No external circuit components present, all BASE[x] and RSET[x] pins floating			7.6		mA
Short Circuit Supply Current	V_{VCS} = GND, all BASE[x] shorted to Ground	I_{Q-MAX}	−	118		mA
LOGIC I/OS						
PWM pull−down resistance	V_{PWM} = 5 V	R_{PWM}	80	120	200	kΩ
PWM Input Threshold Voltage V_{IH} Logic High V_{IL} Logic low		 $V_{PWM-VIH}$ $V_{PWM-VIL}$	 − −	 1.2 1.0	 − −	V
ANLG divider network pull−down resistance		R_{ANLG}	120	150	180	kΩ
ANLG to RSET pin voltage ratio (V_{ANLG} / V_{RSET})	V_{ANLG} ≤ 3.0 V, all outputs on, R1−R6 = 10 Ω	V_{ANLG} /V_{RSET}		3		−
OPEN CATHODE−ANODE FAULT DIAGNOSTICS						
OCA open−LED threshold voltage		V_{OCA}	0.97	1.00	1.03	V
$\overline{FLT-OCA}$ pin pull−down voltage	Open Cathode Anode fault is active, 5 mA sink current	$V_{FLT-OCA}$		65		mV
$\overline{FLT-OCA}$ open−drain leakage	Open Cathode Anode fault is inactive	$I_{FLT-OCA}$		0.2		μA
$\overline{FLT-OCA}$ fault delay	Delay between OCA fault and $\overline{FLT-OCA}$ active	$T_{FLT-OCA}$		1		μs
SHORT CATHODE−ANODE FAULT DIAGNOSTICS						
SCA fault detection threshold sink current	$\overline{FLT-SCA}$ transitions to active state (low)	I_{SCA-ON}		1.3		mA
SCA fault cleared threshold sink current	$\overline{FLT-SCA}$ transitions to inactive state (high)	$I_{SCA-OFF}$		0.4		mA
$\overline{FLT-SCA}$ pin pull−down voltage	Short Cathode Anode fault is active, 5 mA sink current	$V_{FLT-SCA}$		65		mV
$\overline{FLT-SCA}$ fault delay	Delay between SCA fault and $\overline{FLT-SCA}$ active	$T_{FLT-SCA}$		35		μs
$\overline{FLT-SCA}$ open−drain leakage	Short Cathode Anode fault is inactive	$I_{FLT-SCA}$		0.2		μA

5. The quiescent current depends on the external bipolar transistors used (ON Semiconductor MJD340) and more specifically of its DC current gain (h_{FE}).

Table 4. ELECTRICAL CHARACTERISTICS (V_{DD} = 5 V, V_{PWM} = V_{DD}, V_{ANLG} = 3.3 V, for typical values T_A = 25°C, for min/max values T_A = −40°C to +85°C; unless otherwise noted.) (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
TIMING						
PWM Enable Time	V_{PWM} = 0 V to V_{DD} I_{out} = 0 mA to 90% of $I_{out(nom)}$	t_{EN}		800		ns
PWM Disable Time	V_{PWM} = V_{DD} to 0 V I_{out} = $I_{out(nom)}$ to 10% of $I_{out(nom)}$	t_{DIS}		1		μs
Turn−off Shutdown Time, PWM falling to shutdown	V_{PWM} = 5 V to 0 V I_{out} = $I_{out(nom)}$ to shutdown mode	t_{OFF}		25		ms
Channel to channel turn on and turn off delay (staggering)		t_{CC}		50		ns
THERMAL SHUTDOWN						
Thermal Shutdown Temperature		T_{SD}	–	150	–	°C
Thermal Shutdown Hysteresis		T_{SH}	–	20	–	°C

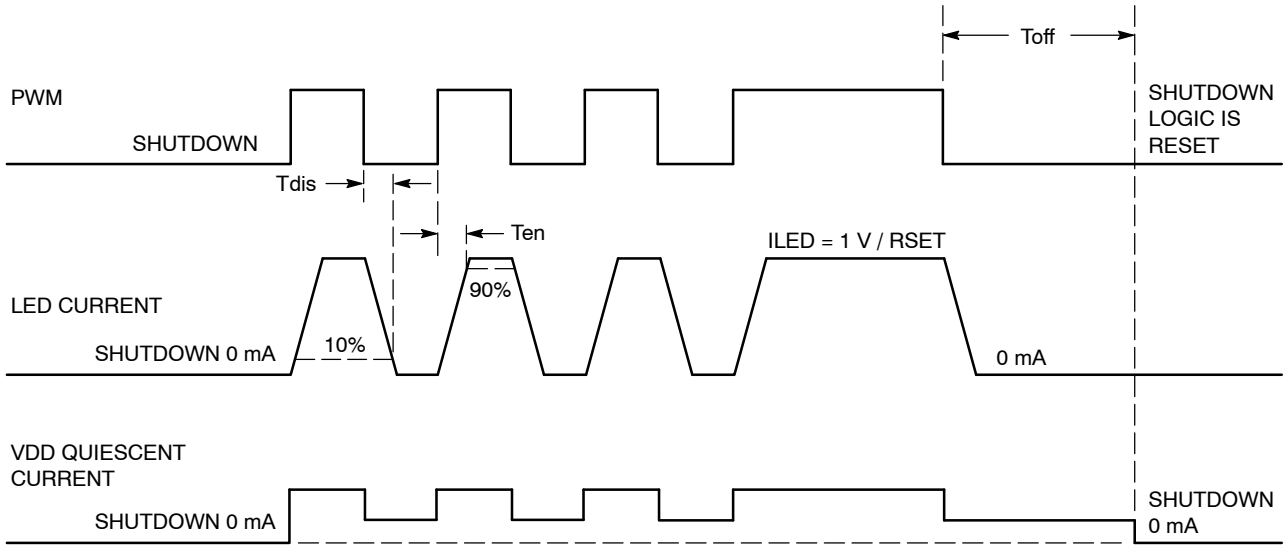


Figure 2. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{DD} = V_{PWM} = 5 V, V_{ANLG} = 3.3 V, T_{AMB} = 25°C unless otherwise specified.)

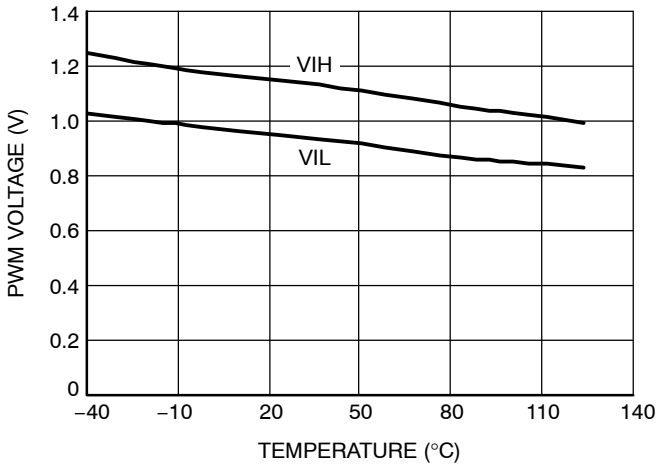


Figure 3. PWM Threshold Voltage vs. Temperature

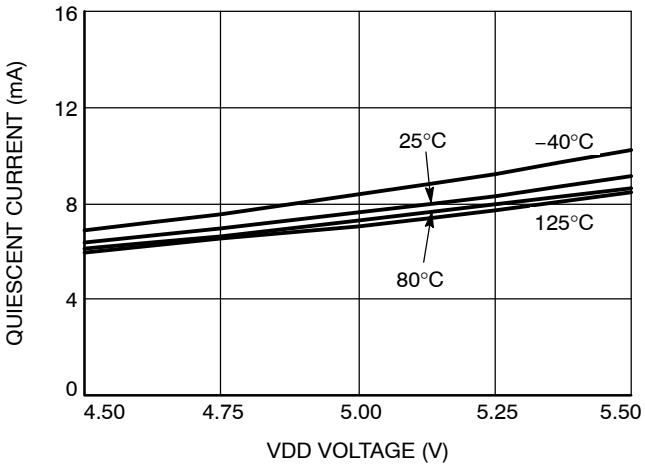


Figure 4. Quiescent Current vs. Temperature

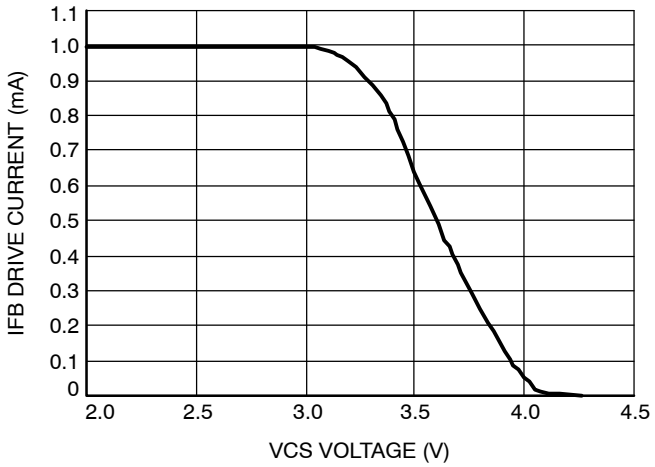


Figure 5. IFB Sink Current vs. VCS Voltage

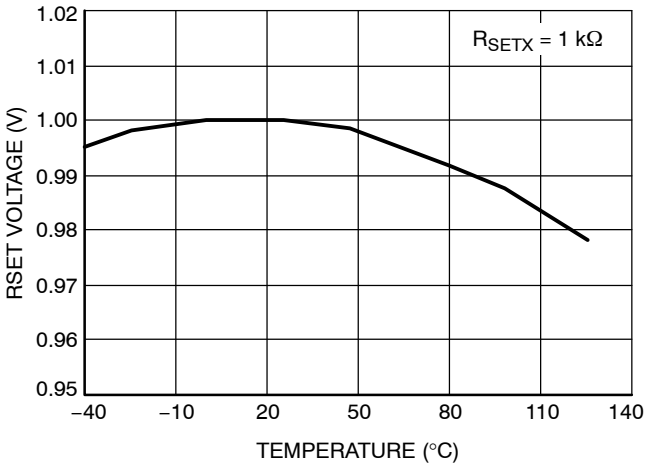


Figure 6. RSET Voltage vs. Temperature

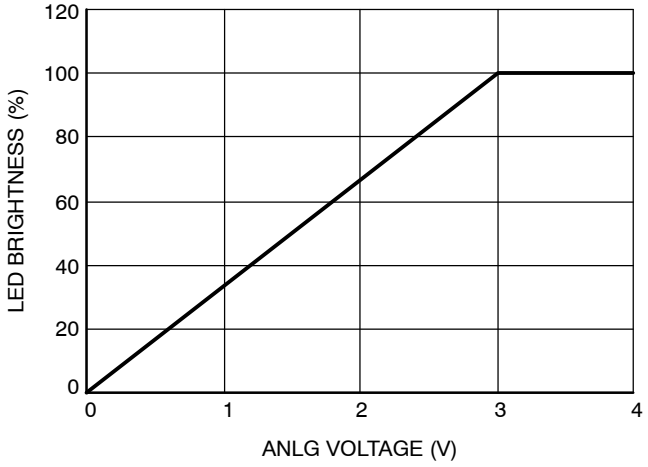


Figure 7. LED Brightness vs. ANLG Voltage

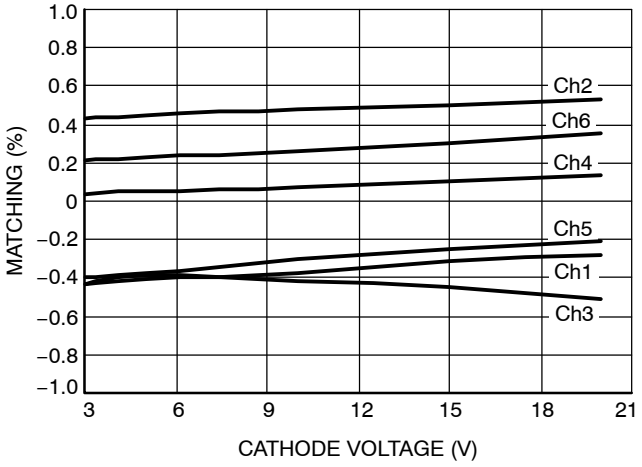


Figure 8. Matching Channel−to−Channel vs. Cathode Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{DD} = V_{PWM} = 5 V, V_{ANLG} = 3.3 V, T_{AMB} = 25°C unless otherwise specified.)

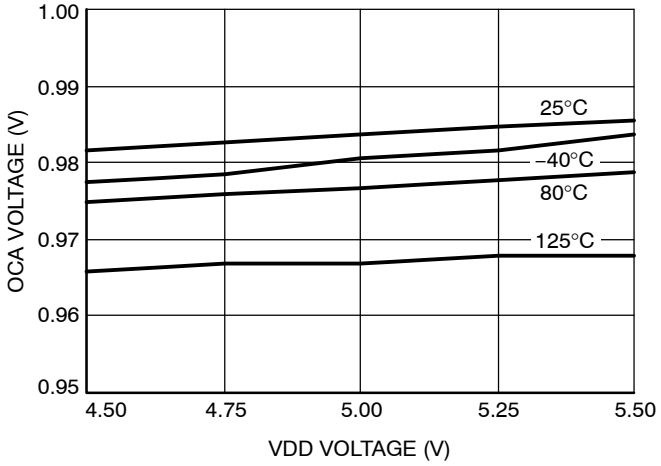


Figure 9. OCA Threshold Voltage vs. Temperature

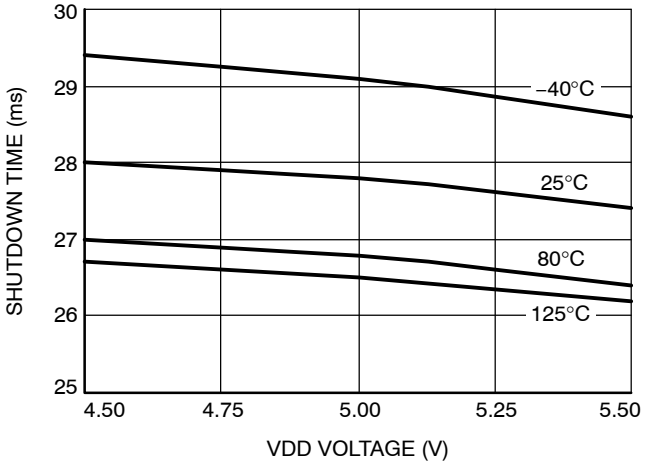


Figure 10. Shutdown Time vs. Temperature

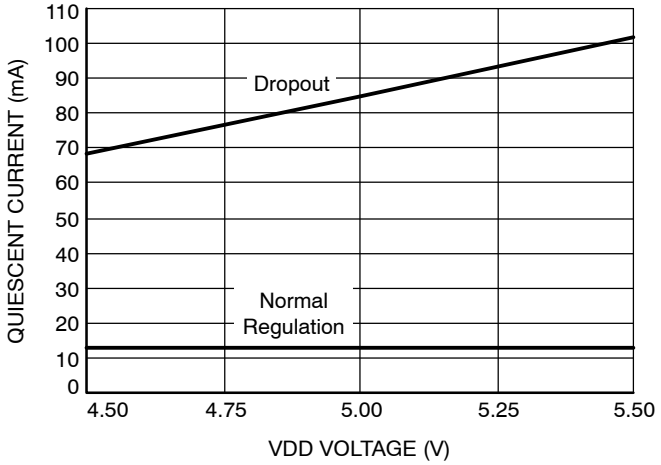


Figure 11. Quiescent Current vs. Supply Voltage (Note 6)

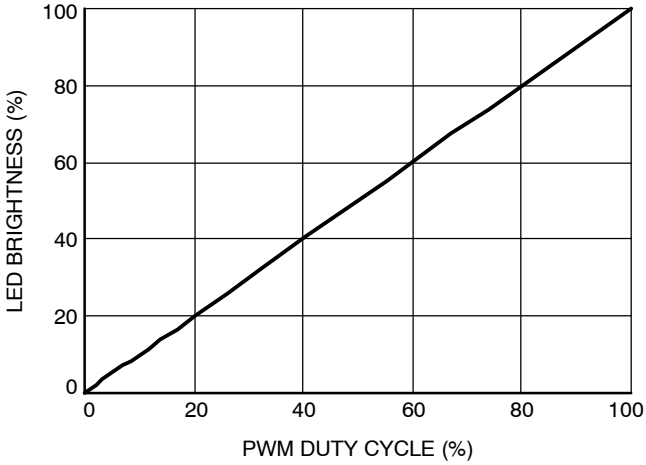


Figure 12. LED Brightness vs. PWM Duty Cycle

6. At initial power up, the CAT4026 will draw a higher quiescent current equal to the “dropout” current until it reaches normal regulation.

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{DD} = V_{PWM} = 5 V, V_{ANLG} = 3.3 V, T_{AMB} = 25°C unless otherwise specified.)

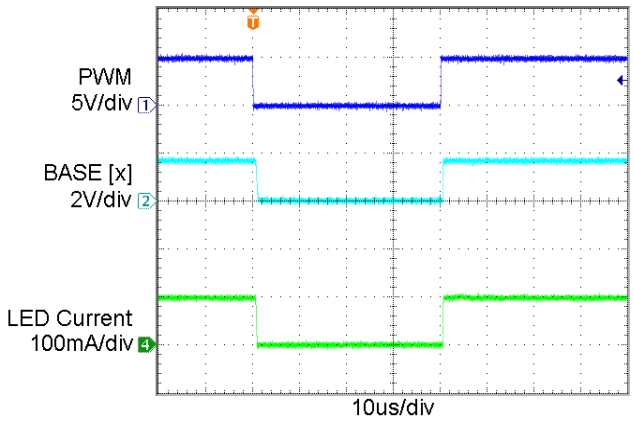


Figure 13. LED Current Transient During PWM Dimming

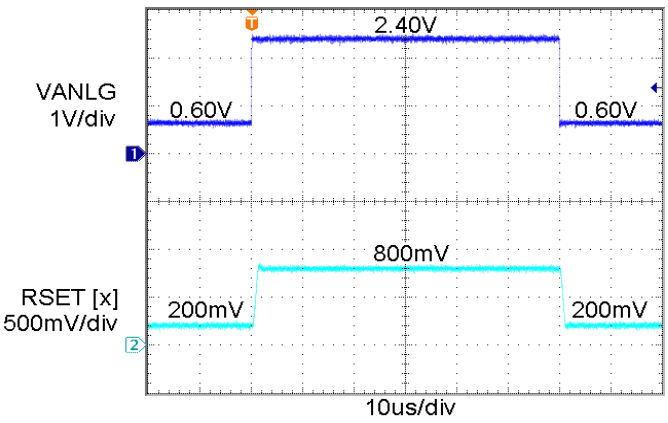


Figure 14. ANLG Transient, 20% to 80% Brightness

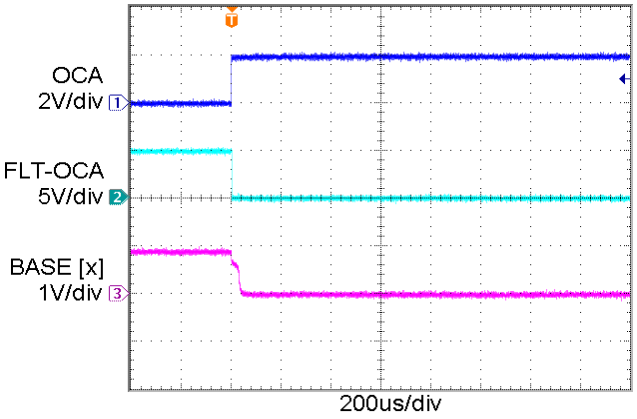


Figure 15. Open Cathode−Anode Waveform

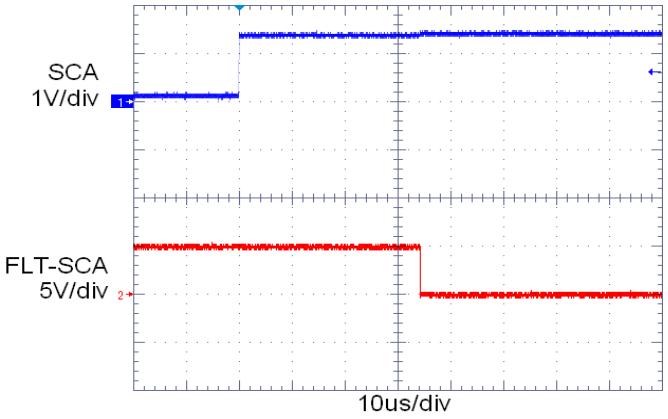


Figure 16. Short Cathode−Anode Waveform

Table 5. PIN DESCRIPTION

Pin #	Name	Function
1	VDD	Supply Bias voltage input for controller
2	PWM	Digital PWM input control to globally PWM all channels
3	ANLG	ANLG input bias signal to globally adjust full scale brightness. (intended for external power derating circuit for SCA conditions)
4, 6, 8, 21, 23, 25	BASE [1:6]	Base drive connection for external channel high voltage BJT
5, 7, 9, 20, 22, 24	RSET [1:6]	Current setting resistor for LED channel (Full Scale Brightness of 1 V)
10	OCA	Open Cathode Anode over−voltage threshold trigger input (sets maximum allowed LED Anode voltage, 1 V trigger)
11	C1	LED Anode capacitor
12	N.C.	Do not connect, leave floating
13	VA	Internal cathode reference voltage (divided by 2 and buffered to 1.8 V). Intended to provide reference bias for external circuitry, such as the power derating operational amplifier.
14	N.C.	Do not connect, leave floating
15	VC	Cathode voltage with compensation (divided by 2 and buffered). Leave floating if not used.
16	IFB	Current sink feedback (1 mA max) used with external circuit to control of LED Anode supply voltage
17	$\overline{\text{FLT−SCA}}$	Shorted Cathode−Anode Fault output logic signal (open−drain, active low) indicating presence of excessive cathode voltage
18	C3	Connect pin to GND
19	$\overline{\text{FLT−OCA}}$	Open Cathode−Anode Fault output logic signal (open−drain, active low) indicating an Open−channel condition
26	VCS	Lowest LED Cathode sense input (connect to sensing diode anodes)
27	SCA	Highest LED Cathode sense input (connect to external high voltage transistor and zener/diode network)
28	GND	Ground reference for all pins

Pin Functions

VDD

The VDD input is the positive supply to the devices. VDD should be nominally 5 V.

PWM

The PWM control input provides multiple functions. When the first rising edge is applied to PWM input, the CAT4026 will immediately power−up and remain powered up until the PWM input has been held low for at least typically 25 ms, at which point the device will enter full shutdown mode and draw zero current.

When PWM is active (high level), all LED channels are enabled. When PWM is inactive (low level), all LED channels are disabled. For PWM dimming frequencies in the 300 Hz range, duty cycles as low as 0.1% are supported.

An internal pull−down resistor (120 kΩ typical) exists on the PWM input. PWM logic high and low detection levels are typically set at 1.2 V and 1.0 V respectively.

ANLG

The ANLG controlled input allows the full scale brightness level of all channels to be globally reduced. When the ANLG control is taken below 3 V, the maximum LED brightness will be equal to 1/3 of the ANLG pin voltage. If the ANLG pin is taken above 3 V, it will have no further effect and the brightness will remain at the full scale (100%) setting.

An internal resistive network to ground (150 kΩ typical) exists on the ANLG pin. The external source resistance driving this input should be taken into consideration when controlling the ANLG input.

A simple power derating external circuit can be applied to the ANLG pin whenever excessive voltage is present on any LED cathode.

If the ANLG control function is not required, the pin should be pulled high (above 3 V) to ensure full scale brightness is maintained.

BASE[1:6]

The BASE output pin drives the base of the external NPNs to regulate the LED current in the associated string to the preset value. External high−voltage bipolar junction transistors, such as MJD340, are recommended.

Operating base currents up to 5 mA can be powered from each of the BASE pins in normal operating conditions. In the event of any BASE pin being shorted directly to GND, internal protection circuitry will limit the drive current to 15 mA (typically).

RSET[1:6]

The RSET input pins sense the voltage of the external LED current bias resistors. Each RSET pin is accurately regulated to a voltage of 1.0 V under the full scale brightness condition (ANLG > 3.0 V).

Each RSET pin contains internal compensating circuitry to eliminate the operating base current, thereby maintaining extremely accurate LED matching on all channels.

$\overline{\text{FLT−OCA}}$

The $\overline{\text{FLT−OCA}}$ flag output is active low (open−drain) and is latched whenever an Open Cathode−Anode fault condition has been detected on any LED string. An external pull−up resistor (10 kΩ) should be connected to $\overline{\text{FLT−OCA}}$.

For systems requiring complete shutdown upon detection of any open−LED channel, the $\overline{\text{FLT−OCA}}$ output can be used to drive the shutdown control of the LED power supply.

For systems which must continue operation under open−LED channels, the $\overline{\text{FLT−OCA}}$ should only be used for diagnostic purposes (not for system shutdown).

The $\overline{\text{FLT−OCA}}$ is cleared upon power−down of the CAT4026 device.

$\overline{\text{FLT−SCA}}$

The $\overline{\text{FLT−SCA}}$ flag output is active low (open−drain) and becomes active whenever any LED cathode terminal exceeds a user programmed voltage level (at the SCA pin, set by an external zener diode). An external pull−up resistor (10 kΩ) should be connected to the $\overline{\text{FLT−SCA}}$ pin.

For systems requiring complete shutdown upon detection of any faulty LED channel, the $\overline{\text{FLT−SCA}}$ output can be used to drive the shutdown control of the LED power supply.

For systems which must continue operation under faulty LED channels, the $\overline{\text{FLT−SCA}}$ should only be used for diagnostic purposes (not for system shutdown). In this case, the $\overline{\text{FLT−SCA}}$ flag can be used to trigger an external power derating circuit reducing the applied voltage at the ANLG control input, thereby reducing the power dissipated in the external bipolar channel transistors.

Note: If an Open−LED channel is present, the $\overline{\text{FLT−SCA}}$ flag may become temporary active (depending on the user threshold levels) while the system is diagnosing the Open−channel fault. When the system has eventually cleared (disabled) the open−channel, the fault $\overline{\text{FLT−SCA}}$ will automatically clear itself once the system has stabilized and returned back to normal operating conditions.

IFB

The IFB pin is a pull−down current sink with a drive level determined by the lowest LED cathode voltage as shown below.

VCS Voltage	IFB Drive Current (typ)
> 4.1 V	0 mA
3.3 V	0.5 mA
< 3.1 V	1.0 mA

VCS = Vcathode + Vdiode

External adjustment of LED Anode supply voltage is controlled by the IFB current sink in conjunction with an external feedback circuit. The external circuit should be configured so that 1 mA drive signal will achieve the desired necessary dynamic adjustment range for expected worst case maximum LED string operating voltage range

A linear transconductance relationship exists for the drive current (1 mA/V) for Cathode operation between 2.5 V and 3.5 V.

C1

Connect a capacitor of 1 nF and a 10 kΩ resistor from the C1 pin to the LED Anode voltage. Capacitor voltage rating must be greater than the highest LED anode voltage.

C3

Connect pin to GND.

SCA

The SCA pin is used to detect a severe mismatch in LED string voltage, such as the occurrence of an Anode−Cathode short. The SCA pin is connected to each LED cathode via a diode array and a voltage level translator. The threshold voltage of the detector can be adjusted by using an external Zener diode.

A conduction level of 1.5 mA into the SCA pin will trigger a FAULT condition. The FAULT condition will be cleared upon the conduction current level falling below 0.5 mA and normal operation will resume.

OCA

The OCA input is used to detect and protect against abnormally high LED Anode condition. An external resistive divider connected to the OCA pin, from the LED Anode voltage, will trigger a $\overline{\text{FLT−OCA}}$ condition once the OCA input level exceeds 1.0 V. Any open−LED channel will automatically be disabled and removed from the feedback loop when OCA is triggered. This method provides an auto−recovery feature for the system to resume normal operation ensuring only the ‘good’ LED channels are included in the feedback loop.

If the open−LED function is not used, the OCA pin should be tied to GND.

VCS

The VCS pin is connected to each LED cathode via a diode array. This pin detects the lowest LED cathode voltage and sets the feedback signaling to allow the SMPS to adjust the LED Anode voltage to the appropriate levels for optimum efficiency (3 V operating point for the minimum cathode voltage on any string). An external high voltage diode array such as BAS21LT is recommended.

VA

The VA output pin is optional and allows the user to power an external feedback control circuit for setting the common LED Anode operating voltage level.

This output is a buffered voltage signal, which tracks 50% of the internal reference being used to control and set the nominal operating level of the lowest LED Cathode string voltage. An internal source impedance of 250 Ω is present on this output and the nominal voltage is set to 1.8 V (thermal compensation exists to cancel out the external sensing diode temperature coefficient present on the VCS pin).

VC

The VC pin is a buffered voltage signal, which tracks 50% of the voltage level present at the VCS input pin (i.e. the VC voltage is determined by the lowest operating Cathode voltage present on any LED string).

This signal provides a convenient feedback control method for systems which use standalone converters to generate the LED Anode supply voltage (as opposed to a current feedback option). An external suitable resistive divider, at the VC pin, can be used to directly control the feedback input of the standalone converter.

During shutdown mode, the VC pin is forced into high impedance mode, while during normal operation an output source impedance of 360 Ω is present on the VC pin.

Simplified Block Diagram

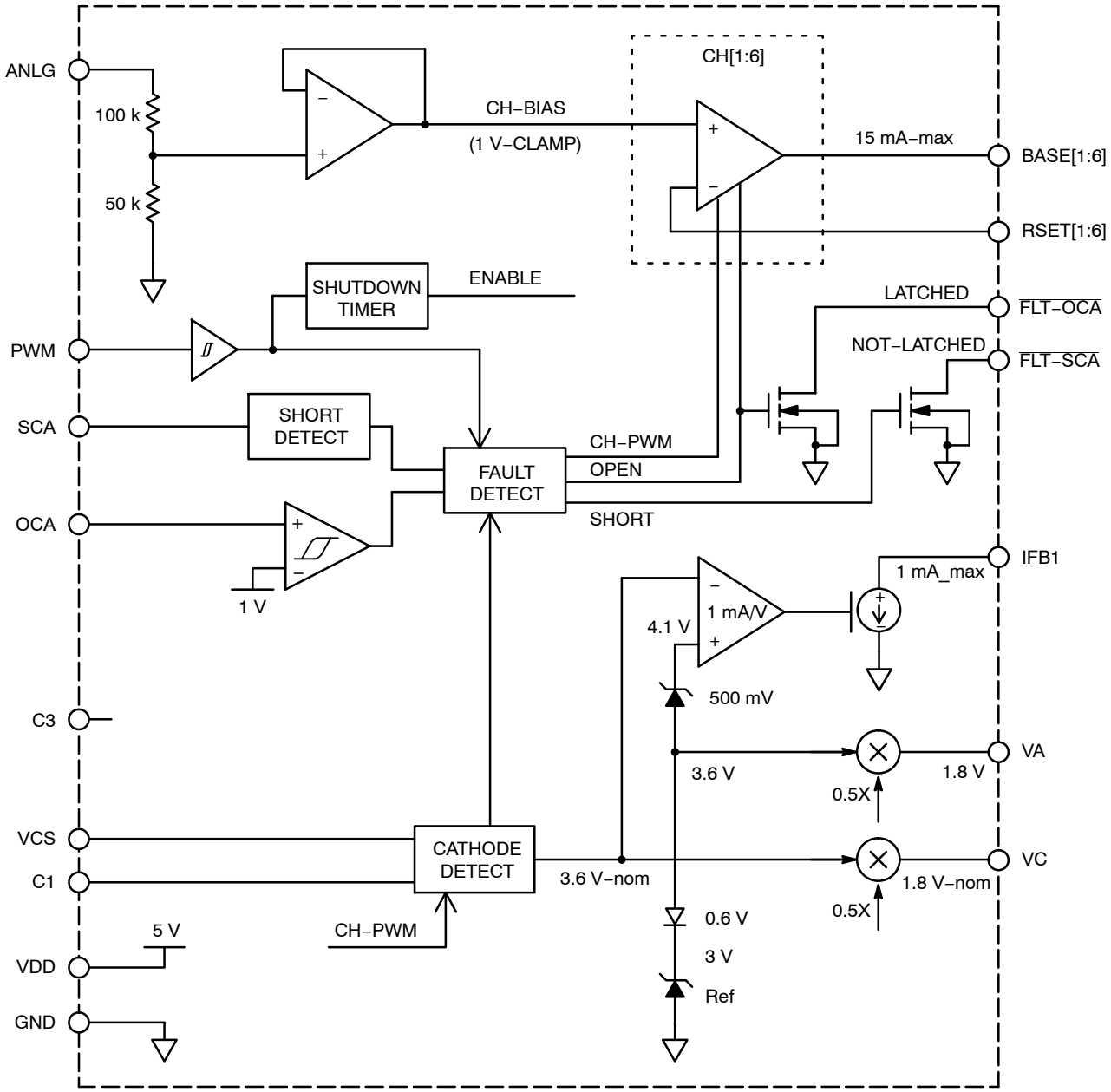


Figure 17. Simplified Block Diagram

APPLICATION INFORMATION

Operation with Open and Shorted LED

The CAT4026 can detect both open and shorted LED strings through two diode−OR circuits connected respectively to the VCS and SCA pins, as shown in the application circuit in Figure 1.

Open LED

When one of the channel becomes open or disconnected, its cathode voltage drops to zero pulled down by the current sensing resistor (R1−R6). The lowest cathode voltage is sensed through a diode at the VCS pin (VCS pin is around 0.6 V above the lowest cathode voltage). This causes the CAT4026 current feedback pin (IFB) current to increase to 1 mA and the power supply to increase the anode voltage VOUT until the OCA pin exceeds 1 V threshold and latches on the $\overline{\text{FLT−OCA}}$ fault (the pin is pulled low). At that time, the CAT4026 disables the open channel (corresponding BASE pin voltage goes to GND) and will ignore that channel until the driver is shutdown. The $\overline{\text{FLT−OCA}}$ pin remains low until the CAT4026 goes to shutdown mode or is powered down. The output voltage VOUT now returns to normal operation level where the lowest cathode voltage is around 3.2 V (VCS pin around 3.6 V). The anode voltage is sensed at the OCA pin through a resistor divider (Ra, Rb) as shown in Figure 21.

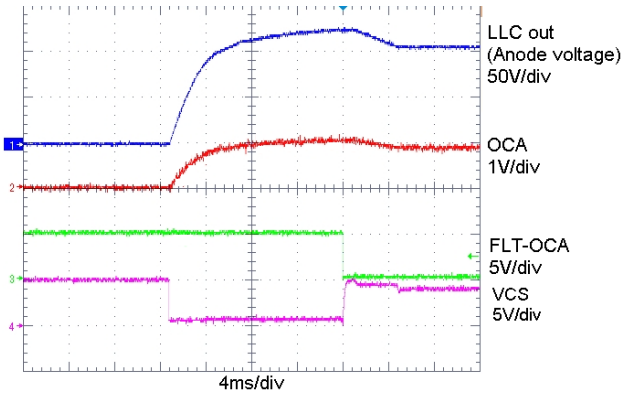


Figure 18. Open LED at Power−up

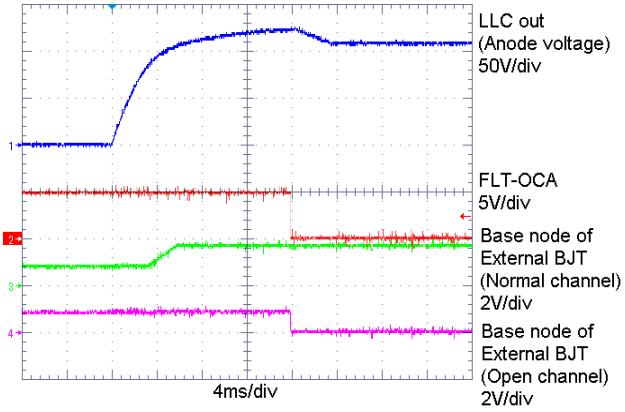


Figure 19. Open LED at Power−up, Base Voltages

Shorted LED

In some cases, the LED string voltage may be different between different strings (channel voltage mismatch). This can be due to LED forward voltage variation or some LEDs becoming shorted in one of the string. One of the string would have a total LED forward voltage lower than other channels. In operation, the cathode voltage of the “shorted” channel will be higher than the other channels causing more power to be dissipated in the external transistor of that channel. Therefore, it is useful to detect this condition and, if needed, derate the LED channel current. The highest cathode voltage is sensed at the SCA pin through a diode−OR network. A zener in series with the diodes, shown in Figure 21, allows to adjust the cathode threshold voltage. Once the SCA pin sinks more than about 1.3 mA, the $\overline{\text{FLT−SCA}}$ fault is triggered and the pin is pulled low. Figure 20 shows a power−up waveform for a threshold voltage at about 45 V. In this example, when the fault is triggered, the LED current decreases from 100 mA to 20 mA.

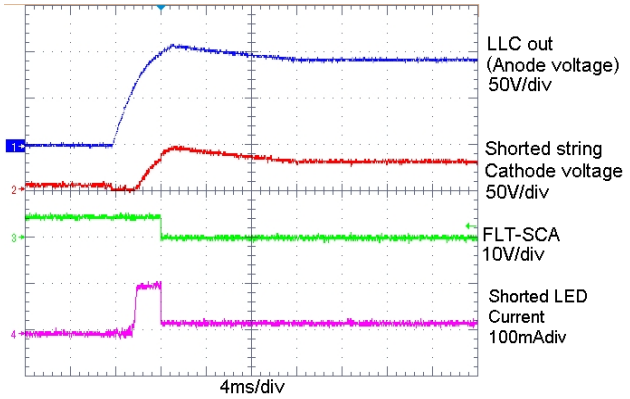


Figure 20. Shorted LED Channel at Power−up

Figure 21 shows a partial application schematic relative to the OCA and SCA fault detection.

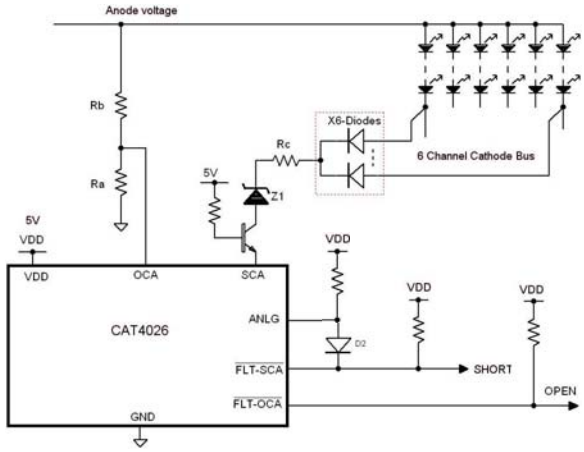


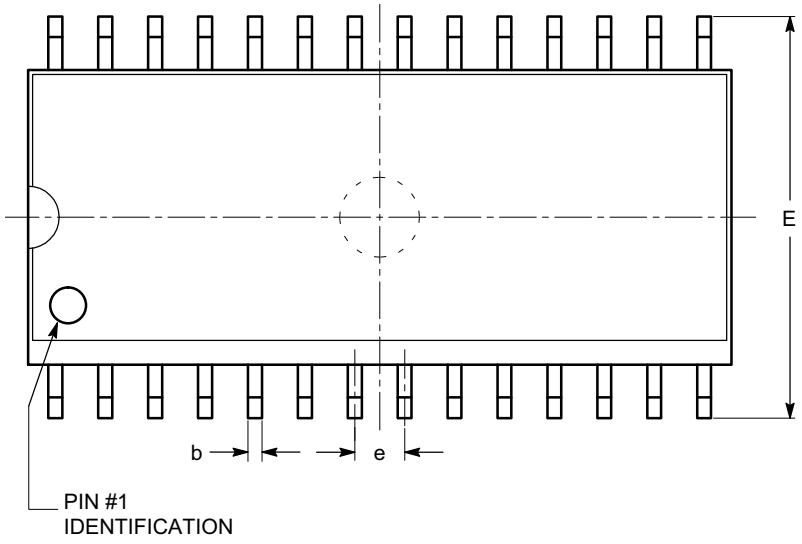
Figure 21. Schematic for Open/Short Detection

Unused LED Channels

For applications that require less than 6 LED channels, the unused channel BASE and RSET pins should be left floating. All the other used channels will operate normally.

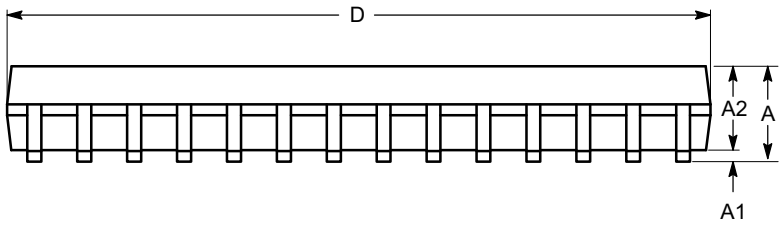
PACKAGE DIMENSIONS

SOIC−28, 300 mils
CASE 751BM−01
ISSUE O

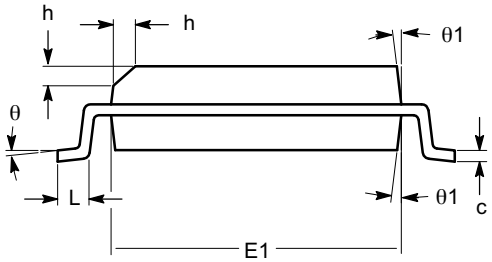


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	2.35		2.65
A1	0.10		0.30
A2	2.05		2.55
b	0.31		0.51
c	0.20		0.33
D	17.78		18.03
E	10.11		10.51
E1	7.34		7.60
e	1.27 BSC		
h	0.25		0.75
L	0.40		1.27
θ	0º		8º
θ1	5º		15º



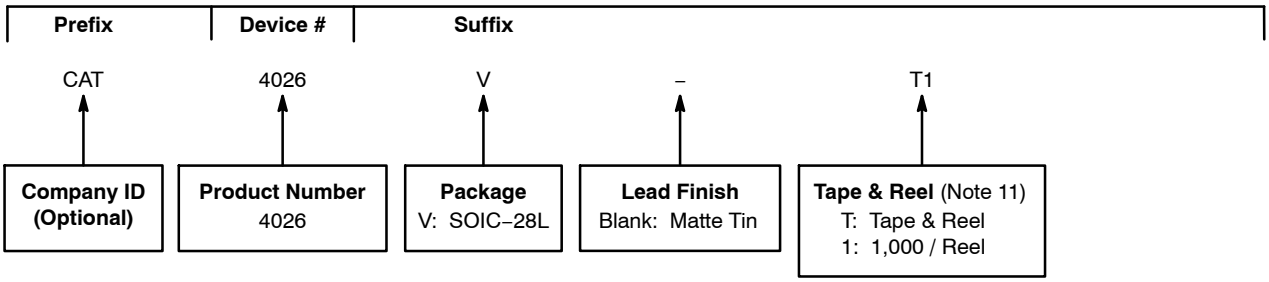
SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-013.

Example of Ordering Information (Note 9)



7. All packages are RoHS−compliant (Lead−free, Halogen−free).
8. The standard lead finish is Matte Tin.
9. The device used in the above example is a CAT4026V−T1 (SOIC−28L, Matte Tin, Tape & Reel, 1,000/Reel).
10. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
11. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PUBLICATION ORDERING INFORMATION

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