CAT521

8-Bit Digital POT With Independent Reference Inputs

FEATURES

- **Buffered Outputs**
- **Output settings retained without power**
- **Output range includes both supply rails**
- **Programming voltage generated on-chip**
- **Serial µP interface**
- **Single supply operation: 2.7V-5.5V**

APPLICATIONS

- **Automated product calibration.**
- **Remote control adjustment of equipment**
- **Offset, gain and zero adjustments in Self-Calibrating and Adaptive Control systems.**
- **Tamper-proof calibrations.**

DESCRIPTION

The CAT521 is a dual 8-Bit Memory DAC designed as an electronic replacement for mechanical potentiometers and trim pots. Intended for final calibration of products such as camcorders, fax machines and cellular telephones on automated high volume production lines and systems capable of self calibration, it is also well suited for applications were equipment requiring periodic adjustment is either difficult to access or located in a hazardous environment.

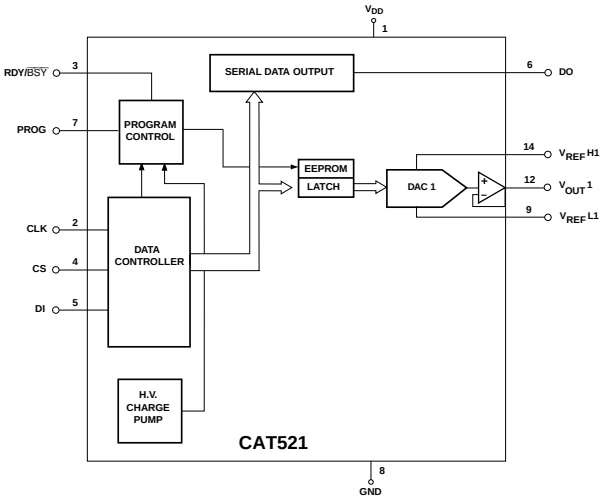
The CAT521 consists of a programmable DAC with independent high and low reference inputs and is capable of a rail to rail output swing. The output is buffered by a rail to rail OP AMP. Output settings, stored in non-volatile EEPROM memory, are not lost when the device is powered down and are automatically reinstated when power is returned. The output can be dithered to test new output values without effecting the stored settings and stored settings can be read back without disturbing the DAC's output.

Control of the CAT521 is accomplished with a simple 3 wire serial interface. A Chip Select pin allows several CAT521's to share a common serial interface and communications back to the host controller is via a single serial data line thanks to the CAT521's Tri-Stated Data Output pin. A RDY/$\overline{BSY}$ output working in concert with an internal low voltage detector signals proper operation of EEPROM Erase/Write cycle.

The CAT521 operates from a single 3–5 volt power supply. The high voltage required for EEPROM Erase/Write operations is generated on-chip.

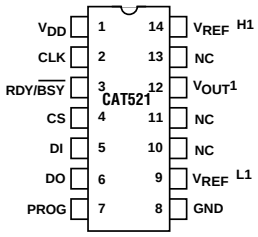
The CAT521 is available in the 0°C to 70°C Commercial and –40°C to +85°C Industrial operating temperature ranges and offered in 14-pin plastic DIP and Surface mount packages.

FUNCTIONAL DIAGRAM

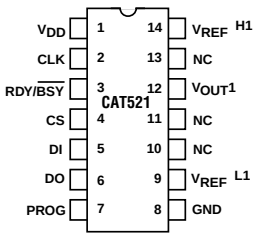


PIN CONFIGURATION

DIP Package (P)



SOIC Package (J)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage*
- V_{DD} to GND ..... –0.5V to +7V

Inputs
- CLK to GND ..... –0.5V to V_{DD} +0.5V
- CS to GND ..... –0.5V to V_{DD} +0.5V
- DI to GND ..... –0.5V to V_{DD} +0.5V
- RDY/BSY to GND ..... –0.5V to V_{DD} +0.5V
- PROG to GND ..... –0.5V to V_{DD} +0.5V
- $V_{REF}H$ to GND ..... –0.5V to V_{DD} +0.5V
- $V_{REF}L$ to GND ..... –0.5V to V_{DD} +0.5V

Outputs
- D_0 to GND ..... –0.5V to V_{DD} +0.5V
- V_{OUT} 1– 2 to GND ..... –0.5V to V_{DD} +0.5V

Operating Ambient Temperature
- Commercial ('C' suffix) ..... 0°C to +70°C
- Industrial ('I' suffix) ..... – 40°C to +85°C

Junction Temperature ..... +150°C
Storage Temperature ..... –65°C to +150°C
Lead Soldering (10 sec max) ..... +300°C

* Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Absolute Maximum Ratings are limited values applied individually while other parameters are within specified operating conditions, and functional operation at any of these conditions is NOT implied. Device performance and reliability may be impaired by exposure to absolute rating conditions for extended periods of time.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Method
V_{ZAP}(1)	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I_{LTH}(1)(2)	Latch-Up	100		mA	JEDEC Standard 17

NOTES: 1. This parameter is tested initially and after a design or process change that affects the parameter.
2. Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V.

DC ELECTRICAL CHARACTERISTICS: V_{DD} = +2.7V to +5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Resolution		8	—	—	Bits
Accuracy						
INL	Integral Linearity Error	I_{LOAD} = 10 µA, T_R = C	—	0.6	± 1	LSB
		T_R = I	—	0.6	± 1	LSB
		I_{LOAD} = 40 µA, T_R = C	—	1.2	—	LSB
		T_R = I	—	1.2	—	LSB
DNL	Differential Linearity Error	I_{LOAD} = 10 µA, T_R = C	—	0.25	± 0.5	LSB
		T_R = I	—	0.25	± 0.5	LSB
		I_{LOAD} = 40 µA, T_R = C	—	0.5	—	LSB
		T_R = I	—	0.5	—	LSB
Logic Inputs						
I_{IH}	Input Leakage Current	$V_{IN} = V_{DD}$	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	–10	µA
V_{IH}	High Level Input Voltage		2	—	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	—	0.8	V
References						
V_{RH}	$V_{REF}H$ Input Voltage Range		2.7	—	V_{DD}	V
V_{RL}	$V_{REF}L$ Input Voltage Range		GND	—	V_{DD} -2.7	V
Z_{IN}	$V_{REF}H$–$V_{REF}L$ Resistance		—	28K	—	Ω
Logic Outputs						
V_{OH}	High Level Output Voltage	I_{OH} = – 40 µA	V_{DD} –0.3	—	—	V
V_{OL}	Low Level Output Voltage	I_{OL} = 1 mA, V_{DD} = +5V	—	—	0.4	V
		I_{OL} = 0.4 mA, V_{DD} = +3V	—	—	0.4	V

DC ELECTRICAL CHARACTERISTICS (Cont.)**:**
V_{DD} = +2.7V to +5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

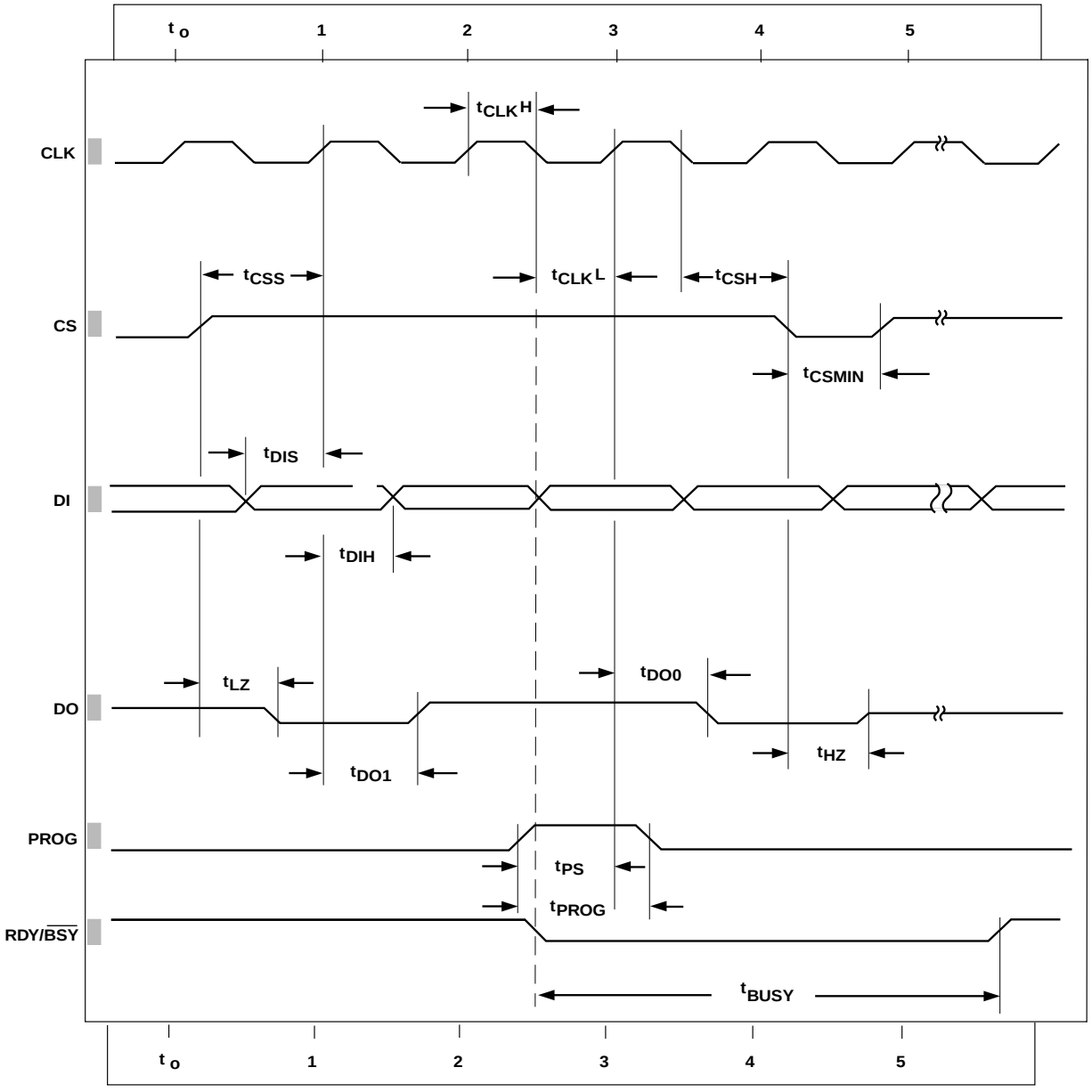
Symbol	Parameter	Conditions	Min	Typ	Max	Units
Analog Output						
FSO	Full-Scale Output Voltage	$V_R = V_{REF}H - V_{REF}L$	0.99 V_R	0.995 V_R	—	V
ZSO	Zero-Scale Output Voltage	$V_R = V_{REF}H - V_{REF}L$	—	0.005 V_R	0.01 V_R	V
I_L	DAC Output Load Current		—	—	1	µA
R_{OUT}	DAC Output Impedance	$V_{DD} = V_{REF}H$ = +5V	—	—	1K	Ω
		$V_{DD} = V_{REF}H$ = +3V	—	—	1K	Ω
PSSR	Power Supply Rejection	I_{LOAD} = 1 µA	—	—	1	LSB / V
Temperature						
TC_O	V_{OUT} Temperature Coefficient	V_{DD} = +5V, I_{LOAD} = 250nA	—	—	200	µV/ °C
		$V_{REF}H$= +5V, $V_{REF}L$ = 0V				
TC_{REF}	Temperature Coefficient of V_{REF} Resistance	$V_{REF}H$ to $V_{REF}L$	—	700	—	ppm / °C
Power Supply						
I_{DD1}	Supply Current (Read)	Normal Operating	—	0.4	0.6	mA
I_{DD2}	Supply Current (Write)	Programming, V_{DD} = 5V	—	1.6	2.5	mA
		V_{DD} = 3V	—	1.0	1.6	mA
V_{DD}	Operating Voltage Range		2.7	—	5.5	V

AC ELECTRICAL CHARACTERISTICS:
V_{DD} = +2.7V to +5.5V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital						
t_{CSMIN}	Minimum CS Low Time		150	—	—	ns
t_{CSS}	CS Setup Time		100	—	—	ns
t_{CSH}	CS Hold Time	C_L = 100 pF, see note 1	0	—	—	ns
t_{DIS}	DI Setup Time		50	—	—	ns
t_{DIH}	DI Hold Time		50	—	—	ns
t_{DO1}	Output Delay to 1		—	—	150	ns
t_{DO0}	Output Delay to 0		—	—	150	ns
t_{HZ}	Output Delay to High-Z		—	400	—	ns
t_{LZ}	Output Delay to Low-Z		—	400	—	ns
t_{BUSY}	Erase/Write Cycle Time		—	4	5	ms
t_{PS}	PROG Setup Time		150	—	—	ns
t_{PROG}	Minimum Pulse Width		700	—	—	ns
$t_{CLK}H$	Minimum CLK High Time		500	—	—	ns
$t_{CLK}L$	Minimum CLK Low Time		300	—	—	ns
f_C	Clock Frequency		DC	—	1	MHz
Analog						
t_{DS}	DAC Settling Time to 1 LSB	C_{LOAD} = 10 pF, V_{DD} = +5V	—	3	10	µs
		C_{LOAD} = 10 pF, V_{DD} = +3V	—	6	10	µs
Pin Capacitance						
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1 MHz(2)	—	8	—	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V, f = 1 MHz(2)	—	6	—	pF

NOTES: 1. All timing measurements are defined at the point of signal crossing V_{DD} / 2.
2. These parameters are periodically sampled and are not 100% tested.

A. C. TIMING DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
1	V_{DD}	Power supply positive
2	CLK	Clock input pin
3	RDY/$\overline{BSY}$	Ready/Busy output
4	CS	Chip select
5	DI	Serial data input pin
6	DO	Serial data output pin
7	PROG	EEPROM Programming Enable Input
8	GND	Power supply ground
9	$V_{REF}L1$	Minimum DAC 1 output voltage
10	NC	No Connect
11	NC	No Connect
12	$V_{OUT}1$	DAC 1 output
13	NC	No Connect
14	$V_{REF}H1$	Maximum DAC 1 output voltage

DAC addressing is as follows:

DAC OUTPUT	A0	A1
$V_{OUT}1$	0	1

DEVICE OPERATION

The CAT521 is a single 8-bit Digital to Analog Converter (DAC) whose output can be programmed to any one of 256 individual voltage steps. Once programmed, the output setting is retained in non-volatile EEPROM memory and will not be lost when power is removed from the chip. Upon power up the DAC returns to the setting stored in EEPROM memory. The DAC can be written to and read from without effecting the output voltage during the read or write cycle. The output can also be adjusted without altering the stored output setting, which is useful for testing new output settings before storing them in memory.

DIGITAL INTERFACE

The CAT521 employs a standard 3 wire serial control interface consisting of Clock (CLK), Chip Select (CS) and Data In (DI) inputs. For all operations, address and data are shifted in LSB first. In addition, all digital data must be preceded by a logic “1” as a start bit. The DAC address and data are clocked into the DI pin on the clock’s rising edge. When sending multiple blocks of information a minimum of two clock cycles is required between the last block sent and the next start bit.

Multiple devices may share a common input data line by selectively activating the CS control of the desired IC. Data Outputs (DO) can also share a common line because the DO pin is Tri-Stated and returns to a high impedance when not in use.

CHIP SELECT

Chip Select (CS) enables and disables the CAT521’s read and write operations. When CS is high data may be read to or from the chip, and the Data Output (DO) pin is active. Data loaded into the DAC control register will remain in effect until CS goes low. Bringing CS to a logic low returns all DAC outputs to the settings stored in EEPROM memory and switches DO to its high impedance Tri-State mode.

Because CS functions like a reset the CS pin has been desensitized with a 30 ns to 90 ns filter circuit to prevent noise spikes from causing unwanted resets and the loss of volatile data.

CLOCK

The CAT521’s clock controls both data flow in and out of the device and EEPROM memory cell programming. Serial data is shifted into the DI pin and out of the DO pin on the clock’s rising edge. While it is not necessary for the clock to be running between data transfers, the clock must be operating in order to write to EEPROM memory, even though the data being saved may already be resident in the DAC control register.

No clock is necessary upon system power-up. The CAT521’s internal power-on reset circuitry loads data from EEPROM to the DAC without using the external clock.

As data transfers are edge triggered clean clock transitions are necessary to avoid falsely clocking data into the control register. Standard CMOS and TTL logic families work well in this regard and it is recommended that any mechanical switches used for breadboarding or device evaluation purposes be debounced by a flip-flop or other suitable debouncing circuit.

V_{REF}

V_{REF}, the voltage applied between pins $V_{REF}H$ &$V_{REF}L$, sets the DAC's Zero to Full Scale output range where $V_{REF}L$ = Zero and $V_{REF}H$ = Full Scale. V_{REF} can span the full power supply range or just a fraction of it. In typical applications $V_{REF}H$ &$V_{REF}L$ are connected across the power supply rails. When using less than the full supply voltage be mindfull of the limits placed on $V_{REF}H$ and $V_{REF}L$ as specified in the References section of DC Electrical Characteristics.

READY/$\overline{BUSY}$

When saving data to non-volatile EEPROM memory, the Ready/Busy ouput (RDY/$\overline{BSY}$) signals the start and duration of the EEPROM erase/write cycle. Upon receiving a command to store data (PROG goes high) RDY/$\overline{BSY}$ goes low and remains low until the programming cycle is complete. During this time the CAT521 will ignore any data appearing at DI and no data will be output on DO.

RDY/$\overline{BSY}$ is internally ANDed with a low voltage detector circuit monitoring V_{DD}. If V_{DD} is below the minimum value required for EEPROM programming, RDY/$\overline{BSY}$ will remain high following the program command indicating a failure to record the desired data in non-volatile memory.

DATA OUTPUT

Data is output serially by the CAT521, LSB first, via the Data Out (DO) pin following the reception of a start bit and two address bits by the Data Input (DI). DO becomes active whenever CS goes high and resumes its high impedance Tri-State mode when CS returns low. Tri-Stating the DO pin allows several 521s to share a single serial data line and simplifies interfacing multiple 521s to a microprocessor.

WRITING TO MEMORY

Programming the CAT521's EEPROM memory is accomplished through the control signals: Chip Select (CS) and Program (PROG). With CS high, a start bit followed by a two bit DAC address and eight data bits are clocked into the DAC control register via the DI pin. Data enters on the clock's rising edge. The DAC output changes to its new setting on the clock cycle following D7, the last data bit.

Programming is accomplished by bringing PROG high sometime after the start bit and at least 150 ns prior to the rising edge of the clock cycle immediately following the D7 bit. Two clock cycles after the D7 bit the DAC control register will be ready to receive the next set of address and data bits. The clock must be kept running throughout the programming cycle. Internal control circuitry takes care of generating and ramping up the programming voltage for data transfer to the EEPROM cells. The CAT521's EEPROM memory cells will endure over 1,000,000 write cycles and will retain data for a minimum of 100 years without being refreshed.

READING DATA

Each time data is transferred into the DAC control register currently held data is shifted out via the D0 pin, thus in every data transaction a read cycle occurs. Note, however, that the reading process is destructive. Data must be removed from the register in order to be read. Figure 2 depicts a Read Only cycle in which no change occurs in the DAC's output. This feature allows µPs to poll DACs for their current setting without disturbing the output voltage but it assumes that the setting being read is also stored in EEPROM so that it can be restored at the end of the read cycle. In Figure 2 CS returns low before the 13th clock cycle completes. In doing so the EEPROM's

Figure 1. Writing to Memory

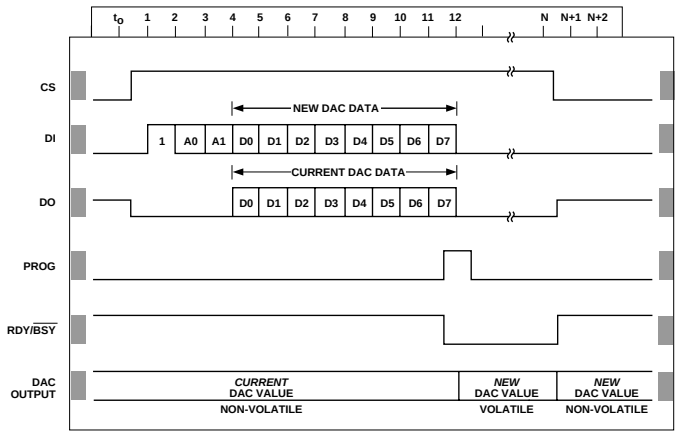
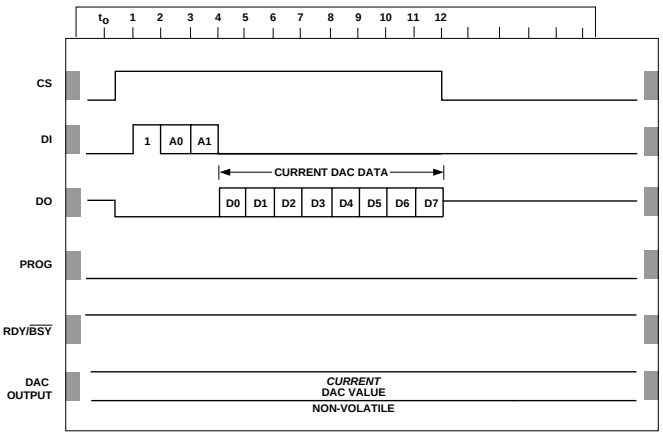


Figure 2. Reading from Memory



setting is reloaded into the DAC control register. Since this value is the same as that which had been there previously no change in the DAC's output is noticed. Had the value held in the control register been different from that stored in EEPROM then *a change would occur* at the read cycle's conclusion.

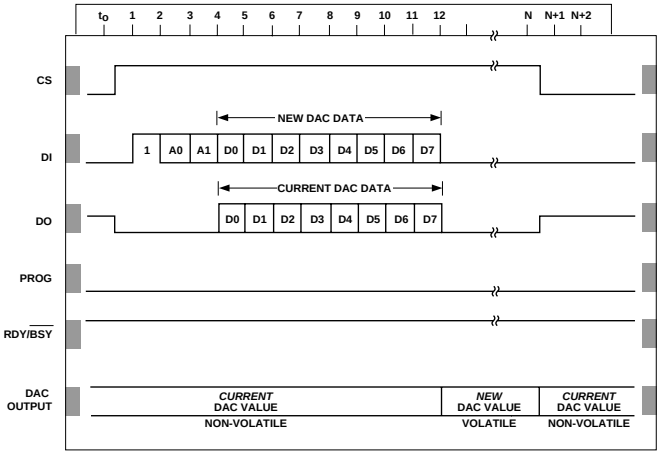
TEMPORARILY CHANGE OUTPUT

The CAT521 allows temporary changes in the DAC's output to be made without disturbing the settings retained in EEPROM memory. This feature is particularly useful when testing for a new output setting and allows for user adjustment of preset or default values without losing the original factory settings.

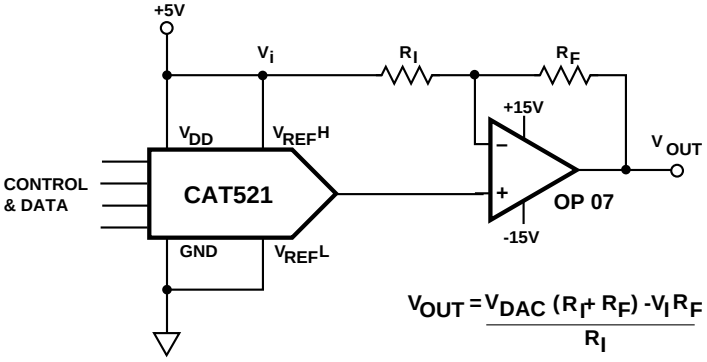
Figure 3 shows the control and data signals needed to effect a temporary output change. DAC settings may be changed as many times as required. The temporary setting remains in effect long as CS remains high. When CS returns low the DAC will return to the output value stored in EEPROM memory.

When it is desired to save a new setting acquired using this feature, the new value must be reloaded into the DAC control register prior to programming. This is because the CAT521's internal control circuitry discards from the programming register the new data two clock cycles after receiving it if no PROG signal is received.

Figure 3. Temporary Change in Output



APPLICATION CIRCUITS



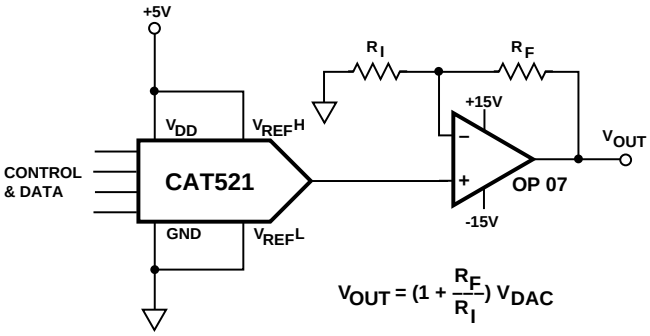
$$V_{OUT} = \frac{V_{DAC}(R_I + R_F) - V_I R_F}{R_I}$$

For $R_I = R_F$

$V_{OUT} = 2V_{DAC} - V_I$

DAC INPUT MSB	DAC INPUT LSB	DAC OUTPUT $V_{DAC} = \frac{CODE}{255}(V_{FS} - V_{ZERO}) + V_{ZERO}$ $V_{FS} = 0.99\ V_{REF}$ $V_{ZERO} = 0.01\ V_{REF}$	ANALOG OUTPUT $V_{REF} = 5V$ $R_I = R_F$
1111	1111	$\frac{255}{255}(.98\ V_{REF}) + .01\ V_{REF} = .990\ V_{REF}$	$V_{OUT} = +4.90V$
1000	0000	$\frac{128}{255}(.98\ V_{REF}) + .01\ V_{REF} = .502\ V_{REF}$	$V_{OUT} = +0.02V$
0111	1111	$\frac{127}{255}(.98\ V_{REF}) + .01\ V_{REF} = .498\ V_{REF}$	$V_{OUT} = -0.02V$
0000	0001	$\frac{1}{255}(.98\ V_{REF}) + .01\ V_{REF} = .014\ V_{REF}$	$V_{OUT} = -4.86V$
0000	0000	$\frac{0}{255}(.98\ V_{REF}) + .01\ V_{REF} = .010\ V_{REF}$	$V_{OUT} = -4.90V$

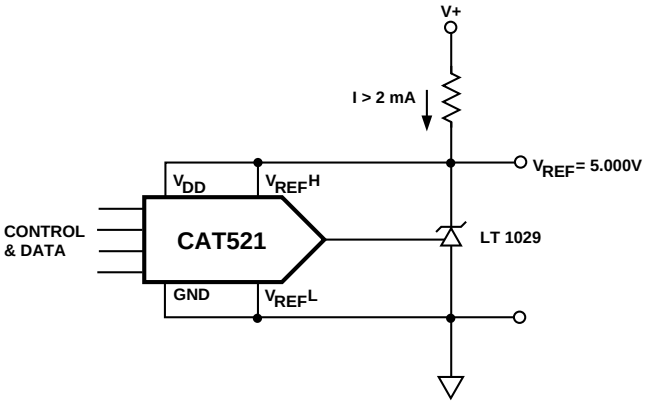
Bipolar DAC Output



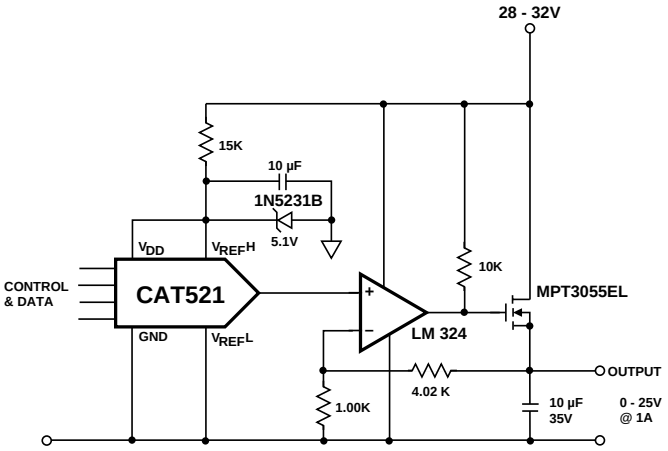
$$V_{OUT} = \left(1 + \frac{R_F}{R_I}\right) V_{DAC}$$

Amplified DAC Output

APPLICATION CIRCUITS (Cont.)

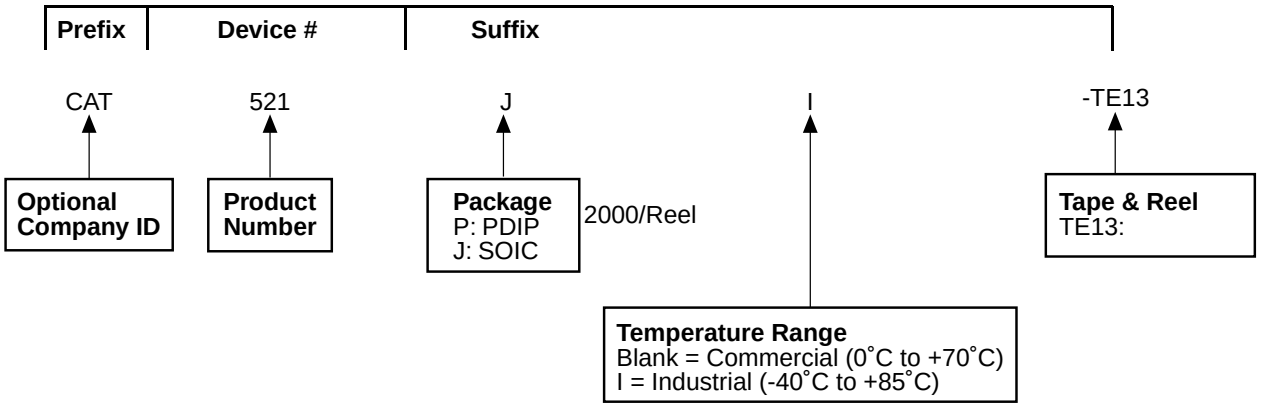


Digitally Trimmed Voltage Reference



Digitally Controlled Voltage Reference

ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT521JI-TE13 (SOIC, Industrial Temperature, Tape & Reel)