T-46-13-27

CAT59C11H - High Endurance
1K BIT SERIAL E²PROM

Preliminary

DESCRIPTION

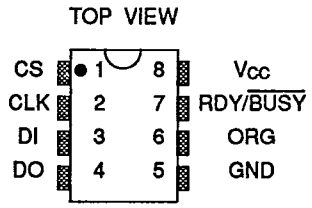
The CAT59C11H is a high endurance 1K bit Serial E²PROM memory device organized in 64 registers of 16 bits or 128 registers of 8 bits each. Each register can be written (or read) serially by using the DI (or DO) pin. The CAT59C11H is manufactured using Catalyst's advanced CMOS E²PROM floating gate technology. It is designed to endure 100,000 erase/write cycles and has a data retention of 100 years. It is packaged in an 8-pin DIP and Small Outline packages. To be offered in a 3V version (CAT33C201H).

FEATURES

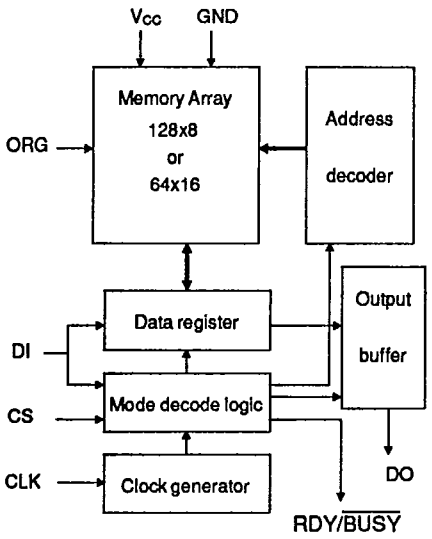
- Highly reliable CMOS floating gate technology
- Single 5V supply
- 64x16 or 128x8 user selectable serial memory
- Compatible with General Instruments ER5911
- Self timed programming cycle with Autoerase
- Word and chip erasable
- Operating range 0°C to 70°C
- 100,000 erase/write cycles
- 100 year data retention
- Power-up inadvertent write protection

E 3

PIN CONFIGURATION



BLOCK DIAGRAM



PIN FUNCTIONS

CS	Chip select
CLK	Clock input
DI	Serial data input
DO	Serial data output
Vcc	+5V power supply
RDY/BUSY	Status output
GND	Ground
ORG	Memory organization

Note: When the ORG pin is connected to Vcc, the 64x16 organization is selected. When it is connected to ground, the 128x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the 64x16 organization.

ABSOLUTE MAXIMUM RATINGS *

Storage temperature . . . . . -65°C to +150°C
Power supply (V_{CC}) . . . . . +7V
Voltage on any input pin . . . . . -0.3 to +7V
Voltage on any output pin . . . . . -0.3V to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
I_{CC1}	Current consumption (operating)	DI=0.0V, SK=5.5V V_{CC} =5.5V, CS = 5.5V DO unloaded			5	mA
I_{CC2}	Current consumption (standby)	V_{CC} = 5.5V, CS = 0 DI = 0, SK = 0			100	µA
I_{LI}	Input leakage current	V_{IN} = 5.5V			10	µA
I_{LO}	Output leakage current	V_{OUT} = 5.5V, CS = 0			10	µA
V_{IH}	High level input voltage		2.0		V_{CC} +1	V
V_{IL}	Low level input voltage		-0.1		0.8	V
V_{OH}	High level output voltage	I_{OH} = -400µA	2.4			V
V_{OL}	Low level output voltage	I_{OL} = 2.1mA			0.4	V

INSTRUCTION SET

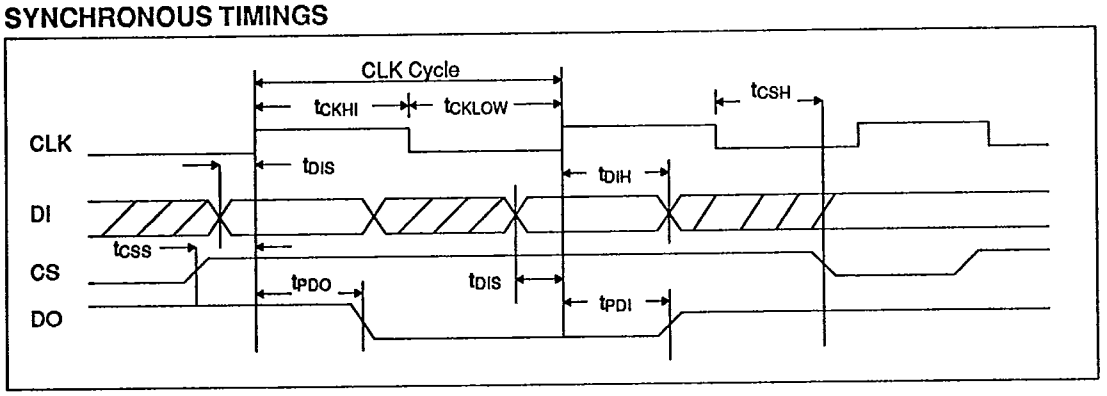
Instruction	Start Bit	Opcode	Address 128 x 8	Address 64 x 16	Data 128 x 8	Data 64 x 16	Comments
READ	1	1000	A_6 - A_0	A_5 - A_0			Read address A_N - A_0
PROGRAM	1	X100	A_6 - A_0	A_5 - A_0	D_7 - D_0	D_{15} - D_0	Program address A_N - A_0
PEN	1	0011	0000000	000000			Program enable
PDS	1	0000	0000000	000000			Program disable
ERAL	1	0010	0000000	000000			Erase all addresses
WRAL	1	0001	0000000	000000	D_7 - D_0	D_{15} - D_0	Write all addresses

AC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to 70°C)

Symbol	Parameter	Conditions	Limits Min.	Typ.	Max.	Unit
t_{CSS}	CS setup time		0.2			µs
t_{CSH}	CS hold time	C_L = 100pF V_{OL} = 0.8V, V_{OH} = 2.0V V_{IL} = 0.45V, V_{IH} = 2.4V	100			ns
t_{DIS}	DI setup time		0.4			µs
t_{DIH}	DI hold time		0.4			µs
t_{PD1}	Output delay to 1				2	µs
t_{PD0}	Output delay to 0				2	µs
t_{EW}	Erase/Write pulse width				10	ms
t_{SKHI}	Minimum SK high time		1			µs
t_{SKLOW}	Minimum SK low time		1			µs
CK_{MAX}	Maximum clock frequency		DC		250	kHz

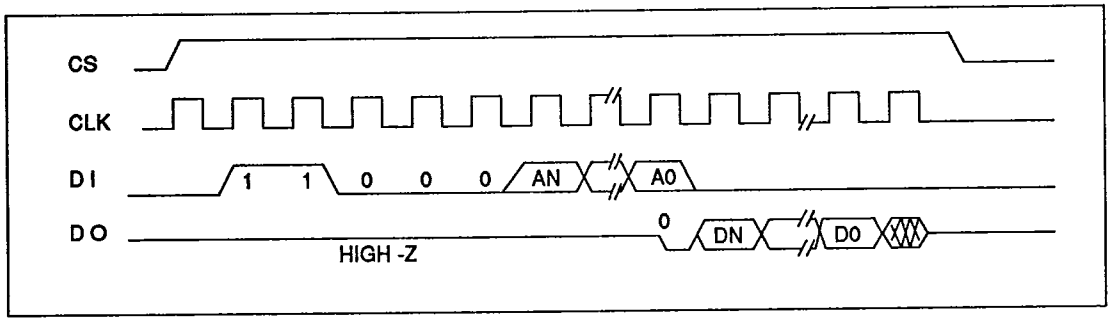
SYNCHRONOUS TIMINGS



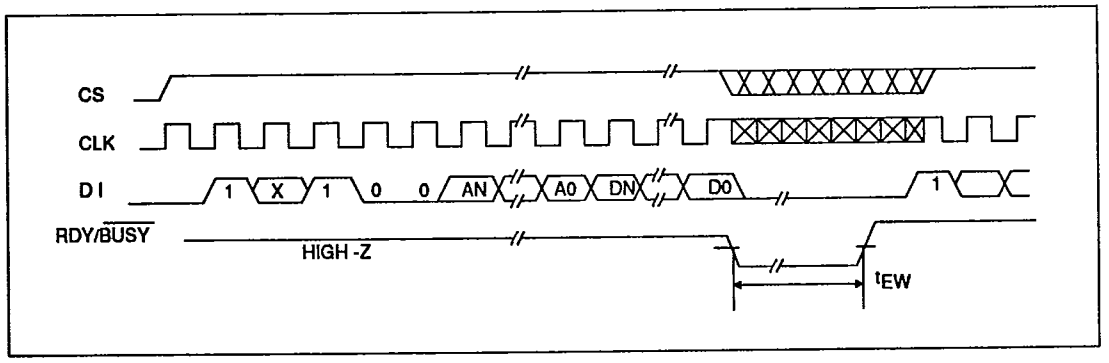
INSTRUCTION TIMING <ORGANIZATION>

Organization	A_N (or AN)	D_N (or DN)
128 x 8	A_6	D_7
64 x 16	A_5	D_{15}

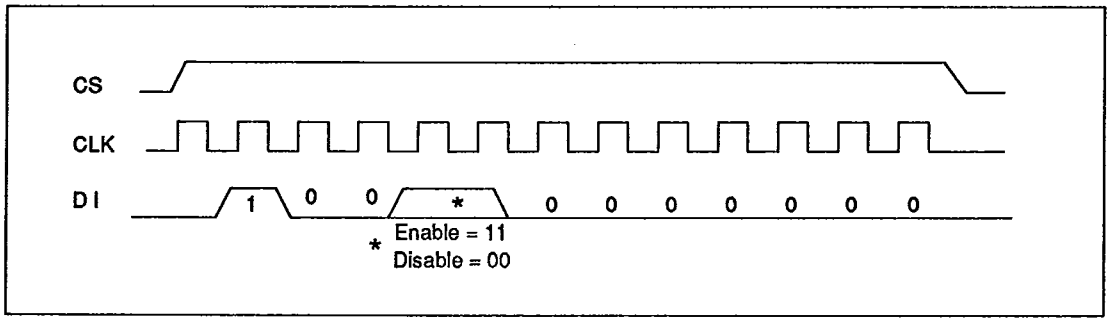
INSTRUCTION TIMING <READ>



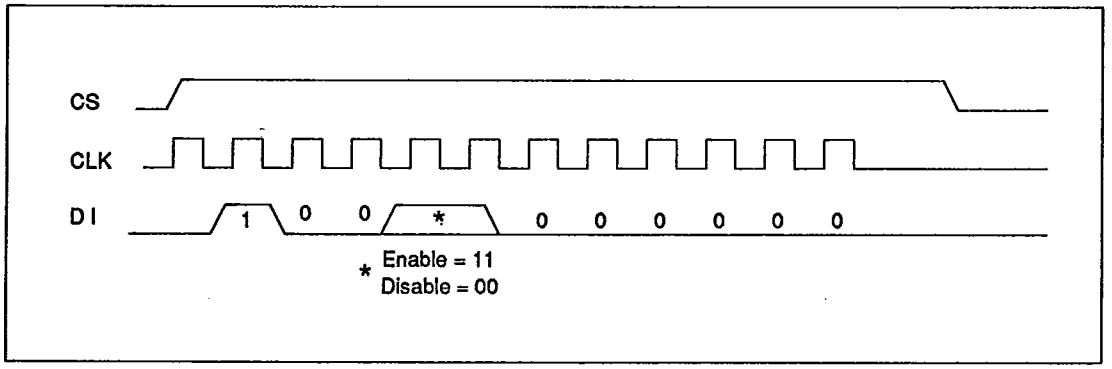
INSTRUCTION TIMING <PROGRAM>



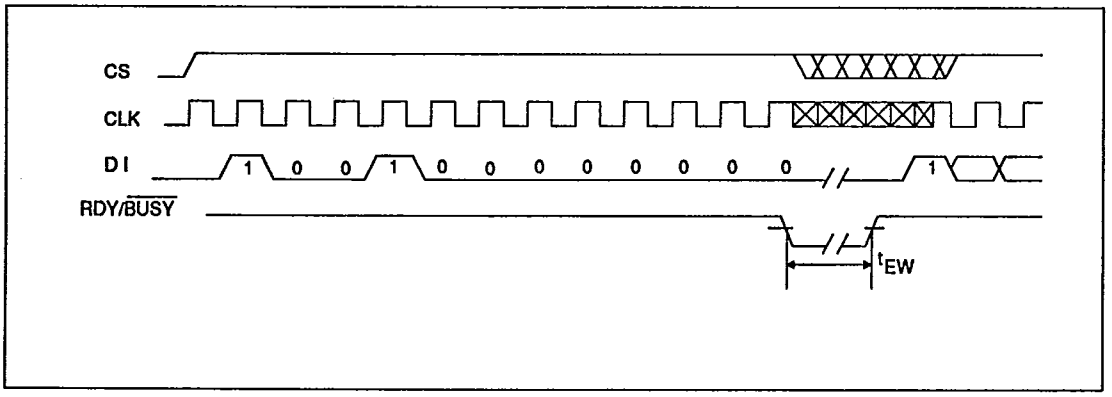
INSTRUCTION TIMING <PEN, PDS 128 x 8 organization>



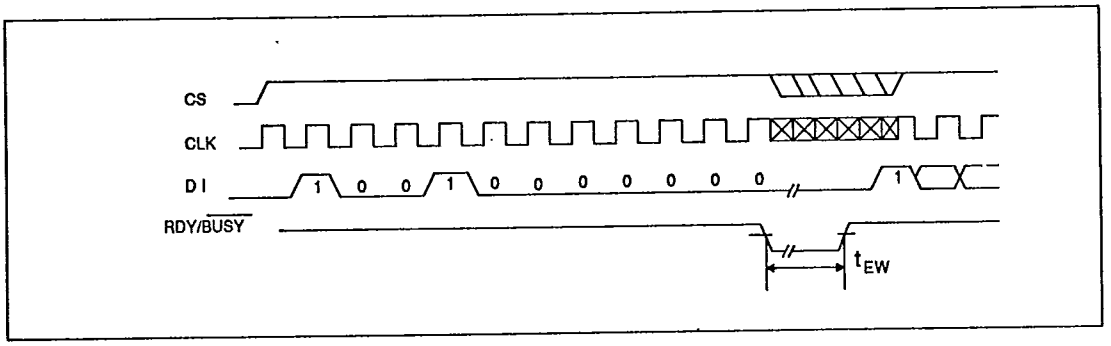
INSTRUCTION TIMING <PEN, PDS 64 x 16 organization>



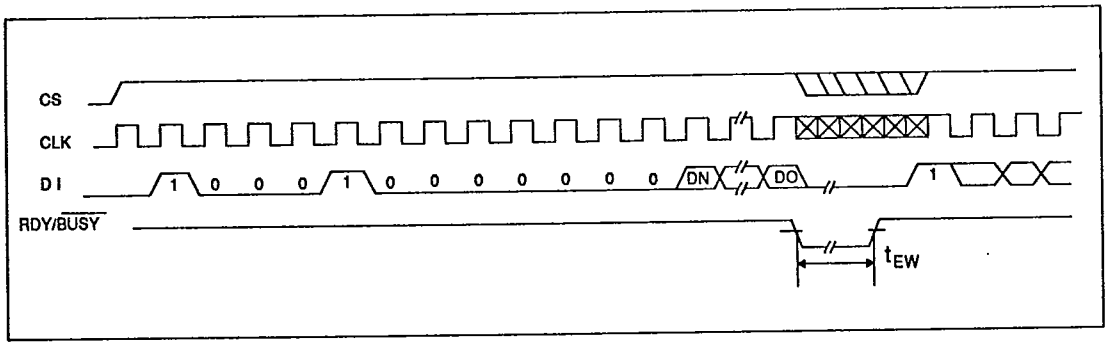
INSTRUCTION TIMING <ERAL 128 x 8 organization>



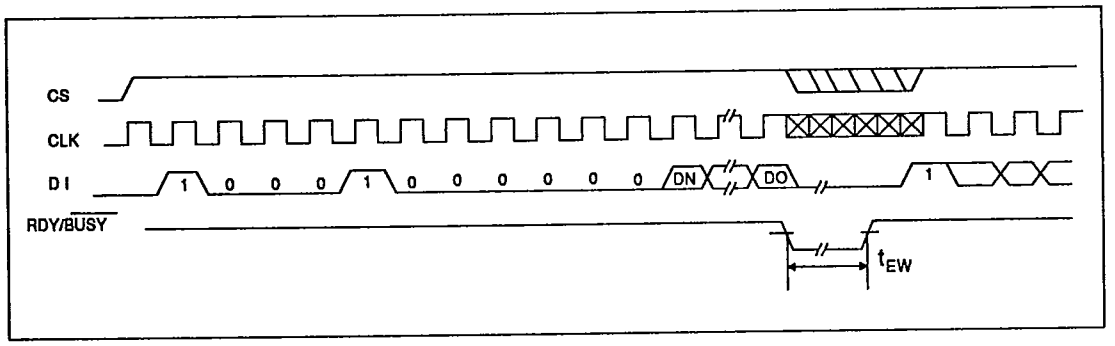
INSTRUCTION TIMING <ERAL 64 x 16 organization>



INSTRUCTION TIMING <WRAL 128 x 8 organization>



INSTRUCTION TIMING <WRAL 64 x 16 organization>



DEVICE OPERATION

The CAT59C11H is a high endurance 1024 bit non-volatile memory intended for use with all standard controllers. The CAT59C11H can be organized as either 64 registers by 16 bits, or as 128 registers by 8 bits. Six 11 bit instructions (12 bit instruction in 128 by 8 organization) control the reading, writing, and erase operations of the device. The CAT59C11H operates on a single 5 Volt supply and will generate on chip the high voltage required during any programming operations. Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (CLK). The DO pin is normal in a high impedance state except when reading data from the device. The ready/busy status can be determined after a programming operation by polling the RDY/$\overline{\text{BUSY}}$ pin.

The format for all instructions sent to the CAT59C11H is one logical "1" start bit, a 4 bit op code, a 6 bit address (7 bit address when organized as 128 X 8), and for write operations a 16 bit data field (8 bit data field when organized as 128 X 8).

READ

Upon receiving a READ command and address (clocked into the DI pin), the DO pin of the CAT59C11H will come out of the high impedance state. After sending 1 dummy zero bit the 16 bits (or 8 bits) of data located at the address location specified in the instruction will be shifted out. The data bit being shifted out will toggle on the rising edge of the CLK and is stable after the specified time delay (t_{PD1} and t_{PD0}).

ERASE/WRITE ENABLE AND DISABLE

The CAT59C11H powers up in the programming disable state. Any programming after power-up or after a PDS (programming disable) instruction must first be preceded by the PEN (programming enable) instruction. Once programming is enabled, it will remain enabled until power to the device is removed or the PDS instruction is sent. The PDS instruction can be used to disable all the CAT59C11H's program and erase functions, and will prevent any accidental programming or erasing of the device. Data can be read normally from the CAT59C11H regardless of the programming enable/disable status.

PROGRAM

After receiving a PROGRAM command, address, and the data, the RDY/BUSY pin goes low and the self clocking erase and data store cycle begins. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11H can be determined by polling the RDY/BUSY pin.

ERASE ALL

Upon receiving an ERAL command, the RDY/BUSY pin goes low and the self clocking erase sequence starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11H can be determined by polling the RDY/BUSY pin.

WRITE ALL

Upon receiving a WRAL command and data, the RDY/BUSY pin goes low and the self clocking data store cycle starts. The clocking of the CLK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT59C11H can be determined by polling the RDY/BUSY pin. It **IS** necessary for all memory locations to be erased before the WRAL command is executed.