# CAT6242

# 1.3 Amp CMOS LDO Voltage Regulator

### Description

The CAT6242 is a low dropout CMOS voltage regulator providing up to 1300 mA of output current with fast response to load current and line voltage changes. CAT6242 has a fixed output voltage that is factory programmable to a level between 1.1 V and 4.1 V with steps of 0.1 V. Other fixed values in the range are available on demand. CAT6242 is packaged in a space saving 3 mm x 3 mm WDFN−6 package with a power pad for heat sinking to the PCB.

### Features

- Guaranteed 1300 mA Continuous Output Current
- Wide Range of Output Voltages Available On Request: 1.1 V to 4.1 V in 100 mV Steps
- Low Dropout Voltage of Maximum 350 mV at 1.3 A for $V_{OUT}$ = 3.3 V
- ±1.0% Output Voltage Accuracy, ±2.0% Over Temperature
- No−load Ground Current of 70 μA Typical
- Full−load Ground Current of 160 μA Typical
- “Zero” Current Shutdown Mode
- Under Voltage Lockout
- Stable with Ceramic Output Capacitors
- Current Limit and Thermal Protection
- 3 mm x 3 mm WDFN−6 Power Package
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

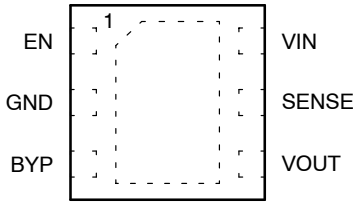
- DSP Core and I/O Voltages
- FPGAs, ASICs
- PDAs, Mobile Phones, GPS
- Camcorders and Cameras
- Hard Disk Drives

**ON Semiconductor®**

**http://onsemi.com**

**WDFN−6**
**3 x 3 mm**
**CASE 511AP**

### PIN CONNECTIONS




(Top View)

### MARKING DIAGRAM


(WDFN−6)

| | |
|---|---|
| 62XX | = Specific Device Code |
| L | = Assembly Location Code |
| AAA | = Assembly Lot Number (Last Three Digits) |
| Y | = Production Year (Last Digit) |
| WW | = Production Week (Two Digits) |
| ▪ | = Pb−Free Package |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

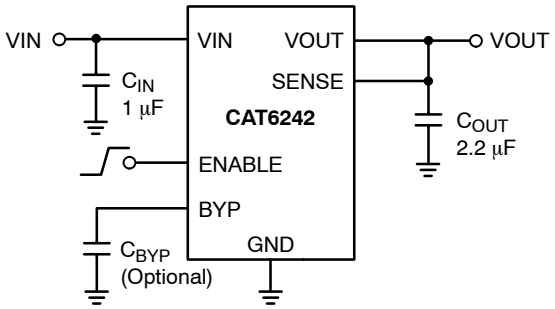



**Figure 1. Application Schematic**

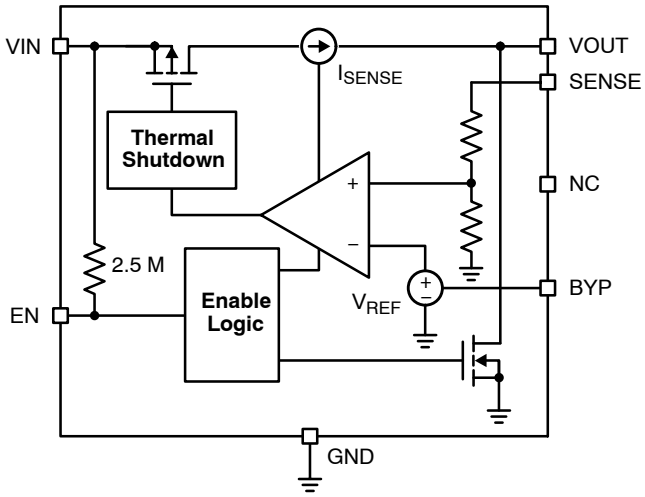



**Figure 2. Simplified Block Diagram**

**Table 1. PIN FUNCTION DESCRIPTION**

| Pin # WDFN−6 | Pin Name | Description |
|---|---|---|
| 1 | EN | The Enable Input. An active HIGH input, turning ON the LDO. A pull−up 2.5 MΩ resistor maintains the circuit in the ON state if the pin is left open. |
| 2, Pad | GND | Power Supply Ground; Device Substrate. The center pad is internally connected to Ground and as such can cause short circuits to signal traces running beneath the IC. This pad is intended for heat sinking the IC to the PCB and is typically connected to the PCB ground plane. |
| 3 | BYP | Bypass input. Placing a capacitor of 100 pF to 470 pF between BYP and ground reduces noise on $V_{OUT}$. This capacitor is optional and it increases the turn−on time. |
| 4 | $V_{OUT}$ | Regulated Output Voltage. A protection block eliminates any current flow from output to input if $V_{OUT} > V_{IN}$. |
| 5 | SENSE | SENSE is the sense input of the circuit and is connected externally to the VOUT line. |
| 6 | $V_{IN}$ | Positive Power Supply Input. Supplies power for $V_{OUT}$ as well as the regulator's internal circuitry. |

**Table 2. ABSOLUTE MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Input Voltage Range (Note 1) | $V_{IN}$ | −0.3 to 7.0 | V |
| Output Voltage Range | $V_{OUT}$ | −0.3 to 7.0 | V |
| Enable Input Range | EN | −0.3 to 7.0 V or ($V_{IN}$ + 0.3), whichever is lower | V |
| Bypass Input Range | BYP | −0.3 to 5.5 V or ($V_{IN}$ + 0.3), whichever is lower | V |
| Power Dissipation | PD | Internally Limited | mW |
| Maximum Junction Temperature | $T_{J(max)}$ | 150 | °C |
| Storage Temperature Range | $T_{STG}$ | −65 to 150 | °C |
| ESD Capability, Human Body Model (Note 2) | $ESD_{HBM}$ | 2 | kV |
| ESD Capability, Machine Model (Note 2) | $ESD_{MM}$ | 200 | V |
| Lead Temperature Soldering<br>Reflow (SMD Styles Only), Pb−Free Versions (Note 3) | $T_{SLD}$ | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating range.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D

**Table 3. THERMAL CHARACTERISTICS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Characteristics, WDFN−6, 3 x 3 mm | | | °C/W |
| Thermal Resistance, Junction−to−Air: 1 $in^2$/1 oz. copper (Note 4) | $R_{\theta JA}$ | 55 | |
| Thermal Reference, Junction−to−Case (Note 4) | $R_{\psi JL}$ | 10 | |

4. Values based on copper area of 645 $mm^2$ (or 1 $in^2$) of 1 oz copper thickness and FR4 PCB substrate.

**Table 4. OPERATING RANGES** (Note 5)

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Voltage CAT6242 (Note 6) | $V_{IN}$ | 1.8 | 5.5 | V |
| Output Current | $I_{OUT}$ | 1 | 1300 | mA |
| Output Voltage | $V_{OUT}$ | 1.1 | 4.1 | V |
| Ambient Temperature | $T_A$ | −40 | 85 | °C |

5. Refer to ELECTRICAL CHARACTERISTIS and APPLICATION INFORMATION for Safe Operating range.
6. Minimum $V_{IN\_MIN}$ = 1.8 V or ($V_{OUT}$ + $V_{DO}$), whichever is higher.

**Table 5. ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = ($V_{OUT}$ + 1 V) or $V_{IN\_MIN}$, whichever is higher, $C_{IN}$ = 1 μF, $C_{OUT}$ = 2.2 μF, for typical values $T_A$ = 25°C, for **Bold** values $T_A$ = −40°C to 85°C; unless otherwise noted.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUT / OUTPUT** | | | | | | |
| $V_{IN}$ | Input Voltage | | **1.8** | | **5.5** | V |
| $V_{OUT}$ | Output Voltage Range | Any level in range with increments of 0.1 V | **1.1** | | **4.1** | V |
| $V_{OUT-ACC}$ | Output Voltage Accuracy | Initial accuracy, $I_{OUT}$ = 1 mA | −1 | | 1 | % |
| | | Initial accuracy, $I_{OUT}$ = 1 mA | **−2** | | **2** | |
| $TC_{OUT}$ | Output Voltage Temp. Coefficient | | | **25** | | ppm/°C |
| $I_{OUT}$ | Output Current | | 0.001 | 1 | 1.3 | A |

**Table 5. ELECTRICAL CHARACTERISTICS** ($V_{IN}$ = ($V_{OUT}$ + 1 V) or $V_{IN\_MIN}$, whichever is higher, $C_{IN}$ = 1 μF, $C_{OUT}$ = 2.2 μF, for typical values $T_A$ = 25°C, for **Bold** values $T_A$ = −40°C to 85°C; unless otherwise noted.)

| Symbol | Parameter | | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **INPUT / OUTPUT** | | | | | | | |
| $V_{R-LINE}$ | Line Regulation | | $V_{IN}$ = $V_{OUT}$ + 1.0 V to 5.5 V, $I_{OUT}$ = 10 mA | −0.2 | ±0.05 | 0.2 | %/V |
| | | | $V_{IN}$ = $V_{OUT}$ + 1.0 V to 5.5 V, $I_{OUT}$ = 10 mA | **−0.35** | | **0.35** | |
| $V_{R-LOAD}$ | Load Regulation | | $I_{OUT}$ = 1 mA to 1300 mA | | 1.5 | 2 | % |
| | | | $I_{OUT}$ = 1 mA to 1300 mA | | | **3** | |
| $V_{DO}$ | Dropout Voltage | $V_{OUT}$ = 2.5 V | $I_{OUT}$ = 300 mA $T_A$ = 25°C | | | 110 | mV |
| | | $V_{OUT}$ = 3.3 V | | | | 85 | |
| | | $V_{OUT}$ = 2.5 V | $I_{OUT}$ = 1 A $T_A$ = 25°C | | | 350 | |
| | | $V_{OUT}$ = 3.3 V | | | | 275 | |
| | | $V_{OUT}$ = 2.5 V | $I_{OUT}$ = 1.3 A $T_A$ = 25°C | | | 450 | |
| | | $V_{OUT}$ = 3.3 V | | | | 350 | |
| $I_{GND}$ | Ground Current | | $I_{OUT}$ = 0 μA | | 70 | **100** | μA |
| | | | $I_{OUT}$ = 1300 mA | | 160 | **250** | |
| $I_{GND-SD}$ | Shutdown Ground Current | | $V_{EN}$ < 0.4 V | | | **2** | μA |
| ISC | Output short circuit current limit | | CAT6242, $V_{OUT}$ = 0 V | | 1000 | | mA |
| **PSRR AND NOISE** | | | | | | | |
| PSRR | Power Supply Rejection Ratio CAT6242 | | f = 1 kHz, $C_{BYP}$ = 470 pF, $I_{OUT}$ = 10 mA | | 54 | | dB |
| | | | f = 20 kHz, $C_{BYP}$ = 470 pF, $I_{OUT}$ = 10 mA | | 42 | | |
| $e_N$ | Output Noise Voltage for 1.8 V output | | BW = 10 Hz to 100 kHz $C_{BYP}$ = 470 pF, $I_{OUT}$ = 10 mA | | 45 | | μVrms |
| **UVLO, $R_{OUT}$ AND ESR** | | | | | | | |
| $R_{OUT-SH}$ | ON resistance of Discharge Transistor | | | | 150 | | Ω |
| ESR | $C_{OUT}$ equivalent series resistance | | | 5 | | 500 | mΩ |
| **ENABLE INPUT** | | | | | | | |
| $V_{HI}$ | Logic High Level | | $V_{IN}$ = 1.8 to 5.5 V | **1.6** | | | V |
| $V_{LO}$ | Logic Low Level | | $V_{IN}$ = 1.8 to 5.5 V | | | **0.4** | V |
| $I_{EN}$ | Enable Input Current | | $V_{EN}$ = 0.4 V | | 1 | **3** | μA |
| | | | $V_{EN}$ = $V_{IN}$ = 2.5 V | | 0.15 | **1** | |
| $R_{EN}$ | Enable pull−up resistor | | | | 2.5 | | MΩ |
| **TIMING** | | | | | | | |
| $T_{ON}$ | Turn−On Time | | $C_{BYP}$ = 0 pF | | 230 | | μs |
| | | | $C_{BYP}$ = 470 pF | | 1600 | | |
| **THERMAL PROTECTION** | | | | | | | |
| $T_{SD}$ | Thermal Shutdown | | | | 145 | | °C |
| $T_{HYS}$ | Thermal Hysteresis | | | | 10 | | °C |

7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

## TYPICAL CHARACTERISTICS (shown for 3.3 V Output Voltage)

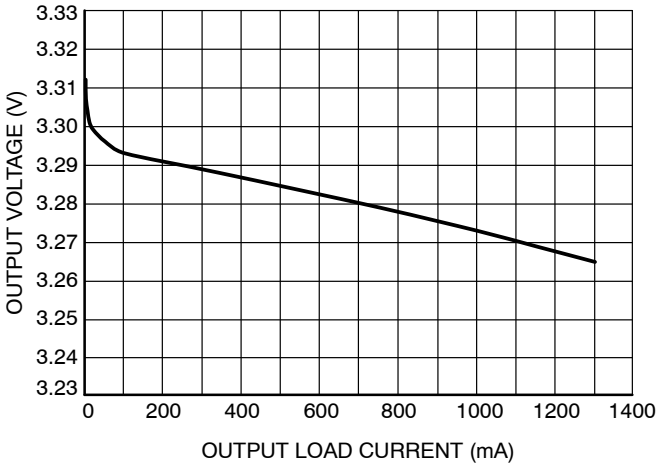



**Figure 3. Output Voltage vs. Load Current**

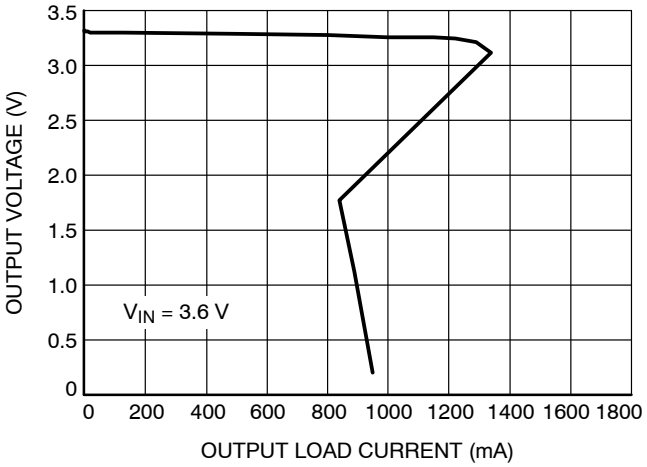



**Figure 4. Output Voltage vs. Load Current**

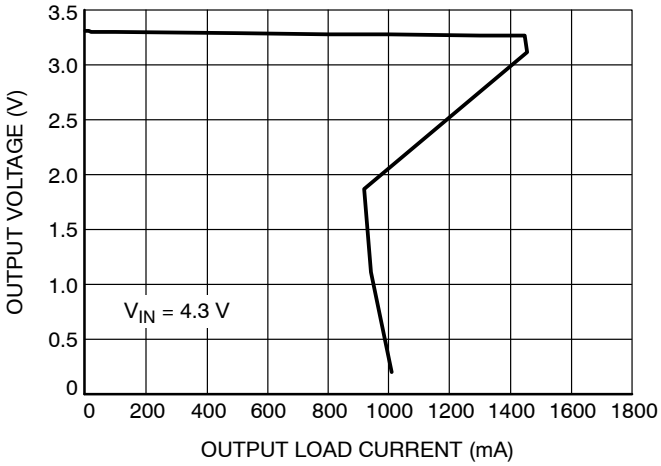



**Figure 5. Output Voltage vs. Load Current**

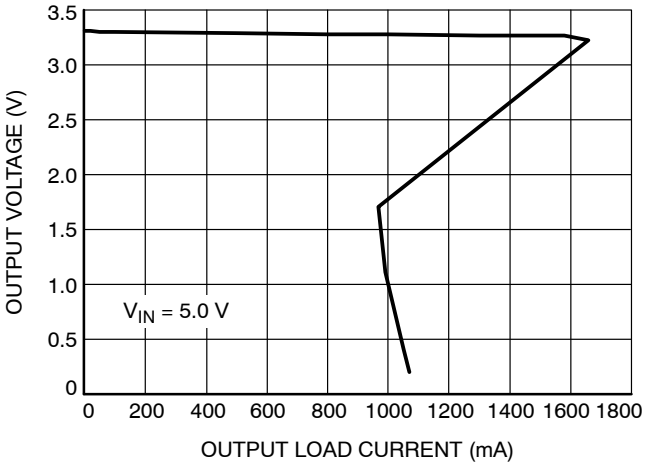



**Figure 6. Output Voltage vs. Load Current**

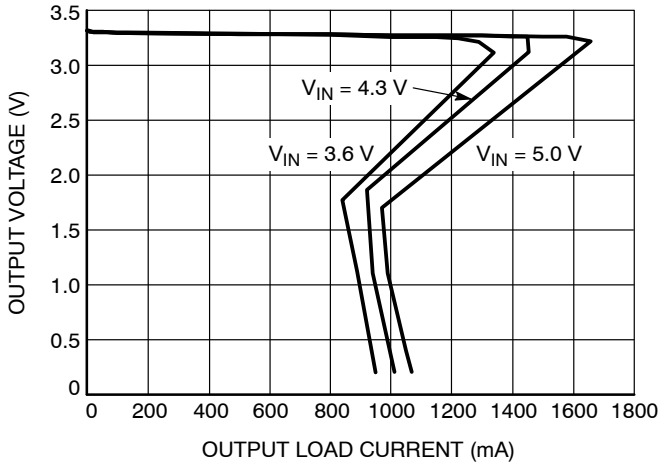



**Figure 7. Output Voltage vs. Load Current**

## TYPICAL CHARACTERISTICS (shown for 3.3 V Output Voltage)

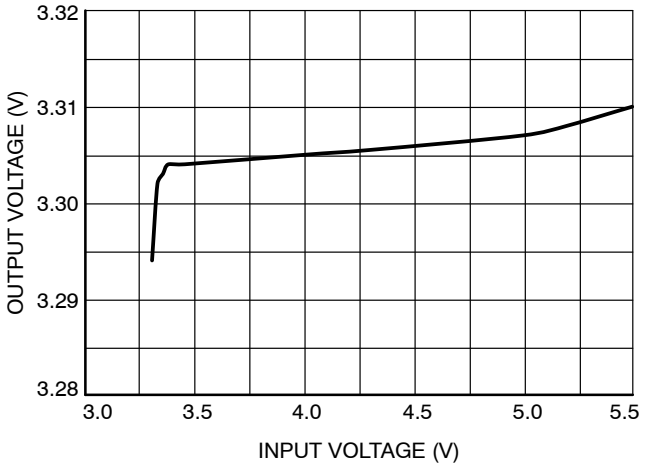



**Figure 8. Output Voltage vs. Input Voltage**

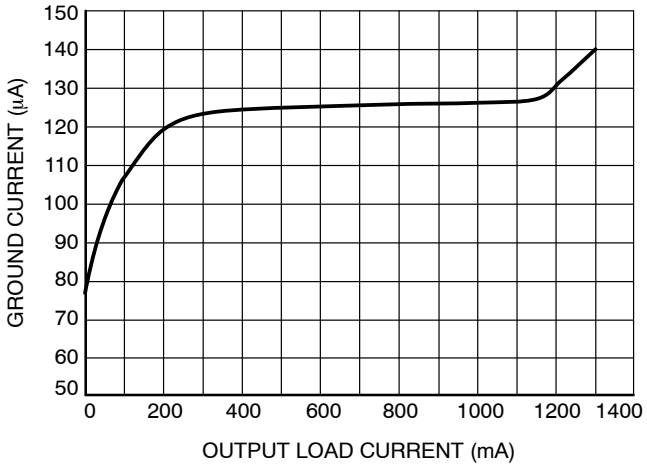



**Figure 9. Ground Current vs. Load Current**

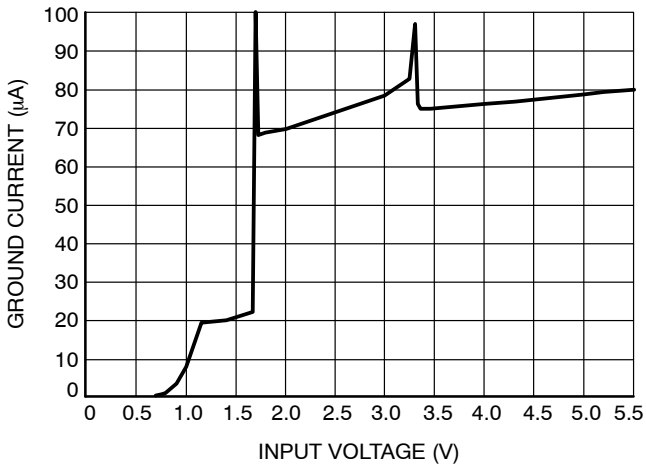



**Figure 10. Ground Current vs. Input Voltage**

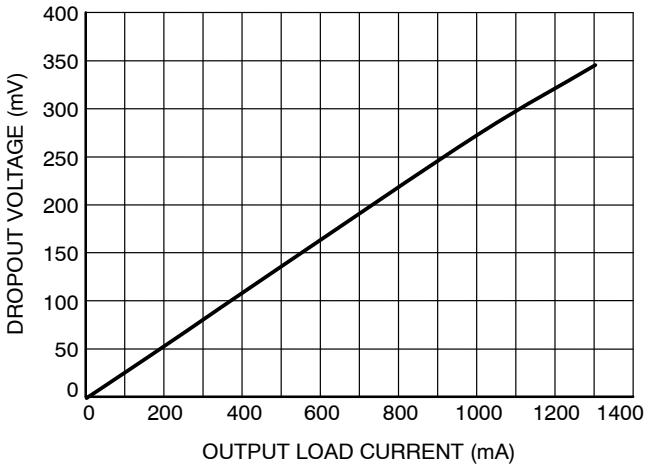



**Figure 11. Dropout Voltage vs. Load Current**

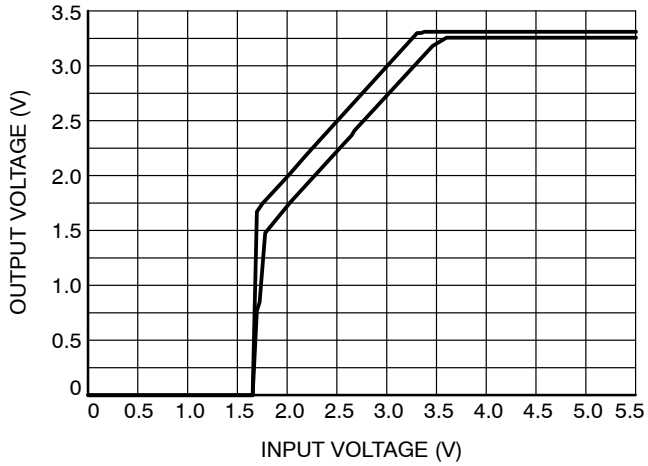



**Figure 12. Dropout Characteristics**

## TYPICAL CHARACTERISTICS (shown for 3.3 V Output Voltage)

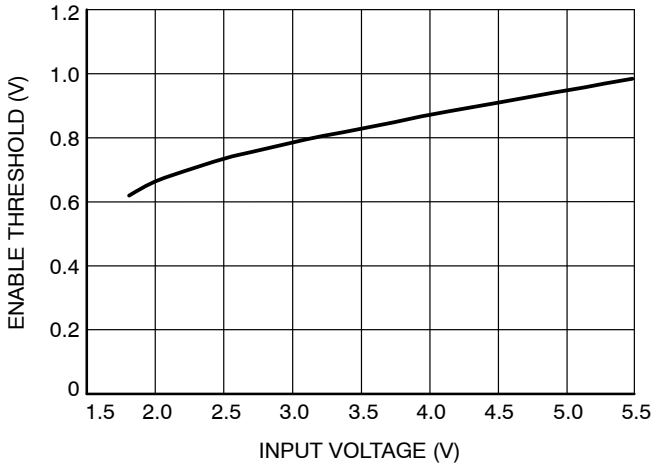



**Figure 13. Rising Enable Threshold vs. Supply Voltage**

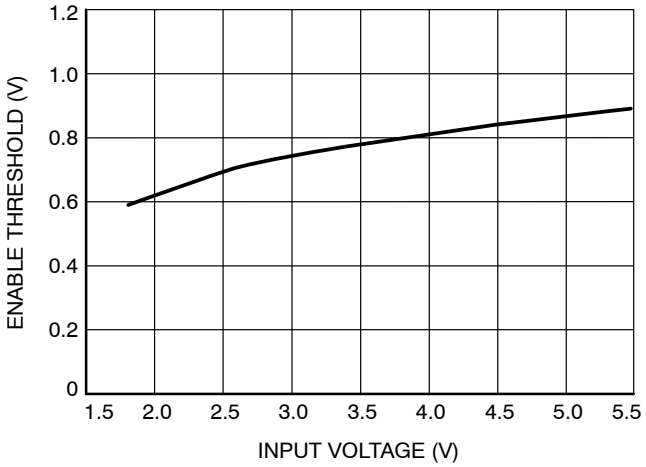



**Figure 14. Falling Enable Threshold vs. Supply Voltage**

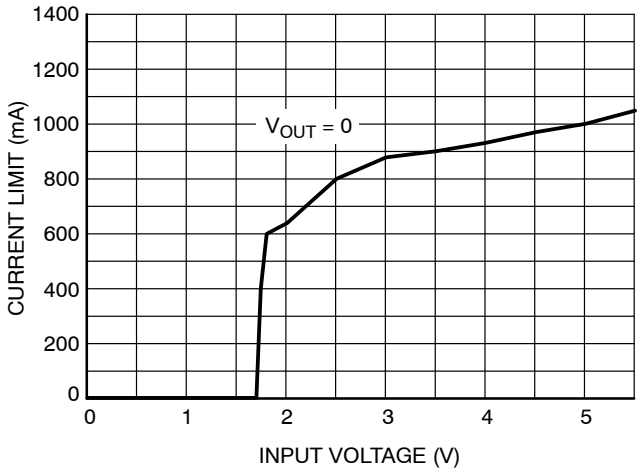



**Figure 15. Output Short Circuit Current Limit vs. Supply Voltage**

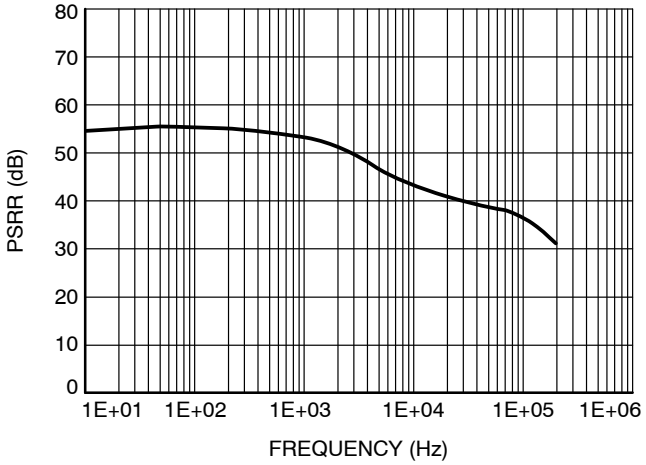



**Figure 16. PSRR @ 10 mA**

## TYPICAL CHARACTERISTICS (shown for 3.3 V Output Voltage)

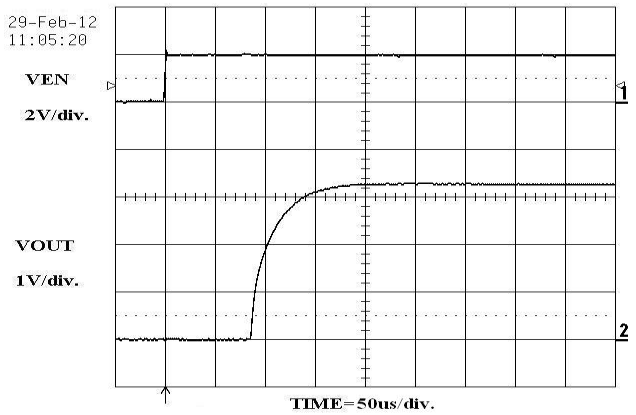



**Figure 17. Power−Up Transient**
**$V_{IN}$ = 4.4 V, $V_{OUT}$ = 3.3 V, $R_{LOAD}$ = 3300 Ω**

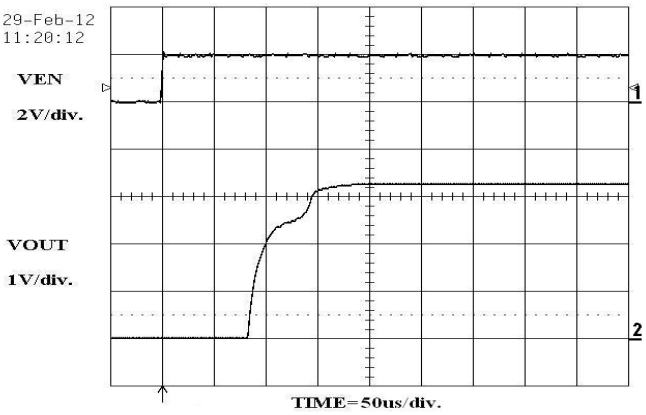



**Figure 18. Power−Up Transient**
**$V_{IN}$ = 4.3 V, $V_{OUT}$ = 3.3 V, $R_{LOAD}$ = 2.5 Ω**

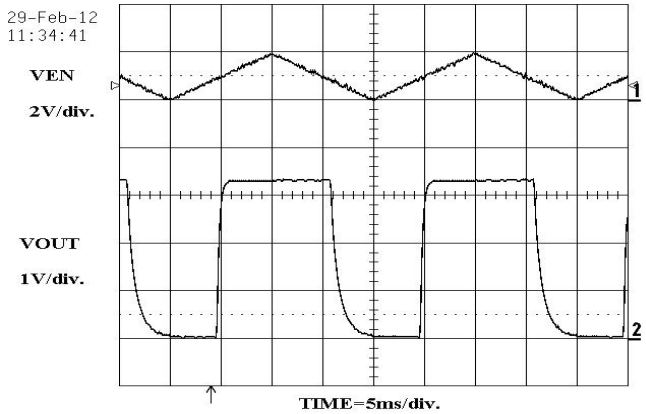



**Figure 19. Slow Enable Operation**
**$V_{IN}$ = 4.4 V, $V_{OUT}$ = 3.3 V, $R_{LOAD}$ = 3300 Ω**

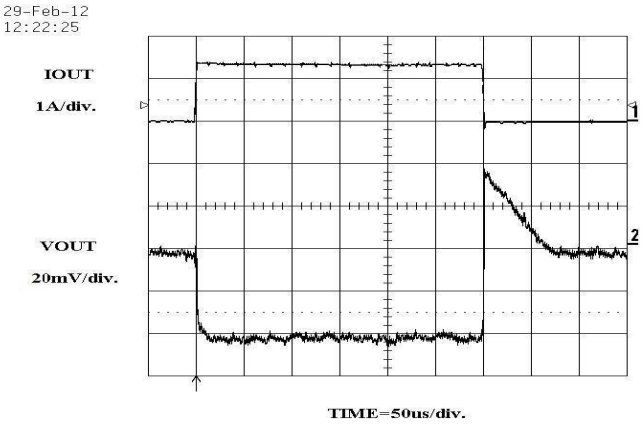



**Figure 20. Load Transient, $V_{IN}$ = 3.9 V,**
**$I_{OUT}$ = 1 mA to 1300 mA, $t_{rise}$ = $t_{fall}$ = 1 μs**

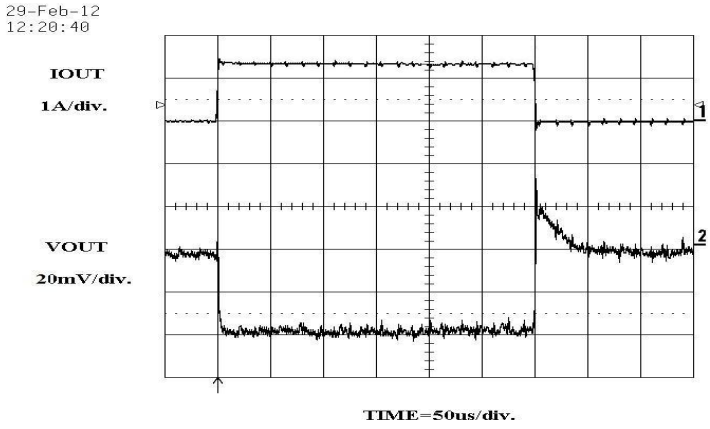



**Figure 21. Load Transient, $V_{IN}$ = 4.3 V,**
**$I_{OUT}$ = 1 mA to 1300 mA, $t_{rise}$ = $t_{fall}$ = 1 μs**

## PIN FUNCTIONS

### $V_{IN}$

Positive Power Input. Power is supplied to the device through the $V_{IN}$ pin. A bypass capacitor is required on this pin if the device is more than six inches away from the main input filter capacitor. In general it is advisable to include a small bypass capacitor adjacent to the regulator. In battery−powered circuits this is particularly important because the output impedance of a battery rises with frequency, so a bypass capacitor in the range of 1 μF to 10 μF is recommended.

### GND

Ground. The negative voltage of the input power source. The center pad on the back of the package is also electrically ground. This pad is used for cooling the device by making connection to the buried ground plane through solder filled vias or by contact with a topside copper surface exposed to free flowing air.

### ENABLE

ENABLE is an active high logic input which controls the regulator's the output state. If ENABLE < 0.4 V the regulator is shutdown and $V_{OUT}$ = 0 V. If ENABLE > 1.6 V the regulator is active and supplying power to the load.

If the regulator is intended to operate continuously and won't be shut down from time to time ENABLE should be tied to $V_{IN}$ or left floating.

### BYP

The Bypass Capacitor input is used to decrease output voltage noise by placing a capacitor between BYP and ground. The recommended range of capacitance is from 100 pF to 470 pF. Values larger than this will provide no additional improvement and will further extend CAT6242's startup time.

A bypass capacitor is not required for operation and BYP may be left open or floating if no capacitor is used but DO NOT ground BYP as this will interfere with the error amplifier's functioning.

### SENSE

SENSE is the sense input of the circuit and is connected externally to the VOUT line.

### $V_{OUT}$

$V_{OUT}$ is the regulator's output and supplies power to the load. $V_{OUT}$ can be shut off via the ENABLE input. All CAT6242 family members are designed to block reverse current, meaning anytime $V_{OUT}$ becomes greater than $V_{IN}$ the pass FET will be shut off so there is no reverse current flow from output to input. CAT6242 is also equipped with an output discharge transistor that is turned ON anytime ENABLE is at a logic Low. This transistor ensures $V_{OUT}$ discharges to 0 V when the regulator is shutdown. This is especially important when powering digital circuitry because if $V_{OUT}$ fails to reach 0 V their POR (power−ON reset) circuitry may not trigger and scrambled data or unpredictable operations may result.

A minimum output capacitor of 2.2 μF should be placed between $V_{OUT}$ and GND to insure stable operation. Increasing the size of $C_{OUT}$ will improve transient response to large changes in load current.

## APPLICATIONS INFORMATION

### Input Decoupling ($C_{IN}$)

A ceramic or tantalum 1 μF capacitor is recommended and should be connected close to the CAT6242's package. Higher capacitance and lower ESR will improve the overall line and load transient response.

### Output Decoupling ($C_{OUT}$)

The minimum output decoupling value is 2.2 μF and can be augmented to fulfill stringent load transient requirements. The regulator works with ceramic chip capacitors as well as low−ESR tantalum devices. Larger values improve noise rejection and load regulation transient response. The CAT6242 is a highly stable regulator and performs well over a wide range capacitor Equivalent Series Resistances (ESR).

### Thermal Considerations

As power in the CAT6242 increases, it may become necessary to provide thermal relief. The maximum power dissipation supported by this device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part. When the CAT6242 has good thermal conductivity through the PCB, the junction temperature will be relatively low even with high power applications. The maximum dissipation the CAT6242 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{R_{\theta JA}} \quad \text{(eq. 1)}$$

Since $T_J$ is not recommended to exceed 125°C, then with CAT6242 soldered to 645 mm$^2$ (1 sq inch), 1 oz copper area, FR4 PCB material can dissipate in excess of 1 W when the ambient temperature ($T_A$) is 25°C. Note that this assumes the pad in the center of the package is soldered to the dissipating copper foil. See Figure below for $R_{\theta JA}$ versus PCB area for heat dissipating areas smaller than 645 mm$^2$. Power dissipation can be calculated from the following equations:

$$P_D \approx V_{IN}(I_{GND} + I_{OUT}) + I_{OUT}(V_{IN} - V_{OUT}) \quad \text{(eq. 2)}$$

or

$$V_{IN(MAX)} \approx \frac{P_{D(MAX)} + (V_{OUT} \times I_{OUT})}{I_{OUT} + I_{GND}} \quad \text{(eq. 3)}$$

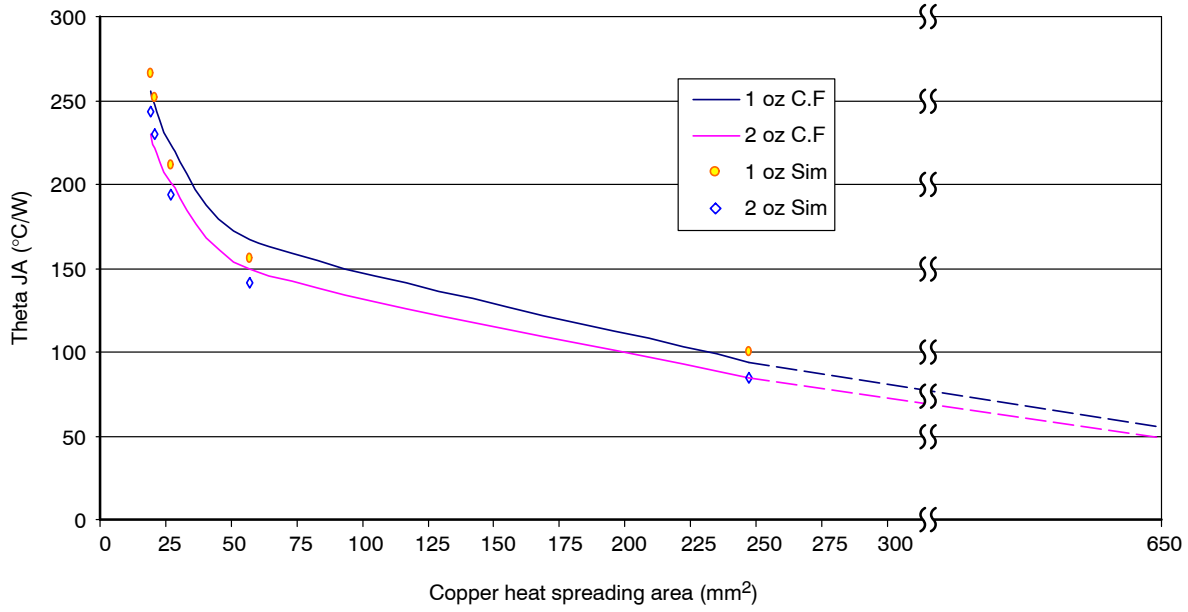



**Figure 22. Thermal Resistance vs. PCB Copper Area**

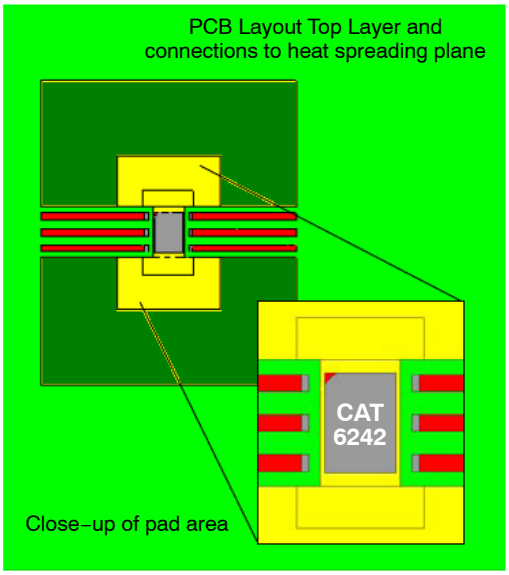


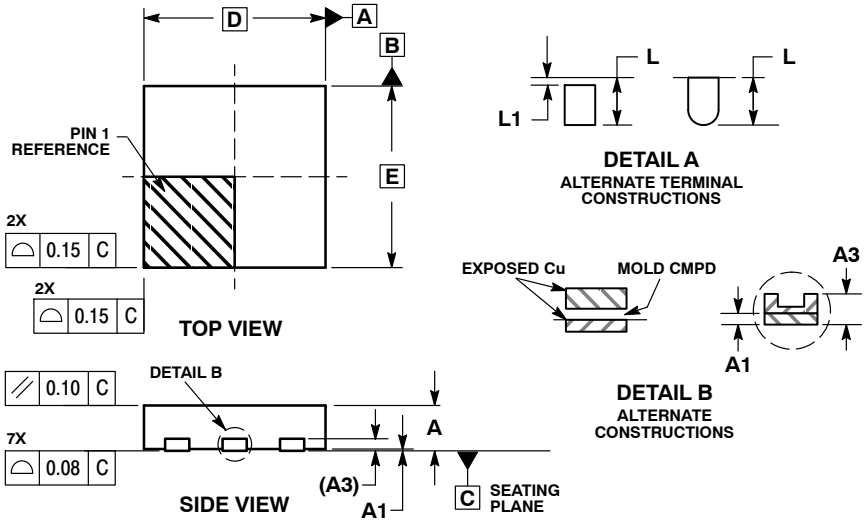

**Figure 23. Topside Copper Foil Pattern for Heat Dissipation for WDFN−6, 3 x 3 mm Package**

### Design Hints

$V_{IN}$ and GND printed circuit board traces should be as wide as possible. When the impedance of these traces is high due to narrow trace width or long length, there is a chance to pick up noise or cause the regulator to malfunction. Place external components, especially the input and output capacitors, as close as possible to the CAT6242, and keep traces between power source and load as short as possible.

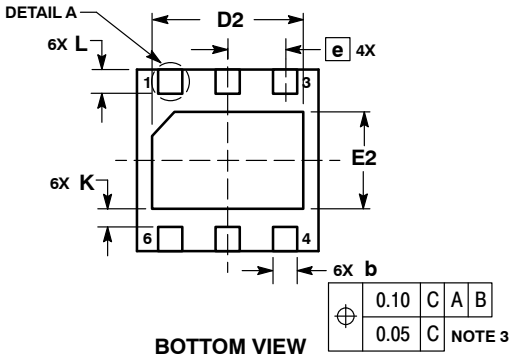
## PACKAGE DIMENSIONS

**WDFN6 3x3, 0.95P**
CASE 511AP−01
ISSUE O

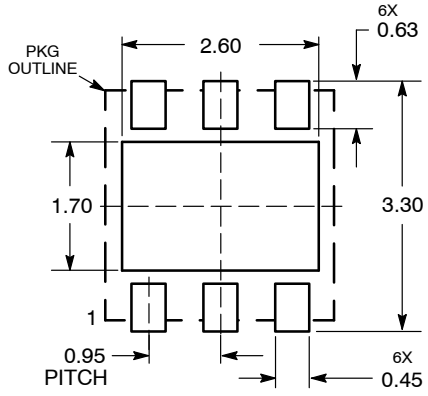



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.70 | 0.80 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.35 | 0.45 |
| D | 3.00 BSC | |
| D2 | 2.40 | 2.60 |
| E | 3.00 BSC | |
| E2 | 1.50 | 1.70 |
| e | 0.95 BSC | |
| K | 0.20 | −−− |
| L | 0.30 | 0.50 |
| L1 | −−− | 0.15 |




### SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**ORDERING INFORMATION** (Notes 8 – 13)

| Device Order Number | VOUT [V] | Specific Device Marking | Package Type | Lead Finish | **Shipping** (Note 12) |
|---|---|---|---|---|---|
| CAT6242−110MT5T3 | 1.1 | AA | WDFN−6 | Matte−Tin | Tape & Reel, 3,000 Units / Reel |
| CAT6242−120MT5T3 | 1.2 | AB | | | |
| CAT6242−130MT5T3 | 1.3 | AC | | | |
| CAT6242−140MT5T3 | 1.4 | AD | | | |
| CAT6242−150MT5T3 | 1.5 | AE | | | |
| CAT6242−160MT5T3 | 1.6 | AF | | | |
| CAT6242−170MT5T3 | 1.7 | AG | | | |
| CAT6242−180MT5T3 | 1.8 | AH | | | |
| CAT6242−190MT5T3 | 1.9 | AI | | | |
| CAT6242−200MT5T3 | 2 | B0 | | | |
| CAT6242−210MT5T3 | 2.1 | BA | | | |
| CAT6242−220MT5T3 | 2.2 | BB | | | |
| CAT6242−230MT5T3 | 2.3 | BC | | | |
| CAT6242−240MT5T3 | 2.4 | BD | | | |
| CAT6242−250MT5T3 | 2.5 | BE | | | |
| CAT6242−260MT5T3 | 2.6 | BF | | | |
| CAT6242−270MT5T3 | 2.7 | BG | | | |
| CAT6242−280MT5T3 | 2.8 | BH | | | |
| CAT6242−285MT5T3 | 2.85 | BZ | | | |
| CAT6242−290MT5T3 | 2.9 | BI | | | |
| CAT6242−300MT5T3 | 3 | C0 | | | |
| CAT6242−310MT5T3 | 3.1 | CA | | | |
| CAT6242−320MT5T3 | 3.2 | CB | | | |
| CAT6242−330MT5T3 | 3.3 | CC | | | |
| CAT6242−340MT5T3 | 3.4 | CD | | | |
| CAT6242−350MT5T3 | 3.5 | CE | | | |
| CAT6242−360MT5T3 | 3.6 | CF | | | |
| CAT6242−370MT5T3 | 3.7 | CG | | | |
| CAT6242−380MT5T3 | 3.8 | CH | | | |
| CAT6242−390MT5T3 | 3.9 | CI | | | |
| CAT6242−400MT5T3 | 4 | D0 | | | |
| CAT6242−410MT5T3 | 4.1 | DA | | | |

8. All packages are RoHS−compliant (Lead−free, Halogen−free).
9. The standard lead finish is Matte−Tin.
10. Contact factory for $V_{OUT}$ level availability.
11. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
12. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
13. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

## PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT**:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
**Phone**: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
**Fax**: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
**Email**: orderlit@onsemi.com

**N. American Technical Support**: 800−282−9855 Toll Free USA/Canada
**Europe, Middle East and Africa Technical Support:**
Phone: 421 33 790 2910
**Japan Customer Focus Center**
Phone: 81−3−5817−1050

**ON Semiconductor Website**: **www.onsemi.com**

**Order Literature**: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

**CAT6242/D**