

# CAT8836

## NanoPower Supervisory Circuit

### Description

The CAT8836 is a voltage supervisory circuit intended to provide circuit initialization and start-up timing for DSPs and other processor-based systems.

When system power comes on, CAT8836's output goes active once the supply voltage  $V_{DD}$  becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors  $V_{DD}$  and keeps the output active as long as  $V_{DD}$  remains below the threshold voltage of  $V_{TH}$ . After  $V_{DD}$  exceeds the monitoring threshold an internal timer delays the return of the output to the inactive state (high) to ensure proper system reset.

The duration of this reset delay is controlled by the CT input. When CT is connected to GND the reset delay is 10 ms, typical, in duration and when connected to  $V_{DD}$ , the delay time is typically 200 ms. Whenever the supply voltage drops below the monitoring threshold voltage  $V_{TH}$ , the output becomes active (low) again.

### Features

- Supply Current: 220 nA (typical)
- Precision Supply Voltage Supervision Range: 1.8 V, 2.5 V, 3.0 V, and 3.3 V
- Power-On Reset Generator with Selectable Delay Time: 10 ms or 200 ms
- Push/Pull  $\overline{\text{RESET}}$  (active low) Output
- Manual Reset Input
- Pin-for-Pin Replacement for TPS3836
- TSOT23-5 Package
- Temperature Range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Applications Using Low-Power DSPs, Microcontrollers, or Microprocessors
- Portable- and Battery-Powered Equipment
- Intelligent Instruments
- Wireless Communication Systems
- Automotive Systems
- Notebook Computers



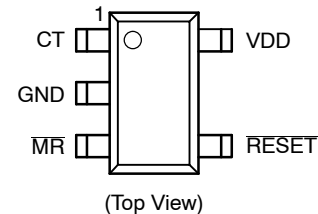
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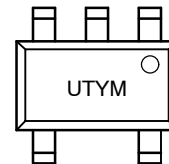


TSOT-23  
TD SUFFIX  
CASE 419AE

### PIN CONNECTIONS



### MARKING DIAGRAM



UT = Device Code  
Y = Production Year (Last Digit)  
M = Production Month: 1-9 (Jan - Sep),  
O, N, D (Oct - Dec)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

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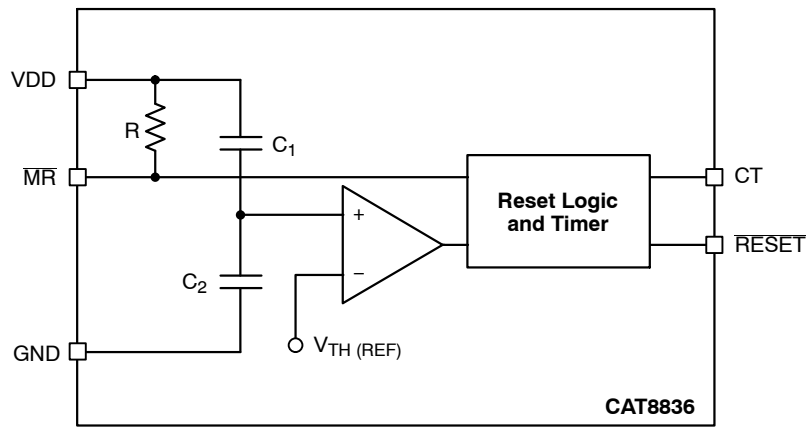


Figure 1. Functional Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Description
1	CT	Delay select pin for a fixed value of 10 ms or 200 ms.
2	GND	Ground
3	$\overline{\text{MR}}$	Manual Reset
4	$\overline{\text{RESET}}$	Active low Reset. Reset is asserted either if VDD falls below reset threshold or if MR is activated.
5	VDD	Supply Voltage which is monitored

Table 2. ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range, unless otherwise noted.)

Parameter	Symbol	Value	Unit
Supply voltage (Note 1)	$V_{DD}$	7	V
All other pins (Note 1)		-0.3 to 6	V
Maximum low output current	$I_{OL}$	5	mA
Maximum high output current	$I_{OH}$	-5	mA
Input clamp current, ( $V_I < 0$ or $V_I > V_{DD}$ )	$I_{IK}$	$\pm 10$	mA
Output clamp current, ( $V_O < 0$ or $V_O > V_{DD}$ )	$I_{OK}$	$\pm 10$	mA
Storage temperature range	$T_{STG}$	-65 to +150	$^{\circ}\text{C}$
Soldering temperature		+260	$^{\circ}\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. All voltages are with respect to GND.

Table 3. RECOMMENDED OPERATING CONDITIONS (Note 2)

Parameter	Symbol	Min	Max	Unit
Supply voltage	$V_{DD}$	1.6	5.5	V
Voltage range, CT, $\overline{\text{MR}}$ and $\overline{\text{RESET}}$ pins		0	$V_{DD} + 0.3$	V
High-level input voltage	$V_{IH}$	$0.7 \times V_{DD}$		V
Low-level input voltage	$V_{IL}$		$0.3 \times V_{DD}$	V
Input transition rise and fall rate at $\overline{\text{MR}}$	$\Delta t/\Delta V$		100	ns/V
Operating temperature range	$T_A$	-40	+85	$^{\circ}\text{C}$

2. Refer to Electrical Characteristics and Application Information for Safe Operating Area.

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**Table 4. ELECTRICAL CHARACTERISTICS** (Over recommended operating conditions, unless otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
RESET high-level output voltage		$V_{OH}$	$V_{DD} = 3.3\text{ V}$ , $I_{OH} = -2\text{ mA}$	$0.8 \times V_{DD}$			V
RESET Low-level output voltage		$V_{OL}$	$V_{DD} = 1.8\text{ V}$ , $I_{OL} = 1\text{ mA}$			0.4	V
			$V_{DD} = 3.3\text{ V}$ , $I_{OL} = 2\text{ mA}$				
RESET power-up voltage (Note 3)			$V_{DD} \geq 1.1\text{ V}$ , $I_{OL} = 50\text{ }\mu\text{A}$			0.2	V
Negative-going input threshold voltage (Note 4)	CAT8836E18	$V_{TH}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	1.66	1.71	1.74	V
	CAT8836J25			2.18	2.25	2.29	V
	CAT8836H30			2.70	2.79	2.85	V
	CAT8836L30			2.56	2.64	2.69	V
	CAT8836K33			2.84	2.93	2.99	V
Hysteresis at $V_{DD}$ input		$V_{HYS}$	$1.7\text{ V} < V_{IT} < 2.5\text{ V}$		30		mV
			$2.5\text{ V} < V_{IT} < 3.5\text{ V}$		40		
Input high-level current	MR (Note 5)	$I_{IH}$	MR = $0.7 \times V_{DD}$ , $V_{DD} = 5.5\text{ V}$	-40	-60	-100	$\mu\text{A}$
	CT		CT = $V_{DD} = 5.5\text{ V}$	-25		+25	nA
Input low-level current	MR (Note 5)	$I_{IL}$	MR = $0\text{ V}$ , $V_{DD} = 5.5\text{ V}$	-130	-200	-340	$\mu\text{A}$
	CT		CT = $0\text{ V}$ , $V_{DD} = 5.5\text{ V}$	-25		+25	nA
Supply current		$I_{DD}$	$V_{DD} > V_{TH}$ , $V_{DD} < 3\text{ V}$		220	400	nA
			$V_{DD} > V_{TH}$ , $V_{DD} > 3\text{ V}$		250	450	
			$V_{DD} < V_{TH}$		10	15	$\mu\text{A}$
Internal pull-up resistor at MR		$R_{IN}$			30		k $\Omega$
Input capacitance at MR and CT		$C_I$	$V_I = 0\text{ V to } V_{DD}$		5		pF

3. The lowest voltage at which the RESET output becomes active.  $t_R$ ,  $V_{DD} \geq 15\text{ }\mu\text{s/V}$ .

4. To ensure best stability of the threshold voltage, a bypass capacitor (ceramic,  $0.1\text{ }\mu\text{F}$ ) should be placed near the supply terminal.

5. If manual reset is unused, MR should be connected to  $V_{DD}$  to minimize current consumption.

**Table 5. SWITCHING CHARACTERISTICS** (At  $T_A = +25^\circ\text{C}$ ,  $R_L = 1\text{ M}\Omega$ , and  $C_L = 50\text{ pF}$ , unless otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Delay time		$t_{PD}$	$V_{DD} \geq V_{TH} + 0.2\text{ V}$ , MR = $0.7 \times V_{DD}$ , CT = GND	5	10	15	ms
			$V_{DD} \geq V_{TH} + 0.2\text{ V}$ , MR = $0.7 \times V_{DD}$ , CT = $V_{DD}$	100	200	300	
Propagation (delay) time, high-to-low-level output	$V_{DD}$ to RESET delay	$t_{PHL}$	$V_{IL} = V_{TH} - 0.2\text{ V}$ , $V_{IH} = V_{TH} + 0.2\text{ V}$			10	$\mu\text{s}$
			$V_{IL} = 1.6\text{ V}$			50	
Propagation (delay) time, high-to-low-level output	MR to RESET delay	$t_{MHL}$	$V_{DD} \geq V_{TH} + 0.2\text{ V}$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$			100	ns

**Table 6. TIMING REQUIREMENTS** (At  $T_A = +25^\circ\text{C}$ ,  $R_L = 1\text{ M}\Omega$ , and  $C_L = 50\text{ pF}$ , unless otherwise noted.)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Pulse width	at $V_{DD}$	$t_W$	$V_{IH} = V_{TH} + 0.2\text{ V}$ , $V_{IL} = V_{TH} - 0.2\text{ V}$	6			$\mu\text{s}$
	at MR	$t_{WR}$	$V_{DD} \geq V_{TH} + 0.2\text{ V}$ , $V_{IL} = 0.3 \times V_{DD}$ , $V_{IH} = 0.7 \times V_{DD}$	1			

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Table 7. FUNCTION TABLE

MR	$V_{DD} > V_{TH}$	RESET
L	0	L
L	1	L
H	0	L
H	1	H

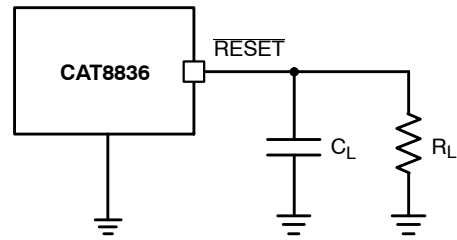


Figure 2. Test Circuit

## TIMING DIAGRAM

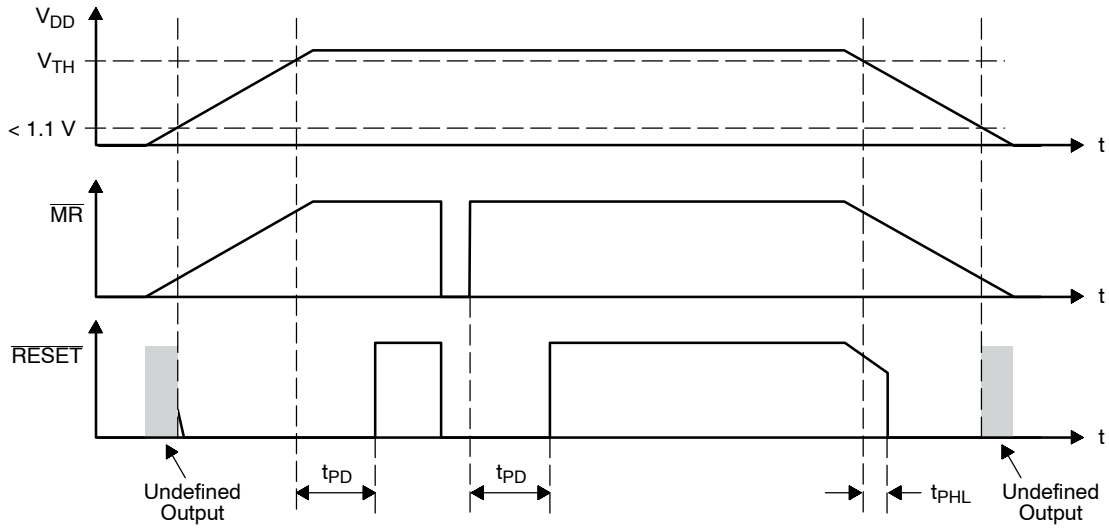


Figure 3. Timing Diagram

TYPICAL CHARACTERISTICS

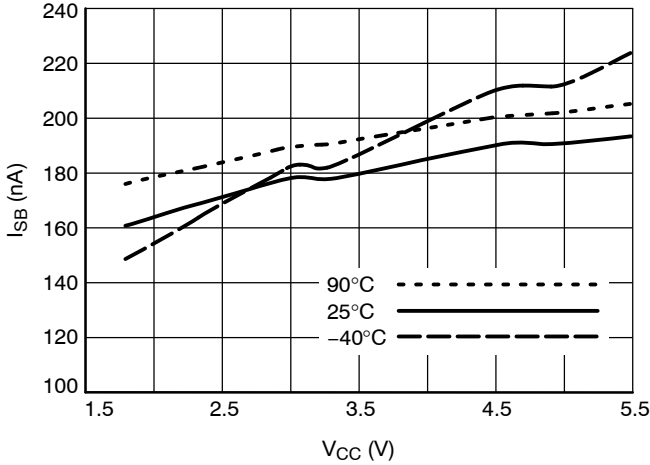


Figure 4. Supply Current vs. Supply Voltage

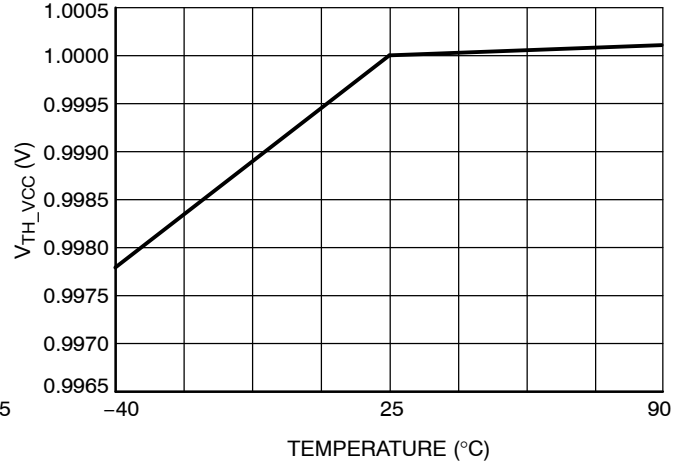


Figure 5. Normalized Reset Threshold Voltage vs. Temperature

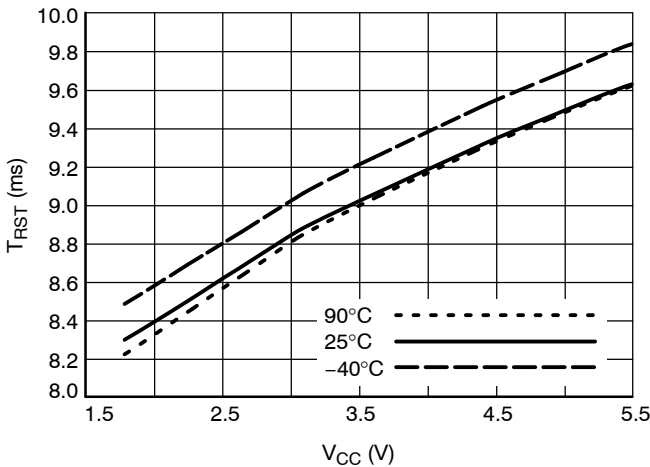


Figure 6. Reset Time Out vs.  $V_{CC}$  (CT = 0 V)

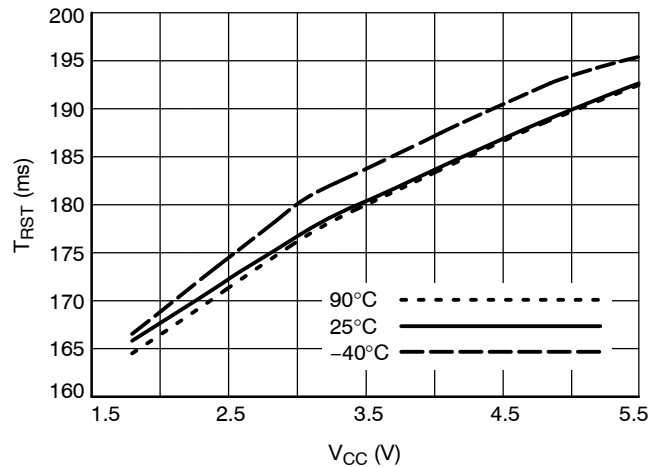


Figure 7. Reset Time Out vs.  $V_{CC}$  (CT = 5 V)

Detailed Description

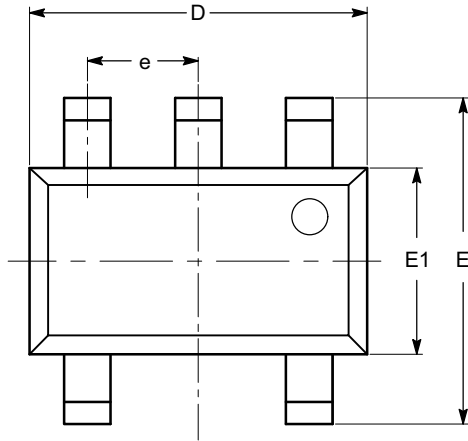
The supervisory circuit monitors  $V_{DD}$  and keeps the  $\overline{\text{RESET}}$  output active as long as  $V_{DD}$  remains below the threshold voltage of  $V_{TH}$ . An internal timer delays the return

of the output to the inactive state (high) to ensure proper system reset. The delay time starts after  $V_{DD}$  has risen above the threshold.

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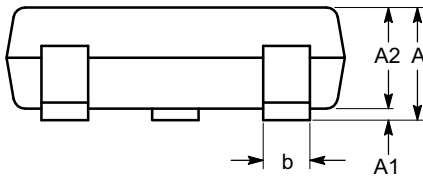
## PACKAGE DIMENSIONS

TSOT-23, 5 LEAD  
CASE 419AE-01  
ISSUE O

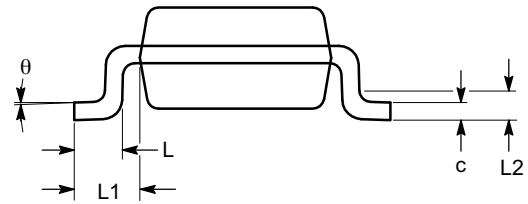


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.00
A1	0.01	0.05	0.10
A2	0.80	0.87	0.90
b	0.30		0.45
c	0.12	0.15	0.20
D	2.90 BSC		
E	2.80 BSC		
E1	1.60 BSC		
e	0.95 TYP		
L	0.30	0.40	0.50
L1	0.60 REF		
L2	0.25 BSC		
$\theta$	0°		8°



SIDE VIEW



END VIEW

### Notes:

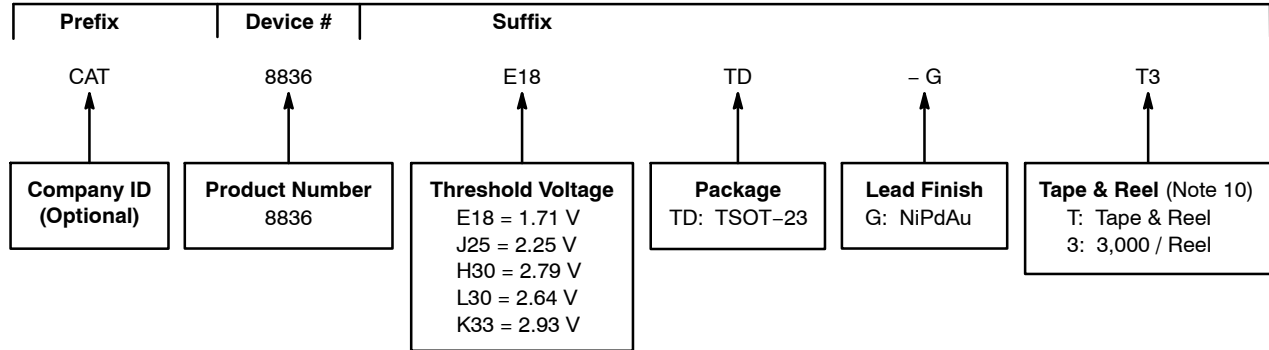
- (1) All dimensions are in millimeters. Angles in degrees.
- (2) Complies with JEDEC MO-193.

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**Table 8. ORDERING INFORMATION**

Device	Nominal Supply Voltage	Threshold Level	Marking	Package	Shipping
CAT8836E18TD-GT3	1.8 V	1.71	UTYM	TSOT-23 (Pb-Free)	3000 / Tape & Reel
CAT8836J25TD-GT3	2.5 V	2.25			
CAT8836H30TD-GT3	3.0 V	2.79			
CAT8836L30TD-GT3	3.0 V	2.64			
CAT8836K33TD-GT3	3.3 V	2.93			

**Example of Ordering Information** (Notes 6 – 9)



6. All packages are RoHS-compliant (Lead-free, Halogen-free).
7. The standard finish is NiPdAu.
8. The device used in the above example is a CAT8836E18TD-GT3 (CAT8836, 1.71 threshold voltage, TSOT-23, NiPdAu, Tape & Reel, 3,000/Reel).
9. For additional detection voltage, package and temperature options, please contact your nearest ON Semiconductor Sales office.
10. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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