CATALYST

CAT93HC46

1-kb High Speed Microwire Serial EEPROM

HALOGEN FREE LEAD FREE™

FEATURES

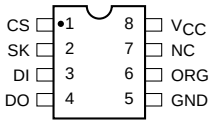
- **High speed operation: 4 MHz @ 5.0 V**
- **1.8 to 5.5 volt operation**
- **Selectable x8 or x16 word organization**
- **Sequential Read**
- **Software write protection**
- **Power-up inadvertent write protection**
- **Low power CMOS technology**
- **1,000,000 program/erase cycles**
- **100 year data retention**
- **Industrial and extended temperature ranges**
- **8-Lead PDIP, SOIC, MSOP and TSSOP packages**

DESCRIPTION

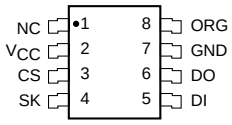
The CAT93HC46 is a 1-kb Serial EEPROM memory device which is configured as registers of either 16 bits (ORG pin at V_{CC}) or 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93HC46 is manufactured using Catalyst's advanced CMOS EEPROM floating gate technology. The device is designed to endure 1,000,000 program/erase cycles and has a data retention of 100 years. The CAT93HC46 is available in 8-pin DIP, SOIC, MSOP or TSSOP packages.

PIN CONFIGURATION

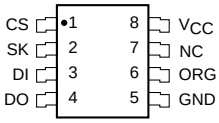
DIP Package (P, L)



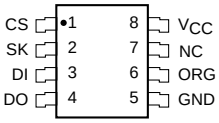
SOIC Package (J, W)



SOIC Package (S, V)



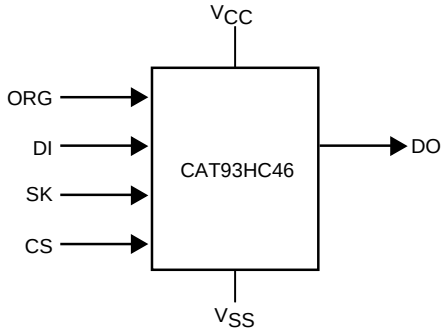
MSOP Package (R, Z)



TSSOP Package (U, Y)

Note: When the ORG pin is connected to VCC, the X16 organization is selected. When it is connected to ground, the X8 pin is selected. If the ORG pin is left unconnected, then an internal pullup device will select the X16 organization.

FUNCTIONAL SYMBOL



PIN FUNCTIONS

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	1.8 to 5.5 V Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Pin with Respect to Ground(1) .... -2.0 V to V_{CC} + 2.0 V
V_{CC} with Respect to Ground ..... -2.0 V to 7.0 V
Lead Soldering Temperature (10 secs) ..... 300°C
Output Short Circuit Current(2) ..... 100 mA

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Typ	Max	Units
N_{END}(3)	Endurance	MIL-STD-883, Test Method 1033	1,000,000			Cycles/Byte
T_{DR}(3)	Data Retention	MIL-STD-883, Test Method 1008	100			Years
V_{ZAP}(3)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000			Volts
I_{LTH}(3)(4)	Latch-Up	JEDEC Standard 17	100			mA

D.C. OPERATING CHARACTERISTICS

Industrial Temperature Range (-40°C to 85°C)

Symbol	Parameter	Limits			Units	Test Conditions
		Min	Typ	Max		
I_{CC1}	Power Supply Current (Write)			2	mA	f_{SK} = 4 MHz, V_{CC} = 5.0 V
I_{CC2}	Power Supply Current (Read)			200	µA	f_{SK} = 4 MHz, V_{CC} = 5.0 V
I_{SB1}	Standby Supply Current (x8)			10	µA	CS = GND, ORG=GND
I_{SB2}(5)	Standby Supply Current (x16)		0	10	µA	CS = GND, ORG = Float or V_{CC}
I_{LI}	Input Leakage Current			1	µA	V_{IN} = 0 V to V_{CC}, CS = GND
I_{LO}	Output Leakage Current			1	µA	V_{OUT} = 0 V to V_{CC}, CS = GND
V_{IL1}	Input Low Voltage	-0.1		0.8		4.5 V ≤ V_{CC} < 5.5 V
V_{IH1}	Input High Voltage	2		V_{CC} + 1		4.5 V ≤ V_{CC} < 5.5 V
V_{IL2}	Input Low Voltage	0		V_{CC} x 0.2		1.8 V ≤ V_{CC} < 4.5 V
V_{IH2}	Input High Voltage	V_{CC} x 0.7		V_{CC} + 1		1.8V ≤ V_{CC} < 4.5 V
V_{OL1}	Output Low Voltage			0.4		4.5 V ≤ V_{CC} < 5.5 V, I_{OL} = 2.1 mA
V_{OH1}	Output High Voltage	2.4			V	4.5 V ≤ V_{CC} < 5.5 V, I_{OH} = -400 µA
V_{OL2}	Output Low Voltage			0.2		1.8 V ≤ V_{CC} < 4.5 V, I_{OL} = 1 mA
V_{OH2}	Output High Voltage	V_{CC} - 0.2				1.8 V ≤ V_{CC} < 4.5 V, I_{OH} = -100 µA

Note:
(1) The minimum DC input voltage is -0.5 V. During transitions, inputs may undershoot to -2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods of less than 20 ns.
(2) Output shorted for no more than one second.
(3) This parameter is tested initially and after a design or process change that affects the parameter.
(4) Latch-up protection is provided for stresses up to 100 mA on I/O pins from -1 V to V_{CC} + 1 V.
(5) Standby Current (ISB_2) = 0 µA (<900 nA).

POWER-UP TIMING (1)(2)

Symbol	Parameter	Min	Typ	Max	Units
t_{PUR}	Power-up to Read Operation			1	ms
t_{PUW}	Power-up to Write Operation			1	ms

A.C. CHARACTERISTICS

Industrial Temperature Range (-40°C to 85°C)

Symbol	Parameter	1.8 V - 5.5 V		2.5 V - 5.5 V		4.5 V - 5.5 V		Units	Test Conditions
		Min	Max	Min	Max	Min	Max		
SK_{MAX}	Maximum Clock Frequency	DC	1	DC	2	DC	4	MHz	CL = 100 pF (3)
t_{CSS}	CS Setup Time	240		120		60		ns	
t_{CSH}	CS Hold Time	0		0		0		ns	
t_{DIS}	DI Setup Time	240		120		60		ns	
t_{DIH}	DI Hold Time	240		120		60		ns	
t_{PD1}	Output Delay to 1		480		240		120	ns	
t_{PD0}	Output Delay to 0		480		240		120	ns	
t_{HZ}(1)	Output Delay to High-Z		240		120		60	ns	
t_{CSMIN}	Minimum CS Low Time	240		120		60		ns	
t_{SKHI}	Minimum SK High Time	480		240		120		ns	
t_{SKLOW}	Minimum SK Low Time	240		120		60		ns	
t_{SV}	Output Delay to Status Valid		480		240		120	ns	
t_{EW}	Program/Erase Pulse Width		5		5		5	ms	

NOTE:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.
(3) The input levels and timing reference points are shown in the “AC Test Conditions” table.

A.C. TEST CONDITIONS

Input Rise and Fall Times	≤ 10 ns	
Input Pulse Voltages	0.4 V to 2.4 V	4.5 V ≤ V_{CC} ≤ 5.5 V
Timing Reference Voltages	0.8 V, 2.0 V	4.5 V ≤ V_{CC} ≤ 5.5 V
Input Pulse Voltages	V_{CC} x 0.2 to V_{CC} x 0.8	1.8 V ≤ V_{CC} ≤ 4.5 V
Timing Reference Voltages	V_{CC} x 0.5	1.8 V ≤ V_{CC} ≤ 4.5 V

DEVICE OPERATION

The CAT93HC46 is a 1024-bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93HC46 can be organized as registers of either 16 bits or 8 bits. When organized as X16, seven 9-bit instructions control the reading, writing and erase operations of the device. When organized as X8, seven 10-bit instructions control the operation of the device. The CAT93HC46 operates on a single power supply and will generate on chip the high voltage required during write operation.

Instructions, addresses, and data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state, except when reading data from the device, or when checking the ready/busy status after a write operation.

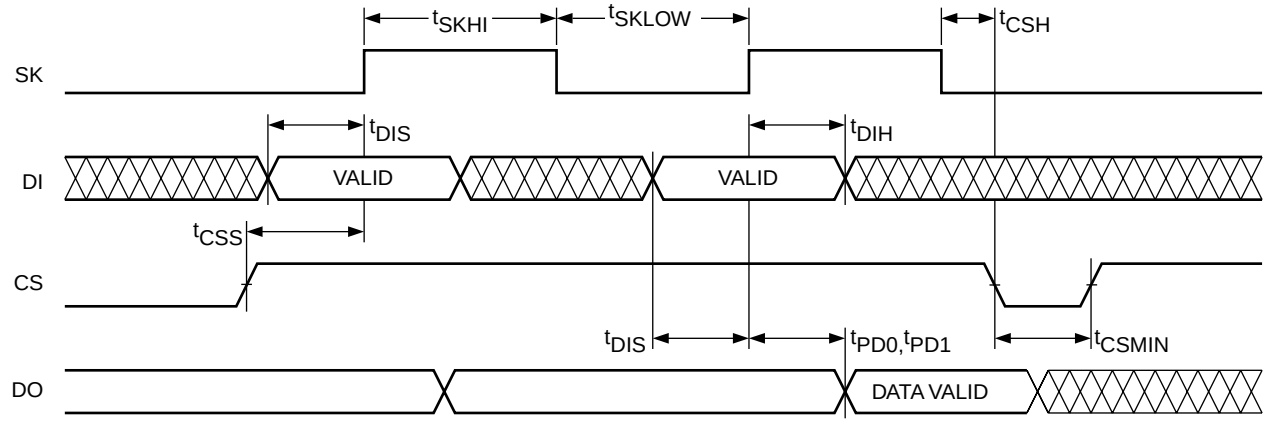
The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the falling edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical "1" start bit, a 2-bit (or 4-bit) opcode, 6-bit byte/word address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organization).

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A6-A0	A5-A0			Read Address AN–A0
ERASE	1	11	A6-A0	A5-A0			Clear Address AN–A0
WRITE	1	01	A6-A0	A5-A0	D7-D0	D15-D0	Write Address AN–A0
EWEN	1	00	11XXXXX	11XXXX			Write Enable
EWDS	1	00	00XXXXX	00XXXX			Write Disable
ERAL	1	00	10XXXXX	10XXXX			Clear All Addresses
WRAL	1	00	01XXXXX	01XXXX	D7-D0	D15-D0	Write All Addresses

Figure 1. Sychronous Data Timing



Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93HC46 will come out of the high impedance state; after an initial dummy zero bit, data will be shifted out, MSB first. The output will toggle on the rising edge of the SK clock and will be stable after the specified time delay (t_{PD0} or t_{PD1})

After the 1st data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the CAT93HC46 will automatically increment to the next address and shift out the next data word. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceeded by a dummy zero bit; all subsequent data words will follow without a dummy zero bit.

Write

After receiving a WRITE command, address and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self-timed clear and data store cycle into the specified memory location. The clocking of the SK pin is not necessary after the device has entered the self-timed mode. (Note 1.) The ready/busy status of the CAT93HC46 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of t_{CSMIN}. The falling edge of CS will start the self-timed clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self-timed mode. (Note 1.) The ready/busy status of the CAT93HC46 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical "1" state.

Figure 2a. Read Instruction Timing

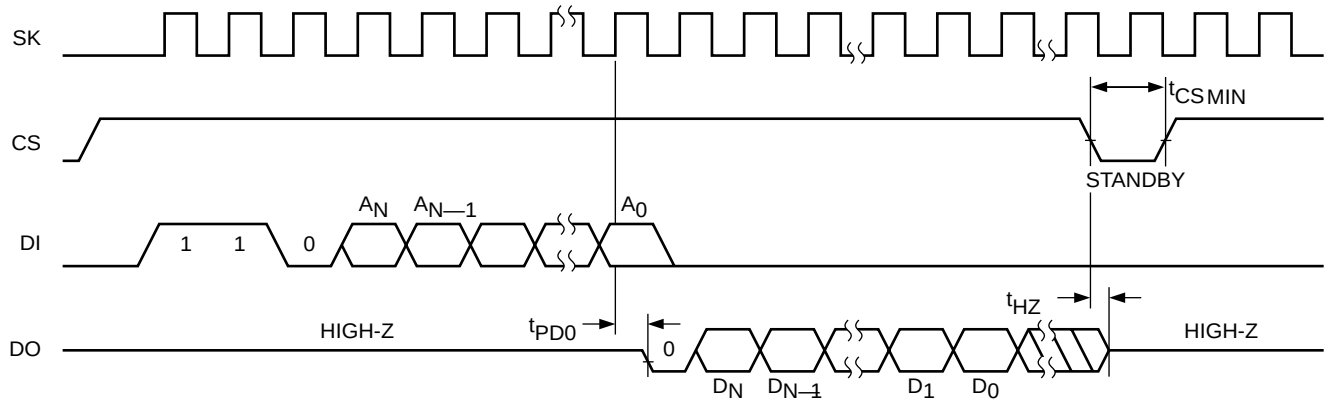
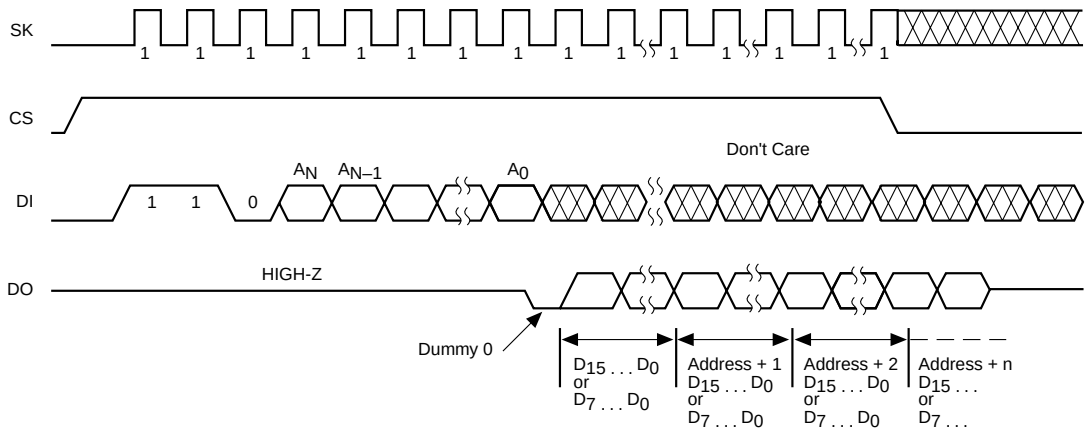


Figure 2b. Sequential Read Instruction Timing



Erase/Write Enable and Disable

The CAT93HC46 powers up in the write disable state. Any writing after power-up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once write is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93HC46 write and clear instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self-timed clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self-timed mode. (Note 1.) The ready/busy status of the CAT93HC46 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory locations will return to a logical “1” state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self-timed data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self-timed mode. The ready/busy status of the CAT93HC46 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed. Once written, the contents of all memory locations will return to a logical “0” state.

Note 1: After the last data bit has been sampled, Chip Select (CS) must be brought Low before the next rising edge of the clock (SK) in order to start the self-timed high voltage cycle. This is important because if the CS is brought low before or after this specific frame window, the addressed location will not be programmed or erased.

Figure 3. Write Instruction Timing

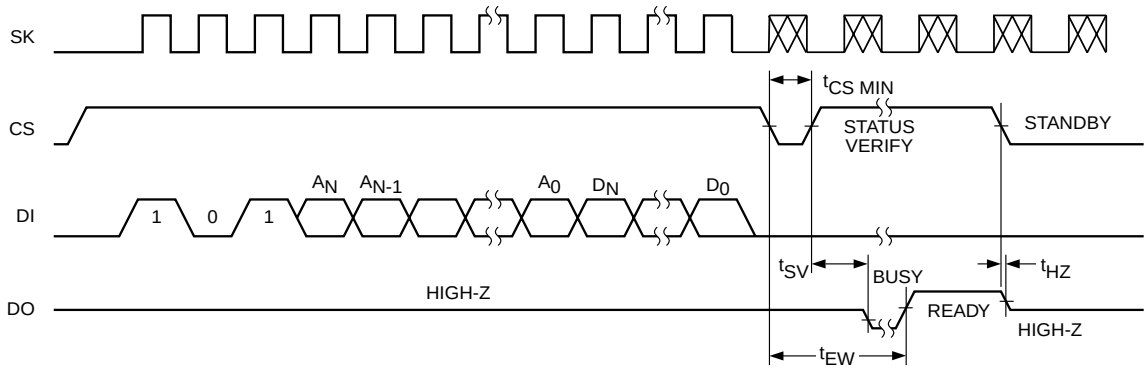


Figure 4. Erase Instruction Timing

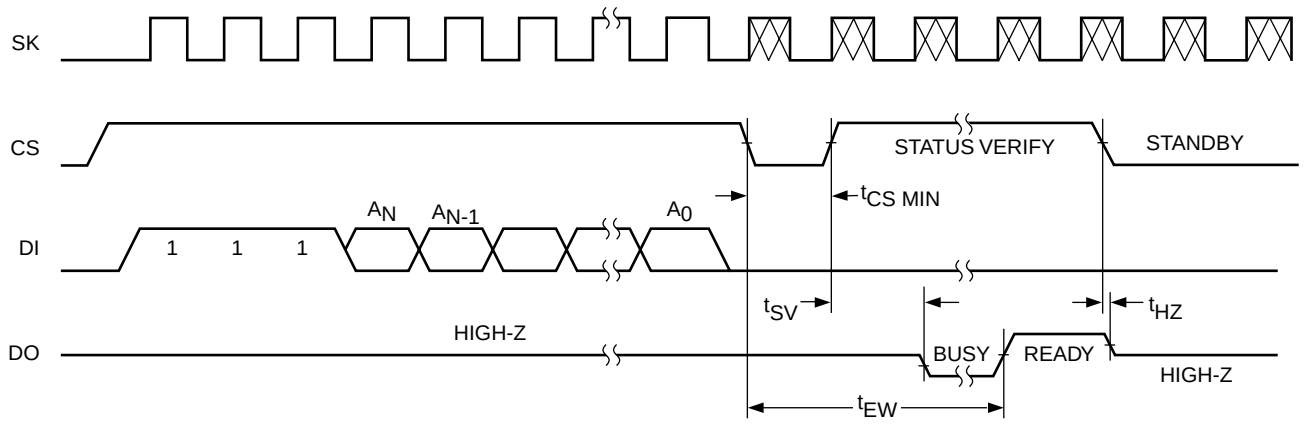


Figure 5. EWEN/EWDS Instruction Timing

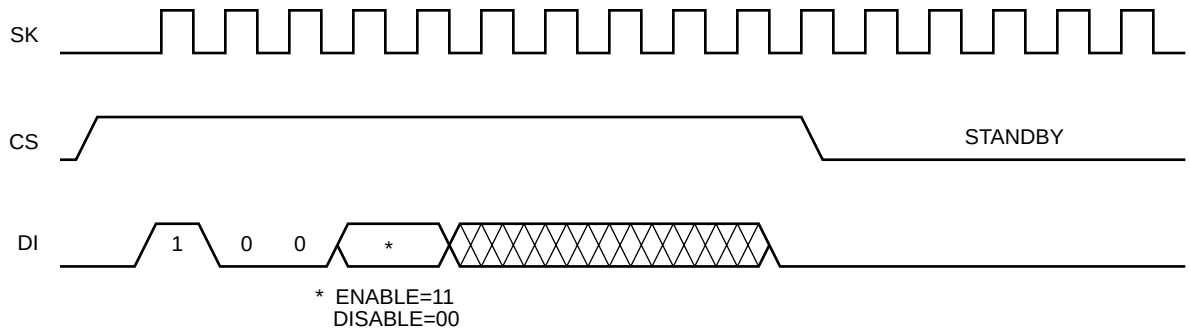


Figure 6. ERAL Instruction Timing

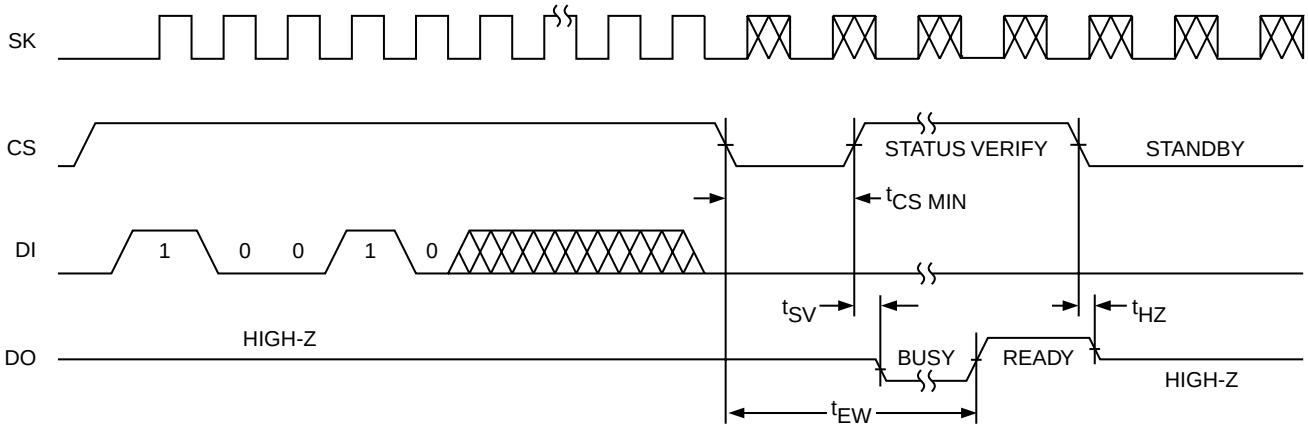
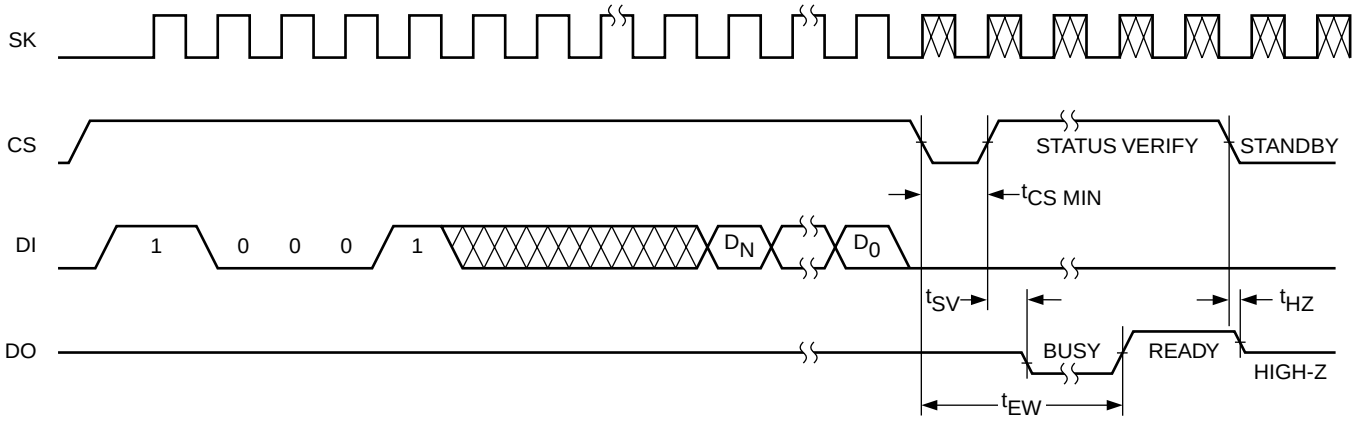
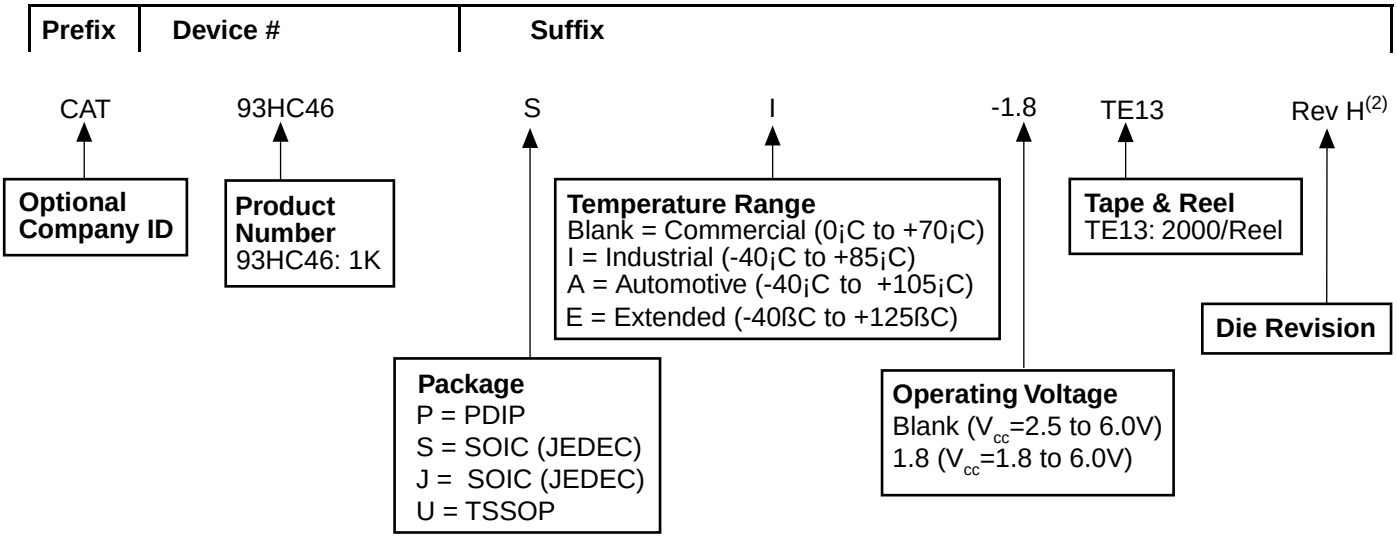


Figure 7. WRAL Instruction Timing



ORDERING INFORMATION



* available upon request

Notes:
(1) The device used in the above example is a 93HC46SI-TE13 (SOIC, Industrial Temperature,Tape & Reel).
(2) Product die revision letter is marked on top of the package as a suffix to the production date code (e.g., AYWWH.) For additional information, please contact your Catalyst sales office.

REVISION HISTORY

Date	Rev.	Reason
11/11/2003	E	Updated Features Eliminated Commercial temperature range Updated DC Operating Characteristics Updated AC Characteristics Updated Ordering Information
11/14/2003	F	Updated DC Operating Characteristics
7/27/2004	G	Add die revision to Ordering Information

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