DESCRIPTION

CB5717 is a highly integrated RF Front-End Integrated Circuit which incorporates key RF functionality needed for IEEE 802.11a/n/ac WLAN systems operating in the 5.15-5.9GHz range. CB5717 integrates a high-efficiency high-linearity power amplifier (PA), a low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters all in one device.

CB5717 has simple and low-voltage control logic, and requires minimal external components. A power detector is also integrated for accurate monitoring of output power from the PA.

CB5717 is assembled in a compact, low-profile 2.5x2.5x0.55mm 16-lead QFN package. CB5717 is the ideal RF front-end solution for implementing 5GHz high-power WLAN systems supporting multiple standards including 802.11ac.

BLOCK DIAGRAM

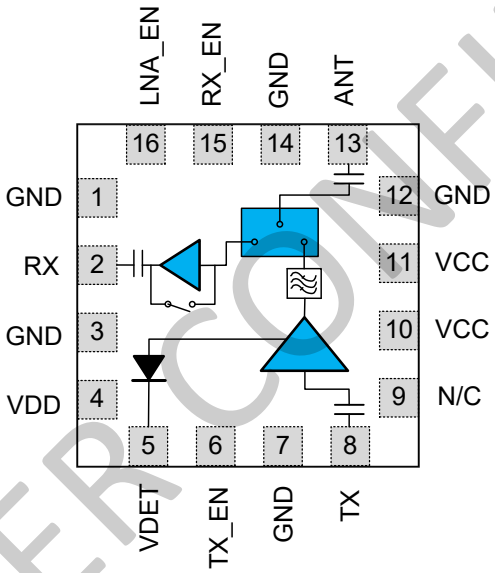


Figure 1. CB5717 Block Diagram

FEATURES

- Integrated high performance 5GHz PA, LNA with bypass and T/R switch
- Fully-matched input and output
- Integrated power detector
- Transmit gain: 28.5dB
- Receive gain: 10dB
- Output power: +20dBm @ 1.8% EVM, VHT80/MCS9, 5V
- Output power: +21dBm @ 3% EVM, HT40/MCS7, 5V
- Integrated 2.4GHz Notch Filter
- ESD protection circuitry on all PINs
- DC decoupled RF ports
- Minimal external components required
- Small package: QFN16 2.5mm x 2.5mm x0.55mm (MSL3, 260℃ per JEDEC J-STD-020)
- RoHS and REACH Compliant

APPLICATIONS

- 802.11ac Wi-Fi Devices
- Tablets / MIDs
- Wi-Fi Media Gateways
- Consumer Electronics s
- Notebook / Netbook / Ultrabook
- Access Points / Routers
- Set Top Boxes / Wireless IPTVs
- Other 5GHz ISM Platforms

PIN-OUT DIAGRAM

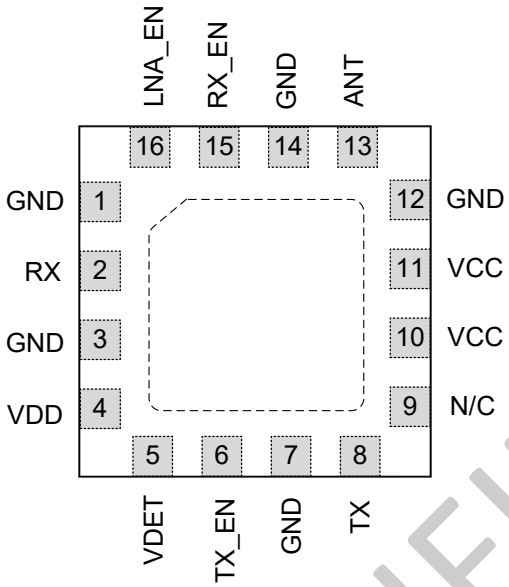


Figure 2. CB5717 Pin out (Top View)

PIN ASSIGNMENTS

Pin	Name	Description
1,3,7,12,14	GND	Ground – Must Be Connected to GND in the Application Circuit
2	RX	RF Output Port from LNA or Bypass
4	VDD	LNA/Switch/Regulator Supply Voltage
5	VDET	Analog Voltage Proportional to the PA Power Output
6	TX_EN	Input to Control TX Enable
8	TX	RF Input Port from the Transceiver
9	NC	Internally Not Connected
10,11	VCC	PA Supply Voltage
13	ANT	Antenna Port RF Signal from the PA or RF Signal Applied to the LNA
15	RX_EN	Input to Control RX Enable
16	LNA_EN	Input to Control LNA Enable or Bypass Mode

ABSOLUTE MAXIMUM RATINGS

Parameters	Test Condition	Minimum	Maximum	Units
DC Supply Voltage	VDD and VCC	0	6.0	V
Control Pin Voltage	All Control Pins	0	3.6	V
DC Current Consumption			600	mA
Input Power (50 ohm load)			+5	dBm
Storage Temperature		-40	150	°C
Operation Temperature		-40	85	°C
Junction Temperature			150	°C
ESD	All PINs, HBM		1000	V

NOTE:
Sustained operation at or above the Absolute Maximum Ratings for any one or combinations of the above parameters may result in permanent damage to the device and is not recommended. All Maximum RF Input Power Ratings assume 50-ohm terminal impedance.

RECOMMENDED OPERATING CONDITIONS

Parameters	Test Condition	Minimum	Typical	Maximum	Units
DC Supply Voltage	VDD and VCC	4.5	5.0	5.5	V
Control Pin Voltage “High”		2.0	3.0		V
Control Pin Voltage “Low”		0		0.3	V
Control Pin DC Current			50		uA
Operation Temperature		-40		85	°C

CB5717 ELECTRICAL SPECIFICATIONS[1]

Parameters	Symbol	Test Condition	Min	Typ.	Max	Units
Transmit Mode：(VDD=VCC= 5V, TX_EN=2.9V, RX_EN=LNA_EN=0V, T = 25℃, Unless Otherwise Noted)						
Frequency	f	Main Frequency Band	5.15		5.90	GHz
Gain	G		26.0	28.5		dB
Gain Flatness		Over Any 80MHz Bandwidth	-0.5		+0.5	dB
Output Power	POUT	With -45dB EVM source VHT160/MCS9, 1.8% DEVM, Preamble only VHT80/MCS9, 1.8% DEVM, Preamble only HT40/MCS7, 3% DEVM, Preamble Only HT20/MCS0, Mask Compliance	 +19.0 +19.5 +20.0 +22.0	 +19.5 +20.0 +21.0 +23.0		dBm
Current Consumption	ICC	CW Signal @ No RF @+20dBm		 305 340	 335 375	mA
Harmonics	 2fo 3fo	HT20/MCS0 Signal @ +23dBm 2nd harmonics 3rd harmonics		 -31 -42		dBm /MHz
Isolation	ISO	From ANT to either TX or RX Pin	-27	-30		dB
Input Return Loss	|S11|		-14	-17		dB
Output Return Loss	|S22|		-12	-15		dB
Power Detector Output	VDET	@ No RF @+20dBm		0.25 0.35	0.30 0.40	V
PA Switching Time	tSW	Shutdown←→TX		400	500	ns
Stability		All non-harmonically related outputs less than -36dBm/MHz		6:1		VSWR
Ruggedness		No Permanent Damage @ Pin =+10dBm		10:1		VSWR

Parameters	Symbol	Test Condition	Min	Typ.	Max	Units
Receive LNA Mode：(VDD=VCC= 5V, TX_EN=0V, RX_EN=LNA_EN=3V, T = 25℃, Unless Otherwise Noted)						
Frequency	f	Main Frequency Band	5.15		5.90	GHz
Gain	G		8	10		dB
Input 1dB Compression Point	Input P1dB		-2.0	-0.4		dBm
Gain Flatness		Over any 80MHz Bandwidth	-0.5		+0.5	dB
Noise Figure	NF			3.5	4.0	dB
Input Return Loss	|S11|		-11	-13		dB
Output Return Loss	|S22|	L	-4	-6		dB
3rd Order Input Intercept Point	IIP3			0		dBm
Switching Time	tSW	LNA←→TX		800		ns
Current Consumption	IDD	@ No RF		15	25	mA

Parameters	Symbol	Test Condition	Min	Typ.	Max	Units
Receive Bypass Mode：(VDD=VCC= 5V, TX_EN=LNA_EN=0V, RX_EN=3V, T = 25℃, Unless Otherwise Noted)						
Frequency	f	Main Frequency Band	5.15		5.90	GHz
Insertion Loss	I.L.			9	12	dB
Input 1dB Compression Point	Input P1dB			+8		dBm
Input Return Loss	|S11|		-10	-12		dB
Output Return Loss	|S22|		-8	-10		dB
3rd Order Input Intercept Point	IIP3			+15		dBm
Switching Time	tSW	Bypass ←→ LNA		100	200	ns
Current Consumption	IDD	@ No RF		13	18	uA

LOGIC TRUTH TABLE

Mode	TX_EN	LNA_EN	RX_EN
Shutdown Mode	0	0	0
Transmit Mode	1	0	0
LNA Low NF Receive Mode	0	1	1
Bypass Receive Mode	0	0	1
Unsupported	All Others		

NOTE:
1. “1” denotes high voltage state (=3.0V);
2. “0” denotes low voltage state (<0.3V) at Control Pins;
3. 1KΩ – 10KΩ series resistor may be required for each control line.

EVALUATION BOARD SCHEMATIC

The CB5717 Evaluation Board is used to test the performance of the CB5717 FEM. A suggested application schematic diagram is shown in Figure 3. A photograph of the Evaluation Board is shown in Figure 4.

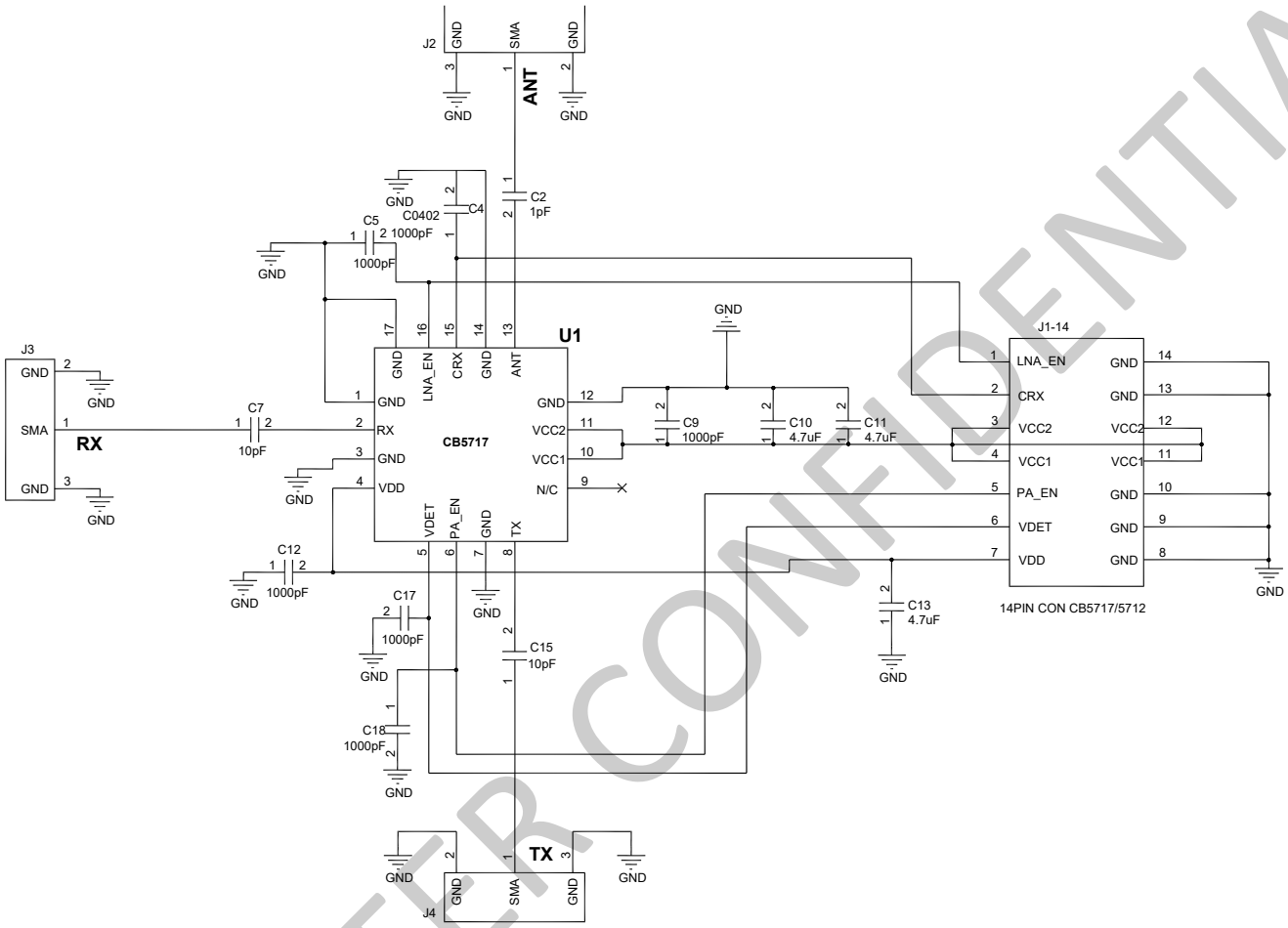


Figure 3. CB5717 Evaluation Board Schematic

EVALUATION BOARD ASSEMBLY DRAWING

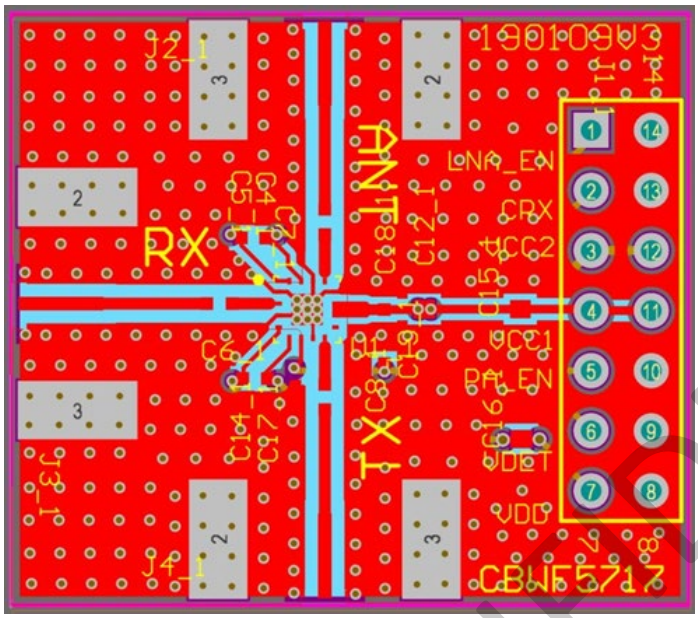
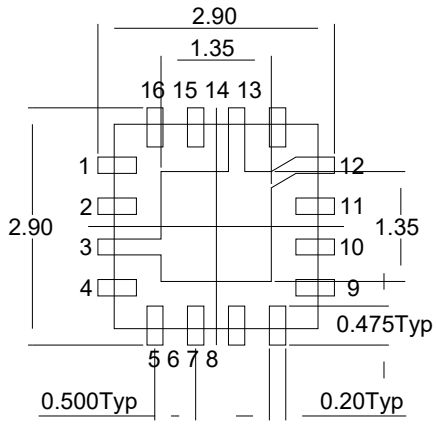


Figure 4. CB5717 Evaluation Board Assembly Drawing

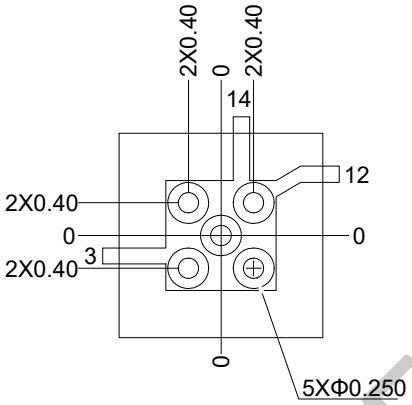
BILL OF MATERIALS

Component	Value	Size	Vendor	Part Number
C2	1pF	0402	Murata	GRM1555C1H1R0BA01#
C7, C15	10pF	0402	Murata	GRM1555C1H100FA01#
C4, C5, C9, C12, C17, C18	1000pF	0402	Murata	GRM1555C1H102GA01#
C10, C11, C13	4.7uF	0805	Murata	GRM21BC71H475KE11#

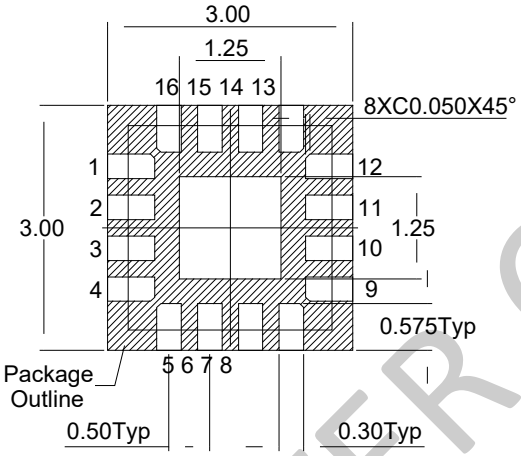
PCB LAND PATTERN



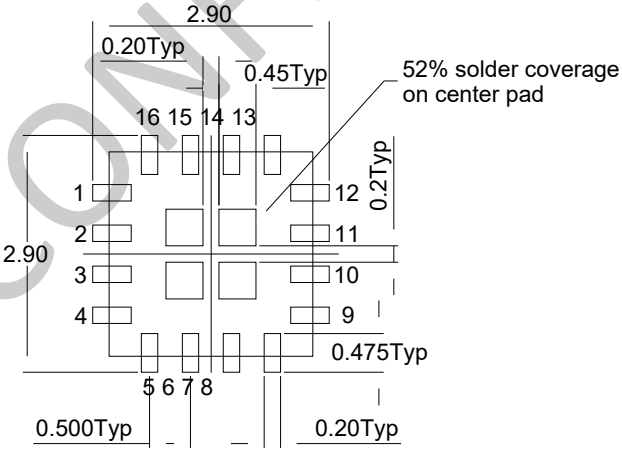
Board Metal



Via Pattern
(Note 4)



SolderMask Pattern
（Note 6)



Stencil Pattern
（Note 5)

Notes:
1.All dimens ions are in millim eters.
2.Dimens ioning and tolerancing according to ASME Y 14.5M-1994.
3.Unless speci fied,dimensions are symm etrical about center lines.
4.Via hole re commendations:0.025mm Cu via wall pl ating (minimum), solder mask on the far si de should te nt or plug via holes.
5.Stencil recommendations:0.10mm stencil thickness ,laser cut apertures,trapezoidal walls and roun ded corners offer b etter paste release.
6.Solder mask re commendations: contact board f abricator for recommended solder mask of fset and toleran ce.

Figure 5. CB5717 PCB Layout Footprint

TYPICAL PART MARKING

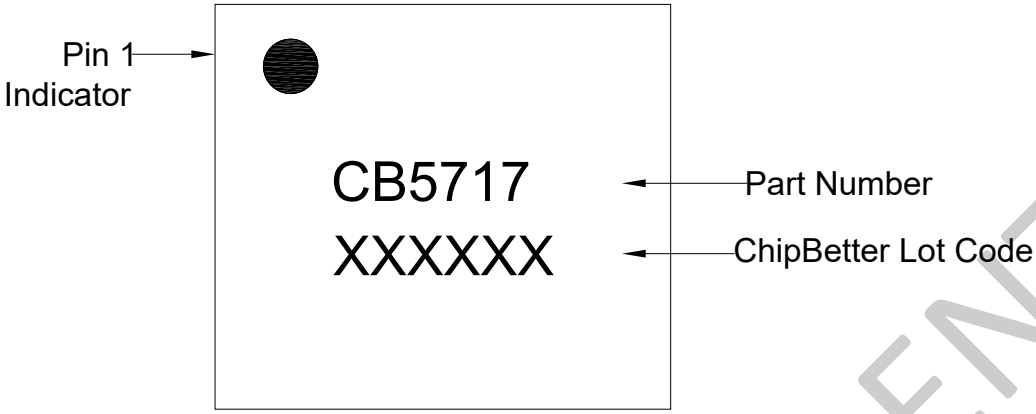
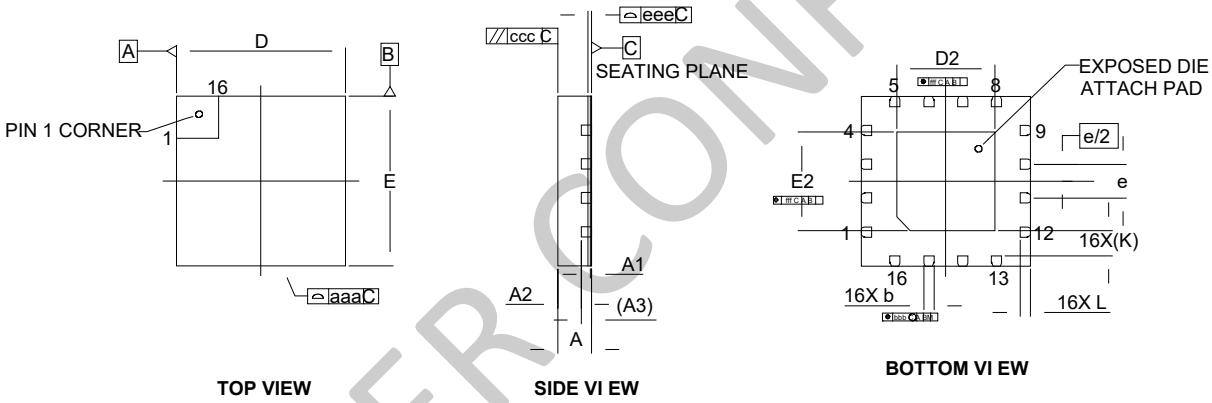


Figure 6. Typical Part Marking for the CB5717

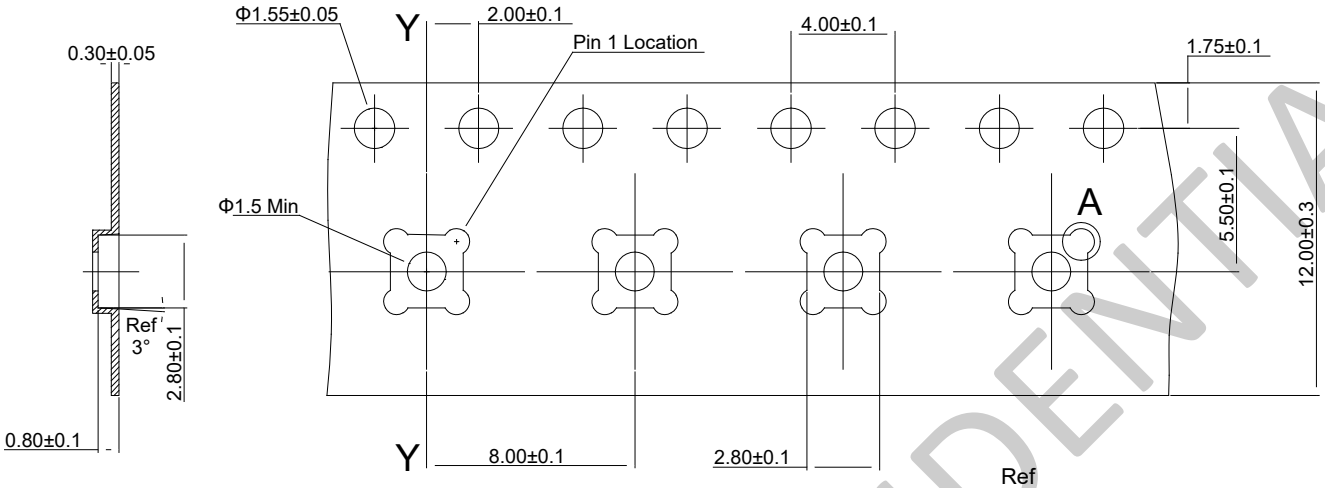
PACKAGE DIMENSIONS (All Dimensions in mm):



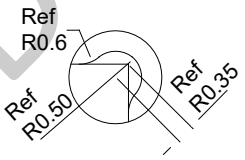
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.5	0.55	0.6
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.4	---
L/F THICKNESS		A3		0.152 REF	
LEAD WIDTH		b	0.15	0.20	0.25
BOOY SIZE	X	D		2.5 BSC	
	Y	E		2.5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	D2	1.45	1.55	1.65
	Y	E2	1.45	1.55	1.65
LEAD LENGTH		L	0.15	0.2	0.25
LEAD TIP TO EXPOSED PAD EDGE		K		0.275 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.1	
EXPOSED PAD OFFSET		fff		0.1	

Figure 7. CB5717 Package Dimension

TAPE AND REEL DIMENSIONS



Section Y-Y



Detail A

Notes:

1. Measured from center line of sprocket hole to center line of pocket.
2. Cumulative toelrance of 10 sprocket holes is ± 0.20mm.
3. Other material available.
4. Typical ESD surface resistivity is from 105 to 1011 Ohms/square per EIA,JEDEC tape and reel specification

All measurements are in millimeters.

Figure 8. CB5717 Tape and Reel Dimensions

CONTACT INFORMATION

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.chipbetter.com
Tel: 0755-26654180

DISCLAIMERS

ChipBetter reserves the right to make changes without further notice to specifications and product descriptions in this document to improve reliability, function or design. ChipBetter does not assume any liability arising out of the application or use of information or product described in this document. Neither does ChipBetter convey any license under its intellectual property rights nor licenses to any of circuits described in this document to any third party.
The information in this document is believed to be accurate and reliable and is provided on an "as is" basis, without any express or implied warranty. Any information given in this document does not constitute any warranty of merchantability or fitness for a particular use. The operation of this product is subject to the user's implementation and design practices. ChipBetter products are not designed or intended for use in life support equipment, devices or systems, or other critical applications, and are not authorized or warranted for such use.