CB664

I2C Clock Distribution Buffer for Three Banks of Mobile SDRAM

Approved Product

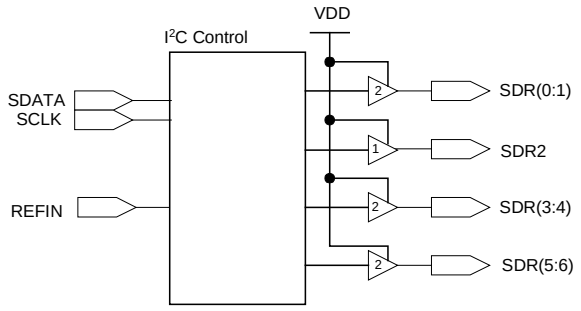
Product Features

- 7 output buffer for high clock fanout applications.
- Output may be individually disabled with I^2C
- VDD = 3.3 volts
- Output frequency range 10 MHz to 100 MHz
- <250ps skew between output clocks.
- 16-pin SSOP and TSSOP package.

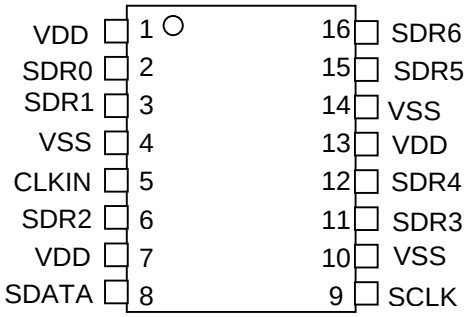
Product Description

The device is a high fanout system clock buffer. Its primary application is to distribute clocks needed to support a wide range of applications such as SDRAM clocks. This device provides low skew distribution clock heavily loaded. One important application of this component is where long traces are used to transport clocks from their generating devices to their loads. The creation of EMI and the degradation of waveform rise and fall times is greatly reduces by running a single reference clock trace to this device and then using it to these devices EMI is therefore minimized and board real estate is saved.

Block Diagram



Pin Configuration



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Pin Description

Pin No.	Pin Name	PWR	I/O	Type	Description
5	CLKIN	VDD	I	PAD	This pin is connected to the input reference clock. This clock be in the range of 10.0 to 100.0 MHz
2,3,6,11,12,15,16	SDR(0:6)	VDD	O	BUF1	Low Skew output clock.
8	SDATA	-	I/O	PAD	Serial data of I^2C-wire control interface. Has internal pull-up resistor.
9	SCLK	-	I	PAD	Serial data of I^2C-wire control interface. Has internal pull-up resistor
4,10,14	VSS	-	-	-	COMMON Ground
1,7,13	VDD	-	-	-	Power for output clock buffers and core logic

Maximum Ratings

Maximum Input Voltage Relative to VSS: VSS – 0.3V

Maximum Input Voltage Relative to VDD: VDD + 0.3V

Storage Temperature: 0^o to $+125^oC$

Operating Temperature: 0^o to $+70^oC$

Maximum Power Supply: 7V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precautions should be taken to avoid application of any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

VSS<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

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2-Wire I²C Control Interface

The 2-wire control interface implements a write only slave interface. The device control be read back. Sub-addressing is not supported, thus, all preceding bytes must be sent in order to change one of the control bytes. The 2-wire control interface allows each clock output to be individually enabled or disabled.

During normal data transfer, the SDATA signal only changes when the SDCLK signal is low, and is stable when SDCLK is high. There are two exceptions to this. A high to low transition on SDATA while SDCLK is high is used to indicate the start of a data transfer cycle. A low to high transition on SDATA while SDCLK is high indicates the end of data transfer cycle. Data is always sent as complete 8-bit bytes, after which an acknowledge is generated. The first byte of a transfer cycle is a 7-bit address with a read /write bit as the LSB. Data is being transferred MSB first.

The device respond to writes to 10 bytes (max) of data to address **D2** by generating the acknowledge (low) signal on the SDATA wire following reception of each byte. The device will not respond to any other control interface conditions.

Control Signal Registers

Note: The pin# column lists the affected pin number where applicable. The @Pup column gives the state at true power up. Bytes are set to the values shown only on true power up, and not when the PWR_DWN# pin is activated.

Following the acknowledge of the Address Byte (**D2)** two additional bytes must be sent:
1. "**Command Code"** byte and
2. **"Byte Count"** byte

Although the data (bits) in these two bytes are considered " don't care", they must be sent and will be acknowledge.

After the Command Code and the Count bytes have been acknowledge, the below described sequence (Byte0, Byte1, Byte2…) will be valid and acknowledged.

Byte 0: (1= Enable, 0= stopped)

Bit	@Pup	Pin #	Description
7	1	6	SDR2(Enable =1,stopped=0)
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	3	SDR1(Enable =1,stopped=0)
2	1	2	SDR0(Enable =1,stopped=0)
1	1	-	Reserved
0	1	-	Reserved

See application note AN664-01 for further reducing power consumption with I²C

Byte 1: (1= Enable, 0= stopped)

Bit	@Pup	Pin #	Description
7	1	16	SDR6 (enable=1,s topped=0)
6	1	15	SDR5 (enable=1, stopped=0)
5	1	-	Reserved
4	1	-	Reserved
3	1	12	SDR4 (enable=1, stopped=0)
2	1	11	SDR3 (enable=1, stopped=0)
1	1	-	Reserved
0	1	-	Reserved

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Electrical Characteristics

Characteristics	Symbol	Min	Typ	Max	Units	Conditions
Input Low Voltage	VIL	-	-	0.8	Vdc	-
Input High Voltage	VIH	2.0	-	-	Vdc	-
Input Low Current	IIL	-66			µA	
Input High Current	IIH			66	µA	
Tri-State leakage current	Ioz	-	-	10	µA	
Dynamic Supply Current (all outputs loaded with 30 pF)	Idd_{66}	9		100	mA	Input Frequency = 66 Mhz
	Idd_{100}	12	-	140	mA	Input Frequency =100 Mhz
Static Supply Current	Isdd	-	-	1	mA	All outputs disabled no input clock
Short Circuit Current	ISC	25	-	-	mA	1 input at a time – 30 seconds
Input Rise Time	VIR	2.4	-	-	nS	0.8 to 2.4 Volts
VDD =VDD1 thru VDD6 = 3.3V±5%, TA = 0°C to 70°C						

Switching Characteristics

Characteristics	Symbol	Min	Typ	Max	Units	Conditions
Output Duty Cycle	-	45	50	55	%	Measured at 1.5V (50/50 in)
Buffer Out/Out Skew all Buffer Outputs	TSKEW	-	-	250	pS	35 pF Load Measured at 1.5V
Buffer Input to Output Skew	TSKEW	2.0	0	5.0	nS	
Jitter Cycle to Cycle*	TJCC			50	pS	@35 pF loading
Jitter Absolute (Peak to Peak)*	TJabs			150	pS	@35 pF loading
VDD =VDD1 thru VDD6 = 3.3V±5%, TA = 0°C to 70°C						

***this jitter is additive to the input clock's jitter

Buffer Characteristics (All Clock Outputs)

Characteristics	Symbol	Min	Typ	Max	Units	Conditions
Pull-Up Current Min	IOH_{min}	-	-	-54	mA	Vout = 1.0 V
ull-Up Current Max	IOH_{max}	-	-	30	mA	Vout = 2.6 V
Pull-Down Current Min	IOL_{min}	-	-	54	mA	Vout = 1.2 V
Pull-Down Current Max	IOL_{max}	-	-	23	mA	Vout = 0.4 V
Rise/Fall Time Min Between 0.4V and 2.4V	TRF_{min}	-	-	1.33	nS	30 pF Load
Rise/Fall Time Max between 0.4V and 2.4V	TRF_{max}	-	-	1.33	nS	30 pF Load
VDD = VDDI thru VDD6 = 3.3V±5%, TA = 0°c TO +70°C						

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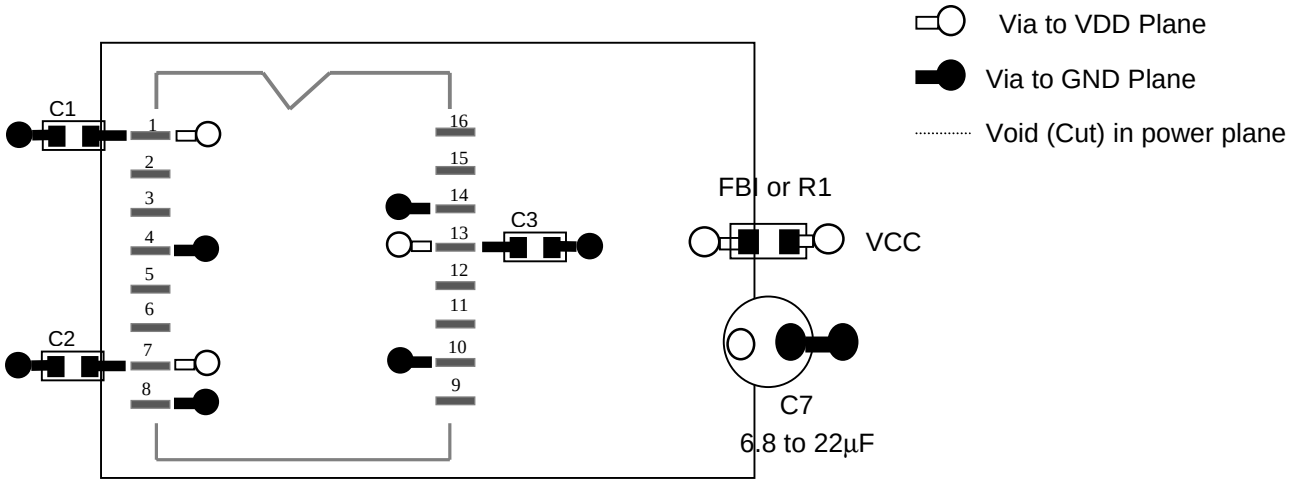
PCB Layout Suggestion



This is only a layout recommendation for best performance and lower EMI. The designer may choose a different approach but C1, C2, C3 (all are o.1µF) should always be used and placed as close to their VDD pins as is physically possible. FB1 or R1 is a ferrite Bead or resistor as needed to reduce conducted EMI from the device into the systems power circuitry.

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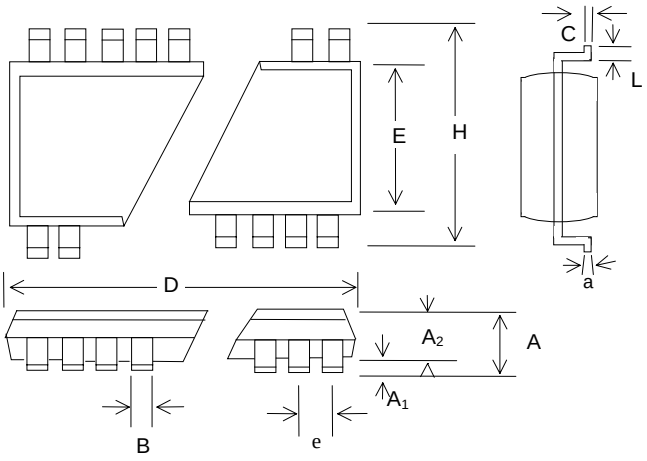
Package Drawing and Dimensions



16 Pin TSSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.047	-	-	1.20
A_1	0.002	-	0.006	0.05	-	0.15
A2	0.031	0.039	0.041	0.80	1.00	1.05
B	0.007	-	0.012	0.19	-	0.30
C	0.004	-	0.008	0.09	-	0.20
D	0.193	0.197	0.201	4.90	5.00	5.10
E	0.169	0.173	0.177	4.30	4.40	4.50
e	0.026 BSC			0.65 BSC		
H	0.244	0.252	0.260	6.20	6.40	6.60
L	0.018	0.024	0.030	0.45	0.60	0.75
a	0º	-	8º	0º	-	8º

16 Pin SSOP Outline Dimensions

	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	0.068	0.073	0.078	1.73	1.86	1.99
A_1	0.002	0.005	0.008	0.05	0.13	0.21
A2	0.066	0.068	0.070	1.68	1.73	1.78
B	0.010	0.012	0.015	0.25	0.30	0.38
C	0.005	0.006	0.009	0.13	0.15	0.22
D	0.239	0.244	0.249	6.07	6.20	6.33
E	0.205	0.209	0.212	5.20	5.30	5.38
e	0.0256BSC			0.65 BSC		
H	0.301	0.307	0.311	7.65	7.80	7.90
L	0.022	0.030	0.037	0.55	0.75	0.95
a	0°	4°	8°	0°	4°	8°

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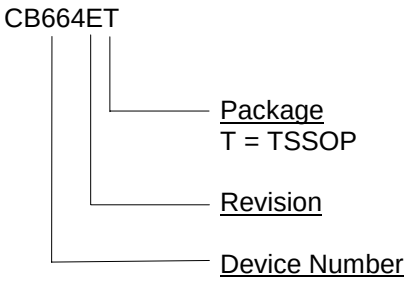
Ordering Information

Part Number	Package Type	Production Flow
CB664ET	16 Pin TSSOP	Commercial, 0ºC to +70ºC
CB664EY	16 Pin SSOP	Commercial, 0ºC to +70ºC

Note: The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: IMI, YYWWW
CB664ET
Lot #



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