Features

- Analog Power Supply Voltage: 3.0V to 3.3V
- Digital Power Supply Voltage: 2.5V to 3.3V
- Maximum Sampling Rate: 50MSPS
- Signal-to-Noise Ratio: ≥65dB
- Differential Nonlinearity Error: ±1.5LSB
- Power Consumption: ≤414mW
- Analog Input Range: 1VPP to 2VPP
- Circuit Interface: Parallel CMOS Level Interface
- ESD Rating: 1000V

Application

- High-end medical imaging equipment
- IF signal sampling for communication receivers
- Portable instruments
- Low-power digital oscilloscopes

Description

The CBM14AD50Q 14-bit 50MSPS A/D converter is a monolithic integrated circuit fabricated using CMOS technology. This product features a pipeline architecture and incorporates internal circuits such as a sample/hold amplifier, pipeline ADC, voltage reference, clock stabilization circuit, and mode selection logic.

Housed in a QFN-32 package with dimensions of 5.0mm (L) × 5.0mm (W) × 0.75mm (H), this device is a direct replacement for the AD9245 from Analog Devices (ADI).

Catalog

Block Diagram

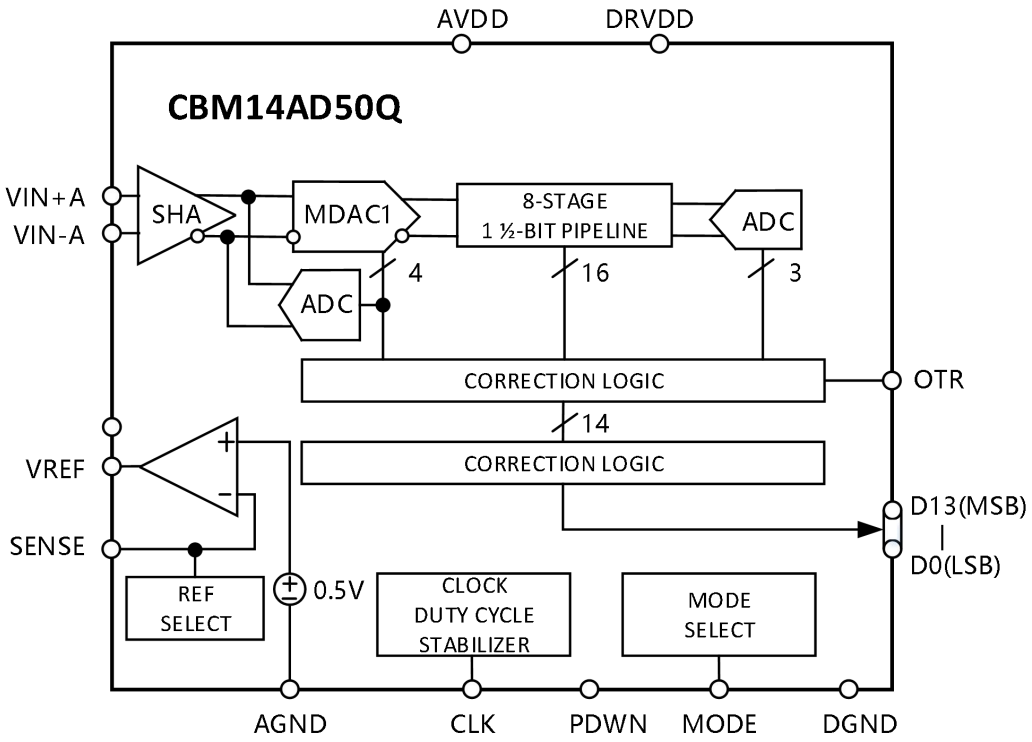


Figure 1. Block Diagram

Timing Sequence Diagram

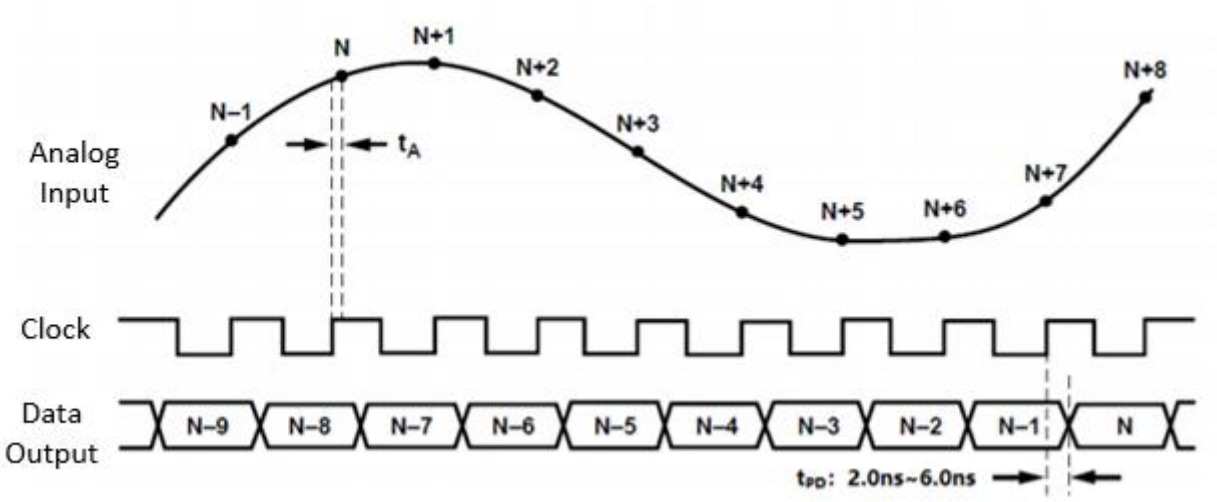


Figure 2. Timing Diagram

Parameter	Description	Min	Typ	Max
tA	aperture delay	--	1.4ns	--
tPD	Output delay	2.0ns	2.85ns	6.0ns
Latency	pipeline delay	--	7 Cycles	--

Pin Configuration

Terminations of 18-bit A/D converter is shown in Figure 4

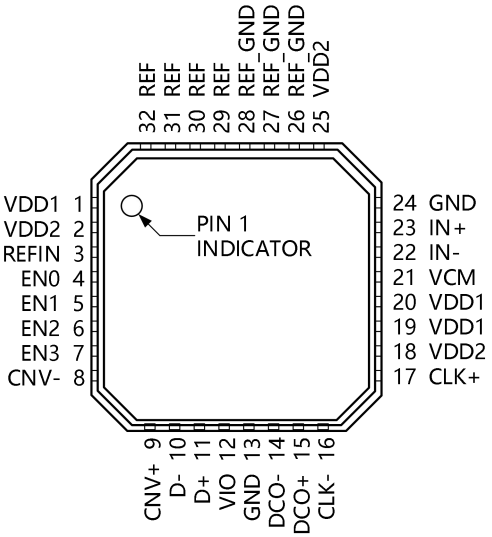


Figure 4 pin configuration

Pin Description

Pin Number	Symbol	Function	Pin Number	Symbol	Function
1	NC	Do Not Connect	17	D10	Data Output Bits D10
2	INCLK	Clock Input	18	D11	Data Output Bits D11
3	NC	Do Not Connect	19	D12	Data Output Bits D12
4	PDWN	Power-Down Function Select	20	D13	Data Output Bits D13 (MSB)
5	D0	Data Output Bits D0 (LSB)	21	OR	Out-of-Range Indicator
6	D1	Data Output Bits D1	22	MODE	Data Format Select and DCS Mode Selection
7	D2	Data Output Bits D2	23	SENSE	Reference Mode Selection
8	D3	Data Output Bits D3	24	VREF	Voltage Reference
9	D4	Data Output Bits D4	25	VREF-	Differential Reference (-)
10	D5	Data Output Bits D5	26	VREF+	Differential Reference (+)
11	D6	Data Output Bits D6	27	VDDA	Analog Power Supply
12	D7	Data Output Bits D7	28	GNDA	Analog Ground
13	D8	Data Output Bits D8	29	IN+	Analog Input Pin (+)
14	D9	Data Output Bits D9	30	IN-	Analog Input Pin (–)
15	GNDD	Digital Output Ground	31	GNDA	Analog Ground
16	VDDD	Digital Output Driver Supply	32	VDDA	Analog Power Supply
Note: heat sink connects analog source					

Recommended operation conditions

- Analog power supply voltage: 3.0V
- Digital power supply voltage: 2.5V
- Differential analog input voltage (Vp-p): 1V/2V
- Clock frequency range: 1MHz ~ 50MHz
- Operating ambient temperature: - 45℃ ~ 85℃

Absolute Maximum Ratings

- Power Supply Voltage: 3.9V
- Storage Temperature (TS): -55°C to 125°C
- Junction Temperature (Tj): 175°C
- Lead Soldering Temperature (TH, 10s): 300°C

Electrical characteristics

(Unless otherwise specified, VDDA=3V, VDDD=2.5V, f_{CLK}=50MHz, GNDA=GNDD=0V, f_{IN}=0.97MHz),MODE=PDWN=SENSE=0V, Internal 1V reference, differential analog input range 2VPP, -40 ℃ ≤ T_A ≤ 85 ℃)

parameter name	symbol	condition	performance index			Unit
			MIN	TYP	MAX	
Resolution	RES			14		Bits
Linear error	EL		-7.5	±3.4	7.5	LSB
Differential error	EDL		-1.5	±0.9	1.5	LSB
Offset error	EO		-1.2	±0.09	1.2	%FSR
Gain error	EG		-4.16	±0.75	4.16	%FSR
Reference output voltage	VREF		0.965	0.985	1.035	V
Digital output high level	VOH		2.4	2.5	--	V
Digital output low level	VOL		--	0.003	0.1	V
Analog Supply Current	IDDA		--	124	138	mA
Digital Supply Current	IDDD		--	6	10	mA
Power Dissipation	PD		--	390	414	mW

Signal-to-Noise Ratio	SNR		65	67.8	--	dB
Signal to noise distortion ratio	SINAD		64.5	67.5	--	dB
Spurious-Free dynamic Range (SFDR)	SFDR		70	82	--	dB
Slew Rate	SR		50	--	--	MSPS

Typical Characteristics (test diagram of electric characteristic)

1、Simulate FFT spectral lines under 1MHz input conditions

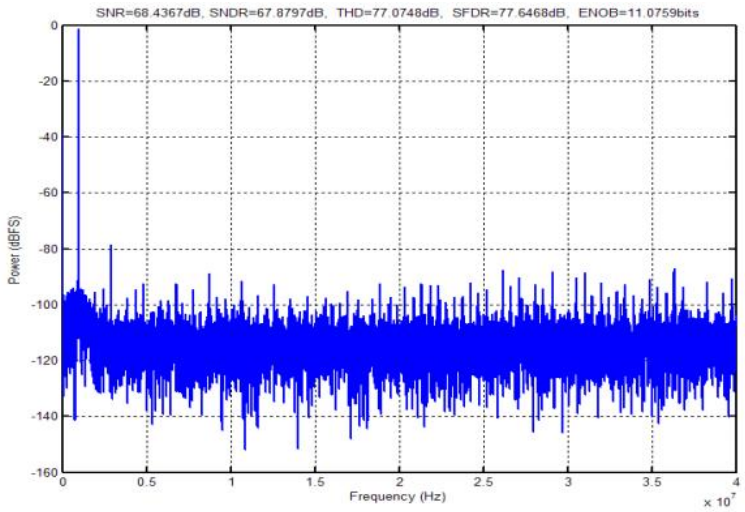


Figure 4. FCLK=50MHz, fin=1MHz FFT spectral line

2、Simulate FFT spectral lines under 10MHz input conditions

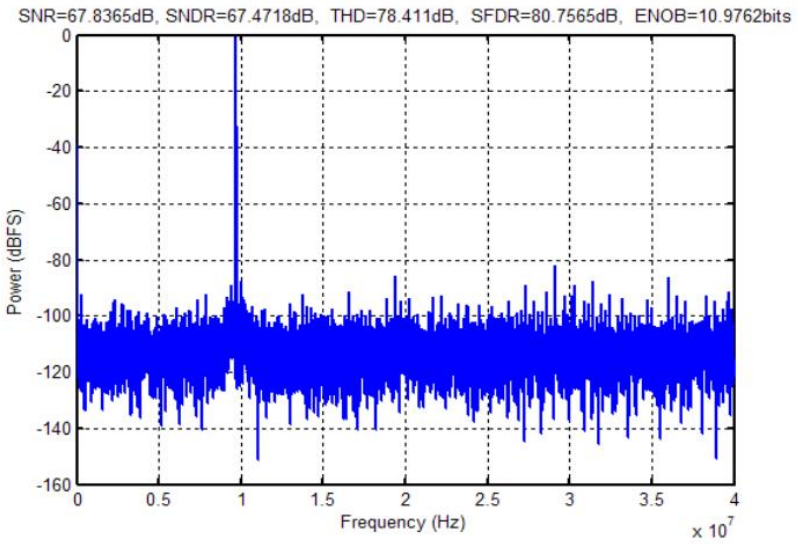


Figure 5. FCLK=50MHz, fin=10MHz FFT spectral lines

3、Differential Error (EDL) Test Curve

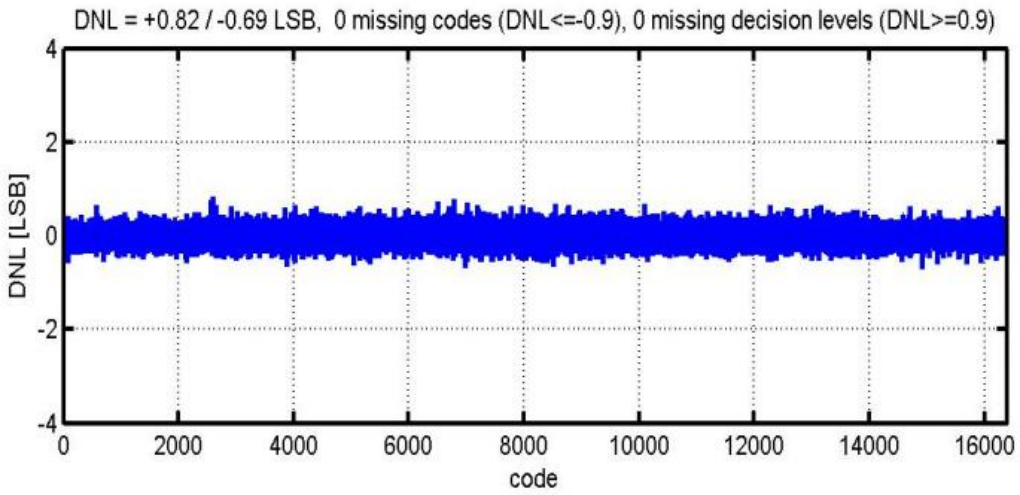


Figure 6. Differential Error (EDL) Test Curve

4、Linear Error (EL) Curve

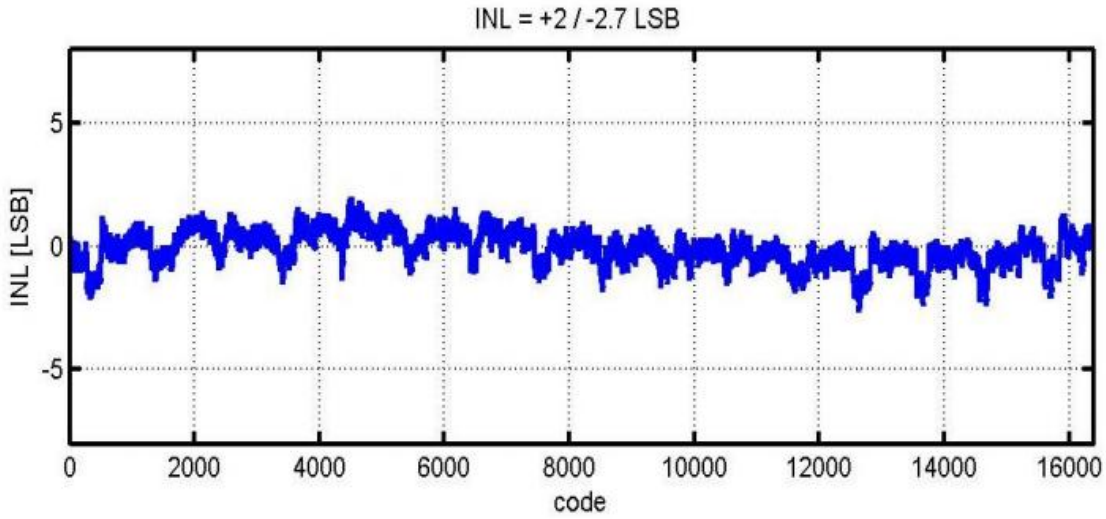


Figure 7 Linear Error (EL) Curve

Typical application circuit diagram

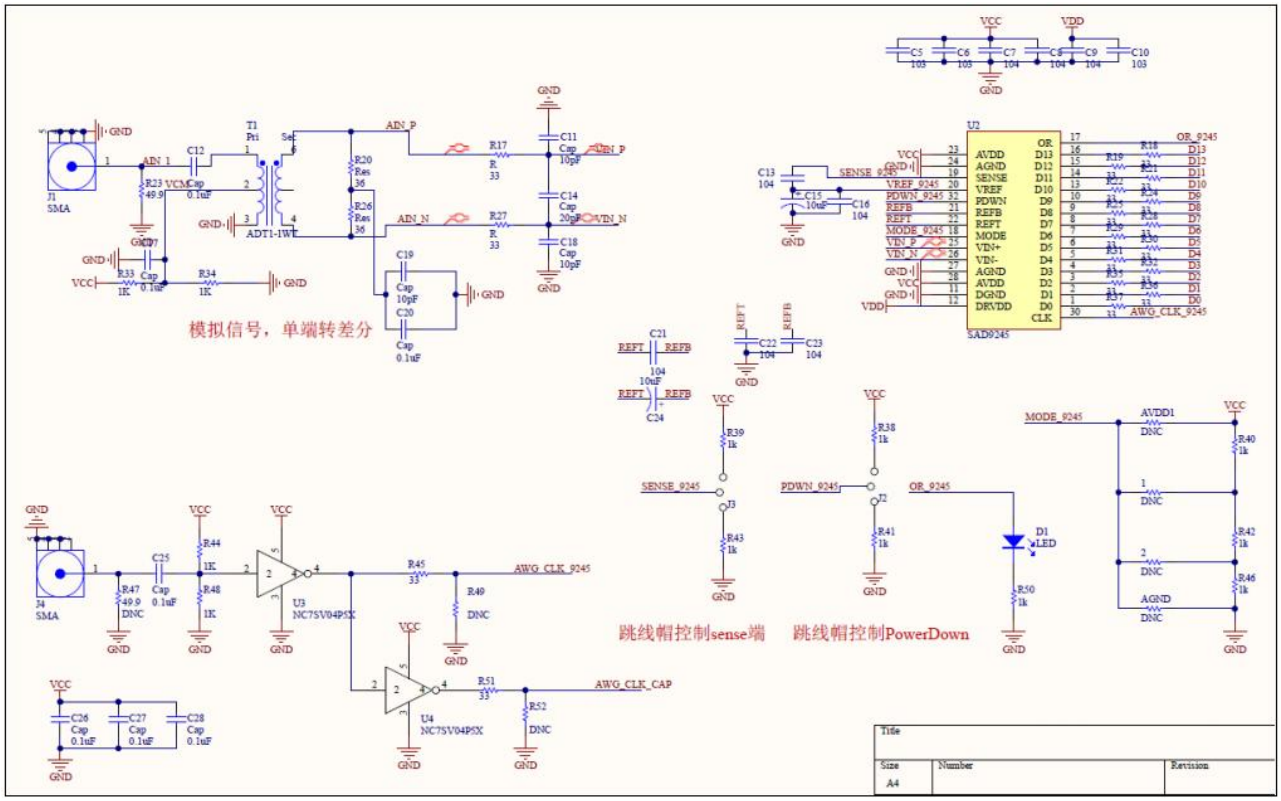


Figure 8 Main Circuit Diagram of CBM14AD50Q

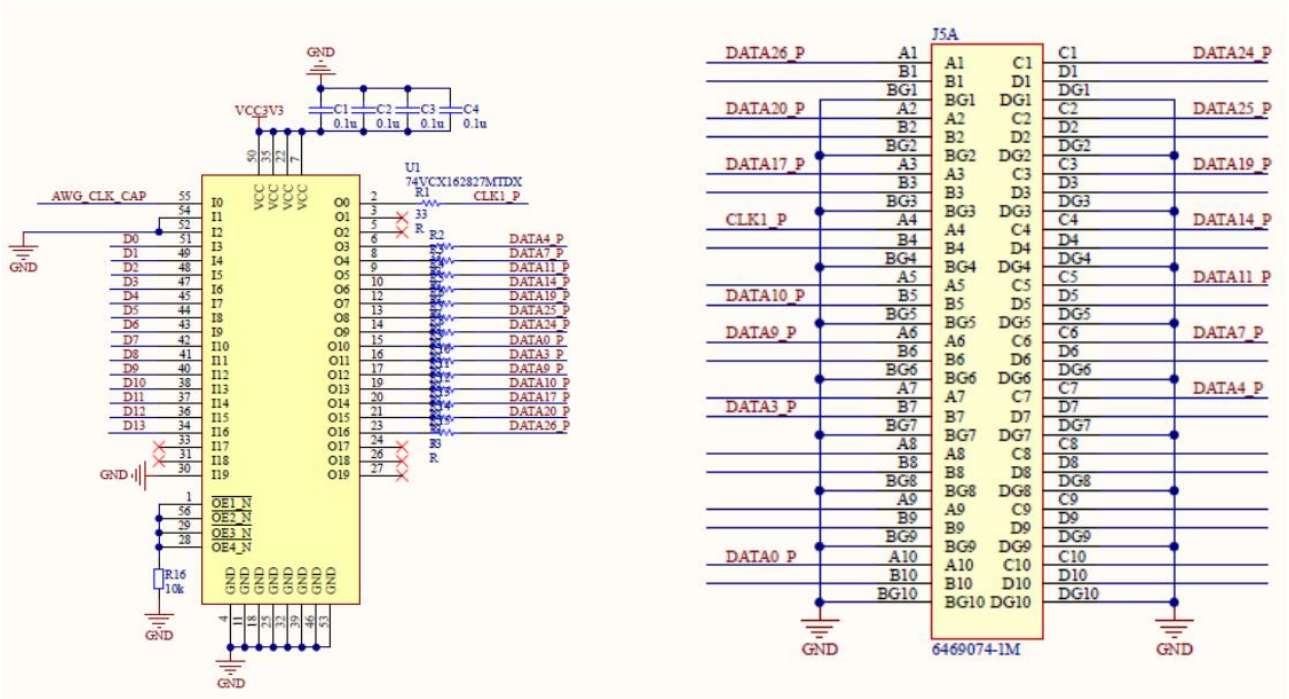


Figure 9 Buffer Buffer and FPGA Interface Circuit Diagram

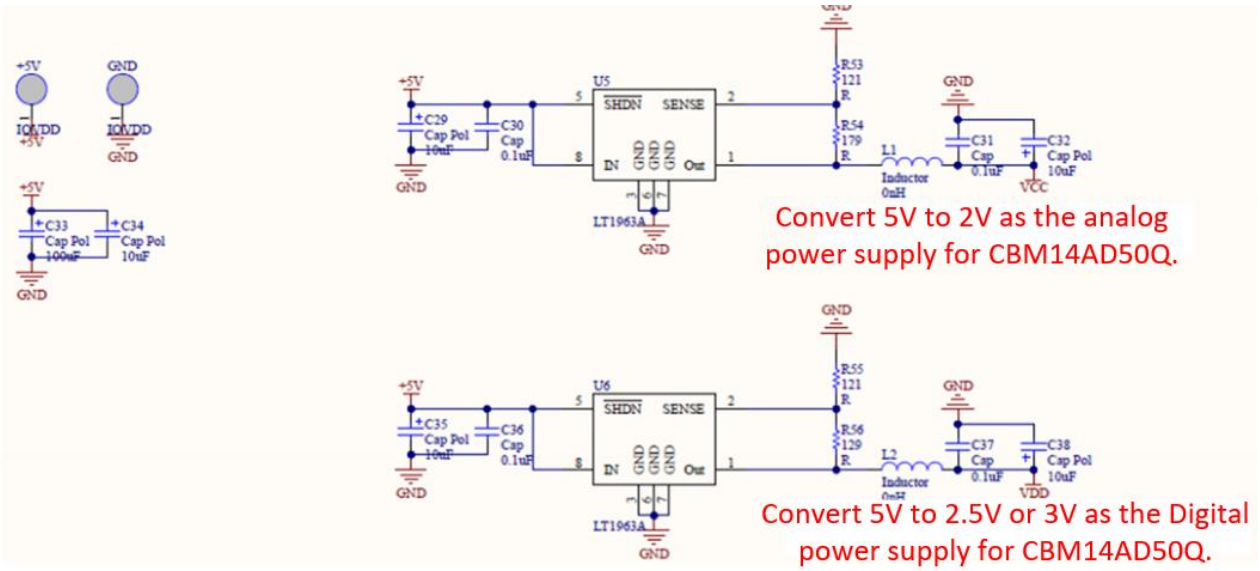


Figure 10. Power module circuit diagram

1. Analog input range and reference voltage selection

The analog input range of CBM14AD50Q is 1VPP~2VPP, and the reference voltage can be adjusted according to the analog input range. A stable and accurate reference voltage is generated inside the circuit, which can be selected as an internal reference or an external reference. The reference voltage value can also be determined through programming (see Figure 11). The usage is controlled by the reference voltage selection terminal SENSE. The analog input range and reference voltage selection are shown in Table 1.

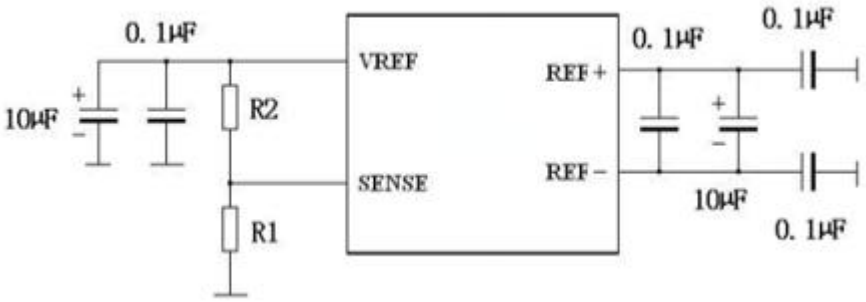


Figure 11 Programmable reference voltage usage connection diagram

Table 1 .Analog Input Range and Reference Voltage Selection Connection Table

Operating mode	SENSE	Reference voltage output VREF	Differential analog input peak voltage VPP
External reference voltage	VDDA	--	2 x additional reference voltage
Fixed internal reference voltage	VREF	0.5V	1.0V

Programmable reference voltage	0.2V ~ VREF	0.5V×(1+R2/R1)	2×VREF
Fixed internal reference voltage	≤0.2V	1.0V	2.0V

2. Power saving mode

This product is equipped with a power-saving mode control terminal PDWN. When PDWN is high, the circuit is in power-saving mode and has only 15mW

Power consumption, with each output in a high impedance state; When PDWN is low, the circuit is in normal working condition. The power-saving mode control is shown in Table 2.

Table 2 CBM 92AD45 Power saving Mode Control Table

PDWN	Function
H	power-saving mode
L	Normal operation

Note: The PDWN control level is at the CMOS level and is suspended at a low level (L).

3. Output data format and clock stability function

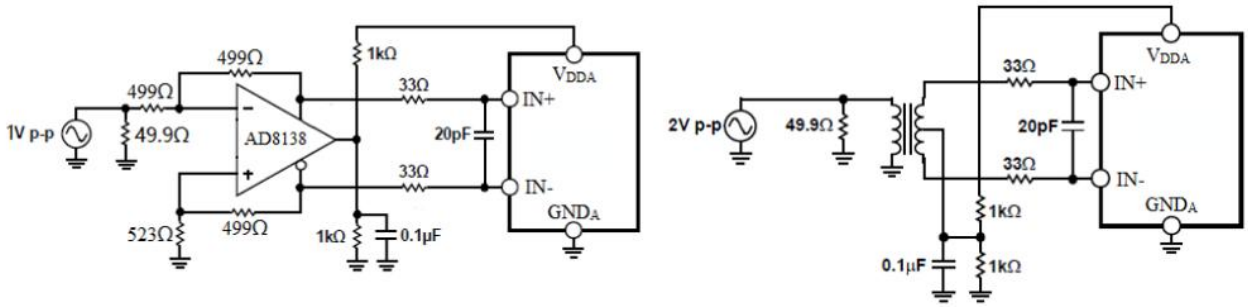
The output data of CBM14AD50Q has two formats: binary complement code and binary offset code. Users can control them through MODE as needed; The circuit contains a clock stabilization circuit, which can also be selected through MODE and controlled as shown in Table 3.

Table 3 .CBM 92AD45 Output Data Format and Clock Stability Function Control Table

MODE	Output data format	Clock stability function
VDDA	Binary complement	Off
2/3 VDDA	Binary complement	On
1/3 VDDA	Binary offset code	On
GNDA(Default)	Binary offset code	Off

4. Analog input

The CBM14AD50Q analog input can be in the form of differential input or single ended input. Differential input mode can be used Amplifier driver, or transformer driver, as shown in Figure 12. The single ended input structure is shown in Figure 13.



(a) Amplifier driver (b) Transformer driven

Figure 12. CBM14AD50Q differential input structure

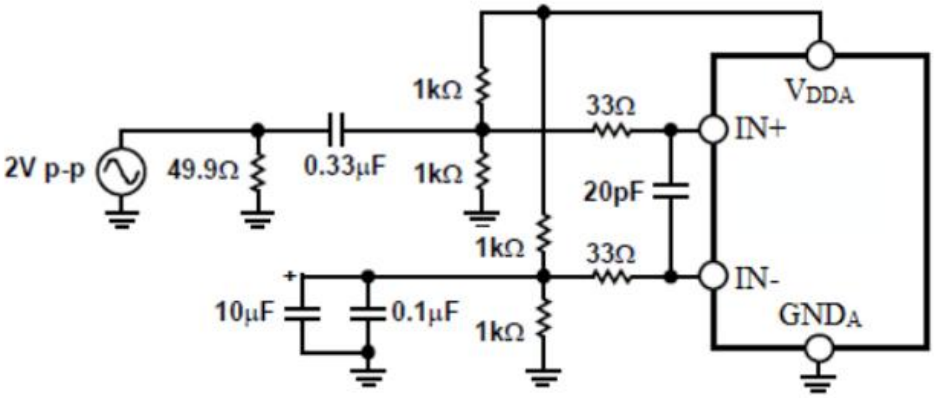


Figure 13. CBM14AD50Q single ended input structure

Package Outline Dimensions

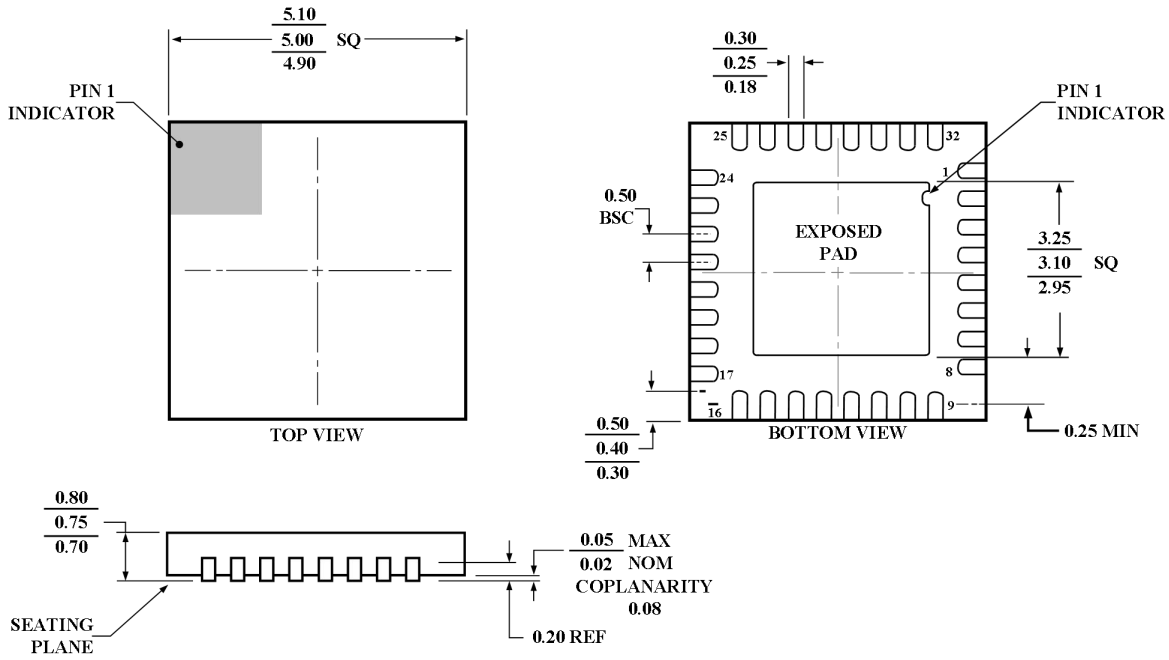


Figure 14. Package Outline Dimensions

Matters Need Attention

1. Product Installation Precautions

（1）Component Orientation during Soldering: Pay attention to the device's orientation to avoid soldering errors.

（2）Grounding and Decoupling:Instruments used for circuit debugging must have a good unified grounding.

Ensure proper grounding and power decoupling in the PCB design.

（3）Power Connection: Avoid reverse power supply connections or short circuits between input/output terminals and the power supply, as this may cause circuit damage.

（4）Electronics Assembly Instructions:

① Moisture Sensitivity Level (MSL): This product has an MSL3 rating. After removing it from the moisture-proof bag, the allowable exposure time to the external environment before dry storage or reflow soldering is: ≤168 hours at ≤30°C/60% RH (workshop lifetime).

② Pre-Baking Requirement: If the product is not stored in a dry environment before assembly, it must be baked at 125°C for 12–24 hours to remove internal moisture. (Note: After baking, the environment is extremely dry, making static electricity highly likely. ESD protection is required.)

③ Lead-Based Reflow Soldering (Sn63Pb37):Recommended peak temperature range: 210°C–230°C.Maximum peak temperature should not exceed 245°C.Dwell time within ±5°C of the peak temperature: ≤20 seconds.Time above liquidus temperature: 60–90 seconds.Heating rate: ≤3°C/s; cooling rate: ≤6°C/s.

④ Lead-Free Reflow Soldering (SAC305):Recommended peak temperature range: 230°C–245°C. Maximum peak temperature should not exceed 260°C.Dwell time within ±5°C of the peak temperature: ≤20 seconds.Time above liquidus temperature: 60–90 seconds.Heating rate: ≤3°C/s; cooling rate: ≤6°C/s.

⑤ Surface Finish of Soldering Terminals: Electroplated pure tin.

⑥ Side Pads: The side pads are bare copper and do not have soldering wettability. Soldering or solder climbing on the sides is not required.

2. Product Usage Precautions

（1） Power-Up Sequence: It is recommended to power on the analog and digital supplies simultaneously or power on the analog supply first.

（2） Logic Input Levels: To ensure dynamic performance, maintain logic high ≥2.8V and logic low ≤0.2V for input ports (INCLK, PDWN).

（3） Op-Amp Compatibility: When using an op-amp with CBM14AD50Q, ensure its output swing exceeds the ADC’ s analog input range (2VPP) to preserve signal integrity.

（4） Reference Decoupling: Use low-ESR capacitors for decoupling at the reference outputs (VREF, VREF+, VREF-).

（5） In applications, it is recommended to use a large-area ground plane on the PCB. This can eliminate potential differences that may exist due to different grounding points, while reducing the impact of capacitance generated by the circuit board on the circuit.

（6） Power Decoupling: Place a 1μF or 0.1μF capacitor adjacent to each power pin.

（7） Differential Input Traces: Match the lengths of differential input traces to maintain signal balance.

（8） Power Domain Separation: Isolate analog and digital power supplies.

（9） Digital Output Traces: Keep digital output traces short and terminate with a digital driver.

3. Product Protection Precautions

ESD Sensitivity: Class 1C (≤2,000V HBM). Use ESD protection during testing, handling, and storage.Storage Environment: Store at 10–25°C and 25–70% relative humidity.

Common Failure Treatment method

1. No Output Signal

Check for clock input at the clock output pin.Verify power supply and ground connections are correct.Ensure input voltage and reference voltage are accurate.

2. Output Data Jitter

Inspect external circuitry and connections.Stabilize the reference voltage to minimize fluctuations.

3. Device Operational Instability

Check the power supply for voltage stability.Ensure proper decoupling capacitors are installed.

Package/Ordering Information

MODEL	ORDERING NUMBER	TEMPERATURE	PACKAGE DESCRIPTION	PACEAGE OPTION	MAKING INFORMATION
CBM14AD50Q		-40℃~85℃	QFN-32	Tray，490	

Revision Log

Version	Revision date	Change content	Reason for Change	Modified by	Reviewed By	Note
V1.0	2025.1.20			WW	LYL	Initial version
V1.1	2025.6.23	Product description error update	Error Update	WW	LYL	