CBM2093

USB 2.0 Flash Disk Controller

Datasheet

Rev 1.0

Revision History

Date	Rev No	Descrption
2009-05-12	1.0	Initial release

Contents

1 DESCRIPTION 4
2 FEATURES 4
3 BLOCK DIAGRAM 6
4 PIN ASSIGNMENT 7
4.1 TQFP48 (TOP SIDE) 7
5 PIN DESCRIPTION 8
6 ELECTRICAL CHARACTERISTICS 11
6.1 ABSOLUTE MAXIMUM RATINGS 11
6.2 RECOMMENDED OPERATING CONDITIONS 11
6.3 STATIC CHARACTERISTICS 11
6.4 DYNAMIC CHARACTERISTICS 12
7 MECHANICAL DIMENSIONS 14
7.1 48-PIN CBM2093 PACKAGE OUTLINE DIMENSION 14
8 COPYRIGHT NOTICE 15

1 Description

Fastest & Securest USB 2.0 Flash Disk Controller with dedicated 32-bit microprocessor

The CBM2093 is the USB 2.0 Flash Disk controller with the fastest transfer speed on the market. CBM2093 can reach theoretical flash access speed limit of over 32MByte/s for read and 20MByte/s for write.

The on-the-fly ECC engine is capable of correcting up to 8/15bits per 512 bytes page . For data security, CBM2093 is designed with both hardware and software data protection technology to prevent data corruption even if it is powered off or unplugged during data transfer.

The CBM2093 supports all 8 /16 bit BUS wide NAND flash memory available in the market. New flash can be supported by software re-configuration.

The CBM2093 has both a) 5V to 3.3V LDO and b) power on reset circuits integrated. Thus greatly reduced BOM cost and eased layout burden.

The CBM2093 runs smoothly with all available hosts and PC platforms. Complied with USB specification rev. 2.0, the CBM2093 can be supported without additional driver under Win XP, Win 2000, Windows Me, Mac OS and Linux OS. With device driver installed, it can support Win 98/98SE as well. Comprehensive applications, such as PC boot up, disk partitions, password check for security disk, are available as part of our standard mass production software package.

The CBM2093 is available in 48-pin TQFP and 64-pin LQFP package, which are thinnest and smallest on the market. The 48-pin CBM2093 supports up to 4 flash chips and the 64-pin CBM2093 supports up to 8 flash chips. Customers can choose different packages to meet their design requirement.

2 Features

- **USB Interface**

  High-speed USB 2.0 interface;

- **Fastest data transfer rate on the market**

  Dual-channel mode: 32MB/s for Read, 20MB/s for Write
  Single-channel mode: 26MB/s for Read, 20MB/s for Write
  Fastest file copy rate on the market.

- **On-the-fly ECC built-in Hardware enhances reliability**

  ECC for SLC NAND flash: 8 bit per page (1 page = 512 bytes)
  ECC for MLC NAND flash: 8/15 bit per page

- **Special wear leveling algorithm to improve the flash life-time**

- **Hardware & Software Data Protection Technology**

  Prevent data corruption even if it is powered off or unplugged during data transfer.

- **NAND, SLC/MLC Flash Interface**

  Support 4k page flash parallel mode.
  Support 8-bit and 16-bit Samsung SLC and MLC NAND flash.
  Support 8-bit and 16-bit Toshiba SLC and MLC NAND flash.
  Support 8-bit and 16-bit Hynix SLC and MLC NAND flash.
  Support 8-bit and 16-bit Micron/Intel SLC and MLC NAND flash.
  Support 8-bit and 16-bit ST/Numony SLC and MLC NAND flash.
  Support 8-bit and 16-bit Infineon SLC and MLC NAND flash.
  Support 8-bit and 16-bit Sandisk SLC and MLC NAND flash.
  Support PowerChip SLC & MLC Nand Flash
  Support Spansion 3.3V MirrorBit-Quad Flash
  Support SMIC Double Density Flash
  Support Actrans Nand Flash
  Software configuration to support various new flash memories
  Supports up to 8 flash chips.

- **Proprietary 32-bit CISC microprocessor feature**

  Proprietary 32-bit CISC processor for USB protocol processing and flash access.

  Single cycle instruction period

- **Integrated 5v to 3.3v voltage regulator**
- **Disk partitions and password check for security disk available**
- **PC boot up as USB Zip Disk, USB Hard Disk or USB CDROM**
- **Auto run function**
- **Low power dissipation**

  Operating current 50mA (Bus power compatible)

- **Build-in LDO**

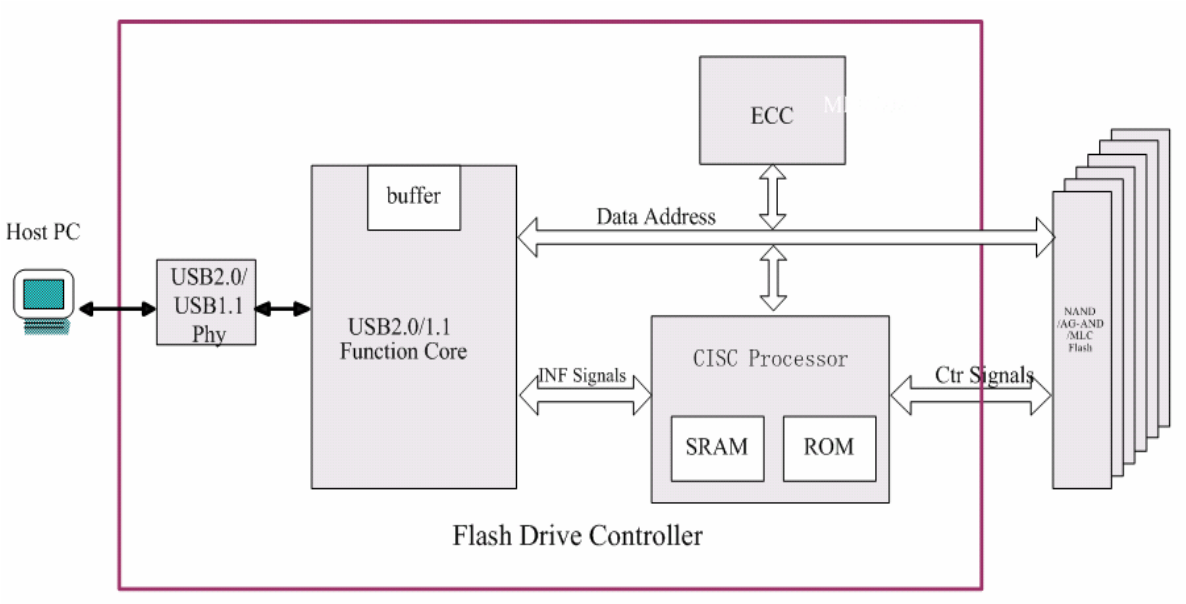
  Output maximum current up to 300mA

- **Leading 0.18um CMOS technology**
- **48-pin TQFP /64-pin LQFP package**

  48-pin CBM2093 supports up to 4 Flash Chips

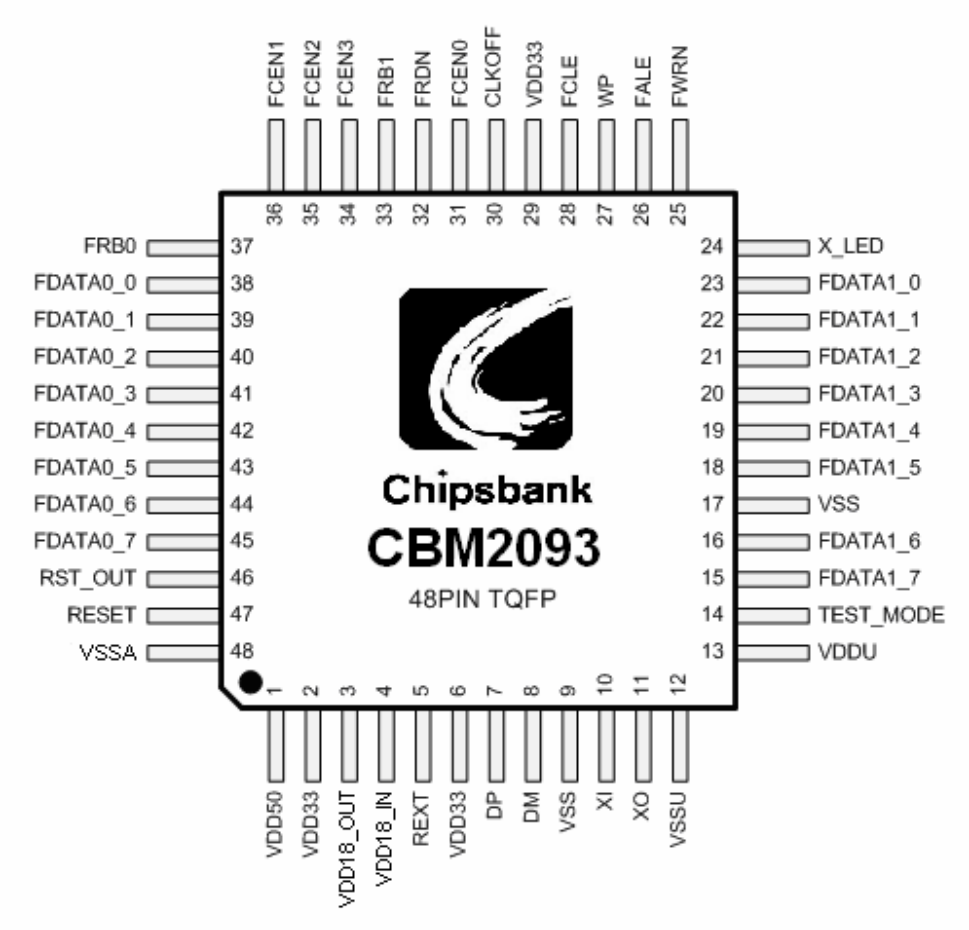
- **Windows, Mac and Linux compatible**

3 Block Diagram



4 Pin Assignment

4.1 TQFP48 (Top Side)



5 Pin Description

Brief CBM2093 pin functions are shown in the following tables.

I: Input signal

O: Output signal

I/O: Bi-direction signal

PWR: Power signal

GND: Ground signal

PU: pull up

PD: pull down

CBM2093 TQFP48 Pin Description

TQFP48 Pin No.	Pin Name	Type	Description
1	VDD50	PWR	Regulator5V Power Input
2	VDD33	PWR	Regulator 3.3V Power OUT
3	VDD18_OUT	PWR	Regulator 1.8V Out
4	VDD18_IN	PWR	CORE 1.8V in
5	REXT	I	Connect External Resister for current reference
6	VDD33	PWR	Padring 3.3V Power
7	DP	I/O	USB Data D+
8	DM	I/O	USB Data D-
9	VSS	GND	Padring 3.3V / Logic 1.8V Ground
10	XI	I	Crystal Input (12 MHz)
11	XO	O	Crystal Output
12	VSSU	GND	Analog 1.8V Ground
13	VDDU	PWR	Analog 1.8V Power
14	TEST_MODE	I PD	Test Mode Enable Pin When high , test mode When low , normal mode
15	FDATA1_7 GPIO15	I/O PU	Group 1 Flash Data Bus - bit 7 General I/O port 15

			When select spi mode ,as spi chip select . (configure as GPIO and clear pin_64(detail in spi_ctl[13] .when select master mode , configure output , otherwise, configure as input.).
16	FDATA1_6 GPIO14	I/O PU	Group 1 Flash Data Bus - bit 6 General I/O port 14 When select spi mode, as clock out support ligh-tun sensor (configure as GPIO and clear pin_64(detail in spi_ctl[13] .when select ligh-tun mode , configure output).
17	VSS	GND	Padring 3.3V / Logic 1.8V Ground
18	FDATA1_5 GPIO13	I/O PU	Group 1 Flash Data Bus - bit 5 General I/O port 13
19	FDATA1_4 GPIO12	I/O PU	Group 1 Flash Data Bus - bit 4 General I/O port 12
20	FDATA1_3 GPIO11	I/O PU	Group 1 Flash Data Bus - bit 3 General I/O port 11
21	FDATA1_2 GPIO10	I/O PU	Group 1 Flash Data Bus - bit 2 General I/O port 10
22	FDATA1_1 GPIO9	I/O PU	Group 1 Flash Data Bus - bit 1 General I/O port 9
23	FDATA1_0 GPIO8	I/O PU	Group 1 Flash Data Bus - bit 0 General I/O port 8
24	X_LED	I/O	When TEST_MODE =1, as scan clock input. When TEST_MODE =0, as LED Indication
25	FWRN	O	Group Flash Write Enable (active low)
26	FALE	O	Group Flash Address Latch Enable
27	WP	I	Write Protect Switch Input
28	FCLE	O	Group Flash Command Latch Enable
29	VDD33	PWR	Padring 3.3V Power
30	CLKOFF	I PD	Clock input switch. CLK_OFF=1, select external test clock.
31	FCEN0	O	Flash Chip Enable - Chip 0 (active low)
32	FRDN	O	Group Flash Read Enable (active low)
33	FRB1 /INTR	I	Group Flash Ready_Busy 1, when select flash_rb1 mode, as Group Flash Ready_Busy1 signal input(detail in soft_flag [25]). 2, when select intr mode, as external interrupt input signal(detail in soft_flag [25]).
34	/SCK(I2c) FCEN3	O	1, When select test-mode, as scan-chain output 2, When select i2c , as sck 3, When select chip select2/3 mode, as CE3 output
35	FCEN2	I/O PU	1, When select test_mode, As scan-chain input 2, when select chip select2/3 mode, as CE2 output .(active when disable test_mode)

36	X_CLK_OUT /FCEN1	I/O PU	1, When select clock input mode (1), X_CLK_OFF=1, as external input test clock. 2, When select chip select1 mode or spi master mode, as output. (only active when X_CLK_OFF =0 or de-slect spi slve mode) (1), select chip select1 mode (detail in soft_flag [28]/[25]), as CE1 output (2), otherwise, as normal clock_out ,which defined at config_r[20].
37	FRB0	I	Group Flash Ready_Busy0
38	FDATA0_0 GPIO0	I/O PU	Group 0 Flash Data Bus - bit 0 General I/O port 0
39	FDATA0_1 GPIO1	I/O PU	Group 0 Flash Data Bus - bit 1 General I/O port 1
40	FDATA0_2 GPIO2	I/O PU	Group 0 Flash Data Bus - bit 2 General I/O port 2
41	FDATA0_3 GPIO3	I/O PU	Group 0 Flash Data Bus - bit 3 General I/O port 3
42	FDATA0_4 GPIO4	I/O PU	Group 0 Flash Data Bus - bit 4 General I/O port 4
43	FDATA0_5 GPIO5	I/O PU	Group 0 Flash Data Bus - bit 5 General I/O port 5
44	FDATA0_6 GPIO6	I/O PU	Group 0 Flash Data Bus - bit 6 General I/O port 6
45	FDATA0_7 GPIO7	I/O PU	Group 0 Flash Data Bus - bit 7 General I/O port 7
46	RST_OUT	O	Chip reset output/ External device reset signal Low active pulse output Should connect with RESET pad
47	RESET	I	Reset Sign (active low)
48	VSSA	GND	Analog 3.3V Ground

6 Electrical Characteristics

6.1 Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

symbol	parameter	conditions		min	max	unit
VDD33	analog supply voltage			-0.5	5.5	v
VDD18	digital supply voltage			-0.5	4.5	v
VDD50	input voltage			-0.5	5.5	v
Vesd	electrostatic discharge voltage[1]	ILI < 1 A	DP, DM and GND pins	-4000	+4000	v
			other pins	-2000	+2000	
Tstg	storage temperature			-40	+125	℃

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 k Ω resistor (Human Body Model).

6.2 Recommended operating conditions

symbol	Parameter	conditions	min	Typ	max	Unit
VDD33	analog supply voltage		3.0	3.3	3.6	V
VDD18	digital supply voltage		1.62	1.8	1.98	V
VDD50	input voltage		4.5	5	5.5	V
VI(AI/O)	input voltage on analog I/O pins DP DM	Low/Full speed	0	3.3	3.6	V
		High speed	0	400	-	mV
Tamb	ambient temperature		0	-	+70	℃

6.3 Static characteristics

All parameters are measured at VCCA = VCCD = 3.0 to 3.6 V; VAGND = VDGND = 0 V; Tamb = -40 to 85 °C;

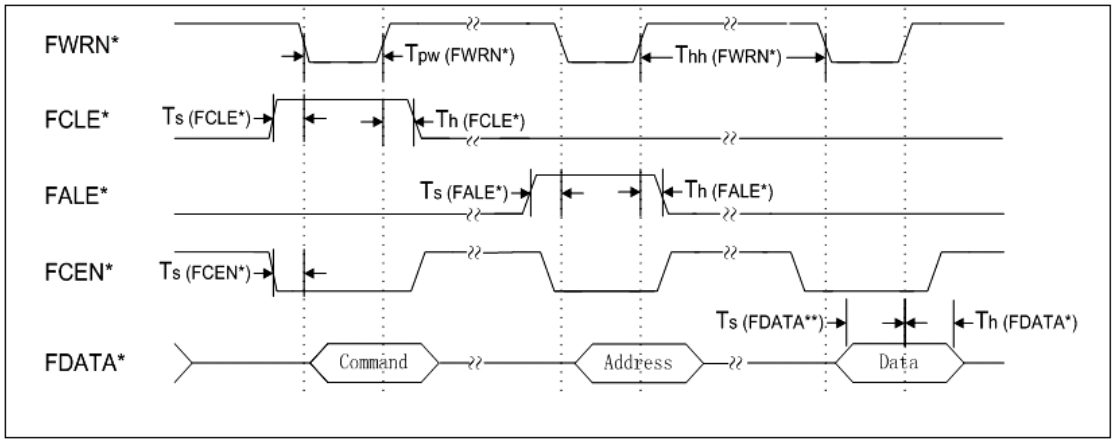
symbol	Parameter	Conditions	min	Type	max	Unit
ICC	operating supply current	Full-speed transmitting and receiving;	-	29.5	-	mA
		high-speed transmitting and receiving	-	50		
ICC(susp)	suspend supply current	in suspend mode	-	500		uA

6.4 Dynamic characteristics

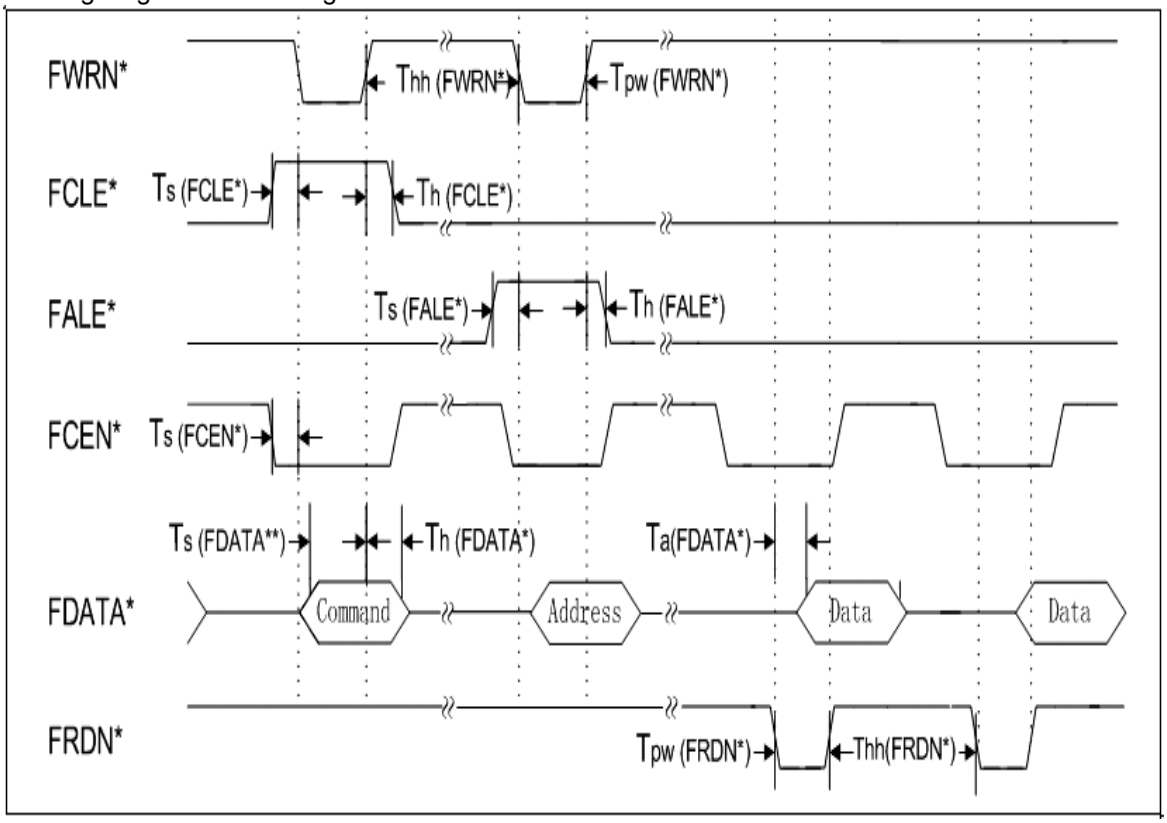
All parameters are measured at VCCA = VCCD = 3.0 to 3.6 V; VAGND = VDGND = 0 V;
Tamb = -40 to 85 ℃ ;

symbol	Parameter	conditions	min	Typ	max	Unit
Ts(FDATA*)	FDATA* setup time relative to rising FWRN* edge	Configured by firmware	8	33	75	ns
Th(FDATA*)	FDATA* hold time relative to falling FWRN* edge	Configured by firmware	8	33	75	ns
Ts (FCLE*)	FCLE* setup time relative to falling FWRN* edge	Configured by firmware	8	16	25	ns
Th (FCLE*)	FCLE* hold time relative to rising FWRN* edge	Configured by firmware	10	16	75	ns
Ts (FALE*)	FALE* setup time relative to falling FWRN* edge	Configured by firmware	8	16	25	ns
Th (FALE*)	FALE* hold time relative to rising FWRN* edge	Configured by firmware	10	16	75	ns
Ts (FCEN*)	FCEN* setup time relative to falling FWRN* edge	Configured by firmware	-	99		ns
Tpw (FWRN*)	FWRN* Pulse Width	Configured by firmware	8	33	75	ns
Thh (FWRN*)	FWRN* high hold time	Configured by firmware	8	33	75	ns
Ta(FDATA*)	FDATA* access time relative to falling FRDN* edge		-5	0	5	ns
Tpw (FRDN*)	FWRN* Pulse Width	Configured by firmware	8	33	75	ns
Thh (FRDN*)	FWRN* high hold time	Configured by firmware	8	33	75	ns

Timing diagram for Writing of Data



Timing diagram for Reading of Data



7 Mechanical Dimensions

7.1 48-Pin CBM2093 Package Outline Dimension

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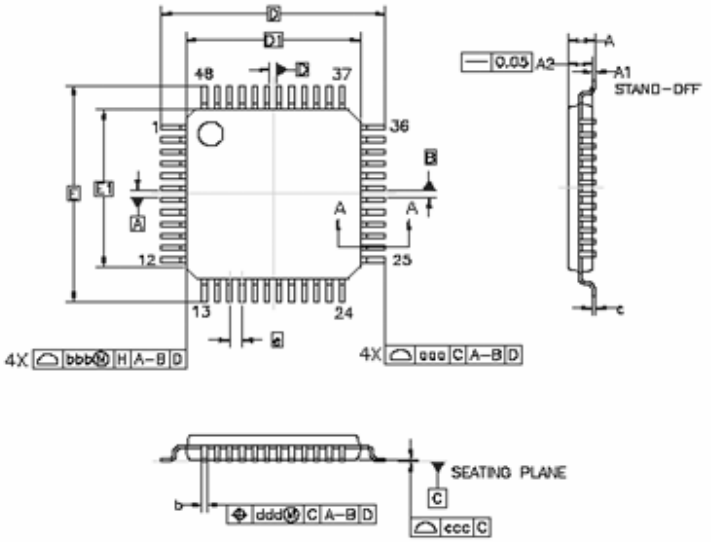
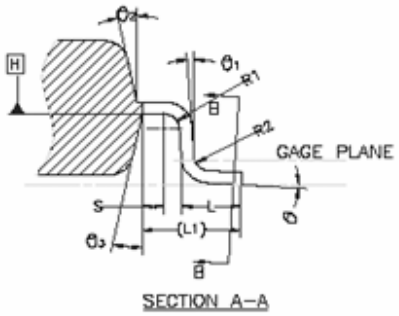
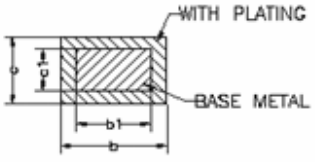




SECTION A-A



SECTION B-B

ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.006
L1	1.00 REF			0.039 REF		
L	0.45	0.60	0.75	0.018	0.024	0.030
S	0.20	—	—	0.008	—	—
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
e	0.50 BSC.			0.020 BSC.		
eee	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSION D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H;
3. DIMENSION b DOES NOT INUDE DAMBER PROTRUSION. ALLOWABLE DAMBER PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONTION. DAMBER CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT;
4. DIMENSION A INCLUDES STANDOFF HEIGHT A1,PACKAGE BODY THICKNESS AND UD HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES;
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TQFP 7.0 × 7.0 mm 48L Package Outline Dimension

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