

CBM2095

USB 2.0 Flash Disk Controller

Datasheet

Rev 2.0

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Contained herein

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Revision History

Date	Rev No	Description
2010-6-24	2.0	Initial release

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1 Description

Fastest & Securest USB 2.0 Flash Disk Controller with dedicated 32-bit microprocessor

The CBM2095 is the USB 2.0 Flash Disk controller with the fastest transfer speed on the market. CBM2095 can reach theoretical flash access speed limit of over 32MByte/s for read and 20MByte/s for write.

The on-the-fly ECC engine is capable of correcting up to 16/25/29/30bits per 1024 bytes page . For data security, CBM2095 is designed with both hardware and software data protection technology to prevent data corruption even if it is powered off or unplugged during data transfer.

The CBM2095 supports all 8 /16 bit BUS wide async NAND flash memory available in the market. New flash can be supported by software re-configuration.

The CBM2095 supports all 8 bit BUS wide ONFI/TOGGLE NAND flash memory available in the market. New flash can be supported by software re-configuration.

The CBM2095 has both a) 5V to 3.3V LDO and b) power on reset circuits integrated. Thus greatly reduced BOM cost and eased layout burden.

The CBM2095 can work properly with **no external crystal**. It was popularly used for UDP products.

The CBM2095 runs smoothly with all available hosts and PC platforms. Complied with USB specification rev. 2.0, the CBM2095 can be supported without additional driver under Win XP, Win 2000, Windows Me, Mac OS and Linux OS. With device driver installed, it can support Win 98/98SE as well. Comprehensive applications, such as PC boot up, disk partitions, password check for security disk, are available as part of our standard mass production software package.

The CBM2095 is available in 48-pin TQFP and 64-pin LQFP package, which are thinnest and smallest on the market. The 48-pin CBM2095 supports up to 4 flash chips and the 64-pin CBM2095 supports up to 8 flash chips. Customers can choose different packages to meet their design requirement.

2 Features

■ USB Interface

High-speed USB 2.0 interface;

■ Fastest data transfer rate on the market

Dual-channel mode: 32MB/s for Read, 20MB/s for Write

Single-channel mode: 26MB/s for Read, 20MB/s for Write

Fastest file copy rate on the market.

■ On-the-fly ECC built-in Hardware enhances reliability

ECC for NAND flash: 16/25/29/30 bit per page (1 page = 1024 bytes)

■ Special wear leveling algorithm to improve the flash life-time

■ Hardware & Software Data Protection Technology

Prevent data corruption even if it is powered off or unplugged during data transfer.

■ **SLC & MLC & TLC NAND Flash Interface**

Support 8k page flash parallel mode.
Support 8-bit and 16-bit Samsung SLC&MLC&TLC NAND flash.
Support 8-bit and 16-bit Toshiba SLC&MLC&TLC NAND flash.
Support 8-bit and 16-bit Hynix SLC&MLC&TLC NAND flash.
Support 8-bit and 16-bit Sandisk SLC&MLC&TLC NAND flash.
Support 8-bit and 16-bit Micron/Intel SLC&MLC&TLC NAND flash.
Support 8-bit and 16-bit ST/Numony SLC&MLC NAND flash.
Support 8-bit and 16-bit Infineon SLC&MLC NAND flash.
Support PowerChip SLC&MLC Nand flash
Support Spansion 3.3V MirrorBit-Quad flash
Support Actrans Nand Flash
Support ONFI2.0 DDR mode flash
Support Samsung Toggle mode flash
Software configuration to support various new flash memories
Supports up to 8 flash chips

■ **Proprietary 32-bit CISC microprocessor feature**

Proprietary 32-bit CISC processor for USB protocol processing and flash access.

Single cycle instruction period

■ **Integrated 5v to 3.3v voltage regulator**

■ **Disk partitions and password check for security disk available**

■ **PC boot up as USB Zip Disk, USB Hard Disk or USB CDROM**

■ **Auto run function**

■ **Low power dissipation**

Operating current 50mA (Bus power compatible)

■ **Build-in LDO**

Output maximum current up to 300mA

■ **Build-in crystal**

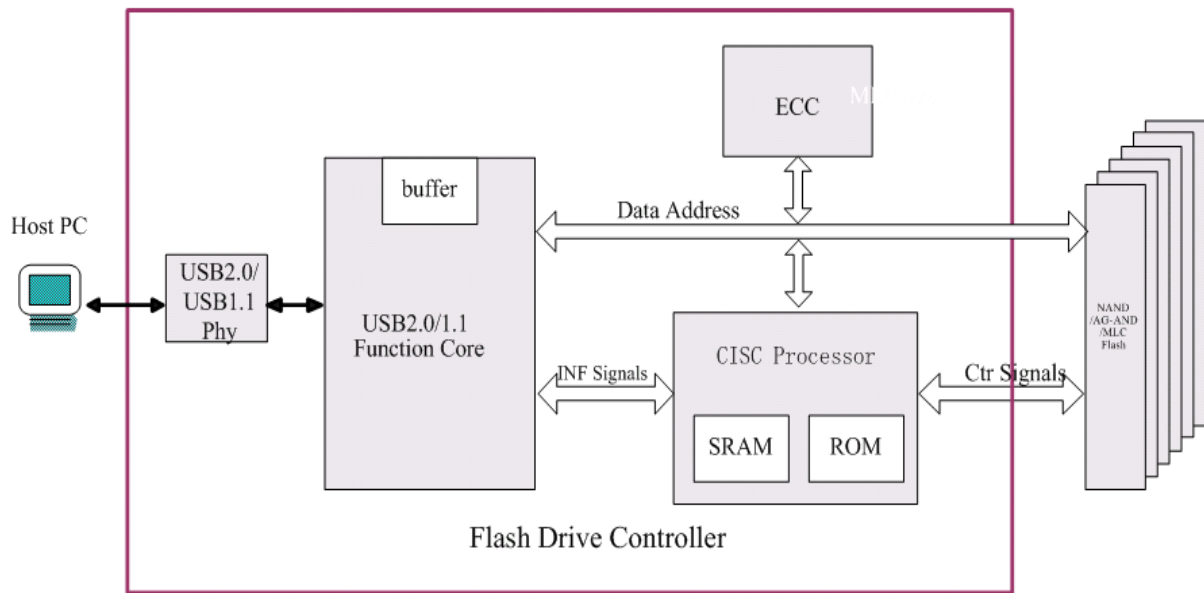
■ **Leading 0.16um CMOS technology**

■ **48-pin TQFP /64-pin LQFP package**

48-pin CBM2095 supports up to 4 Flash Chips

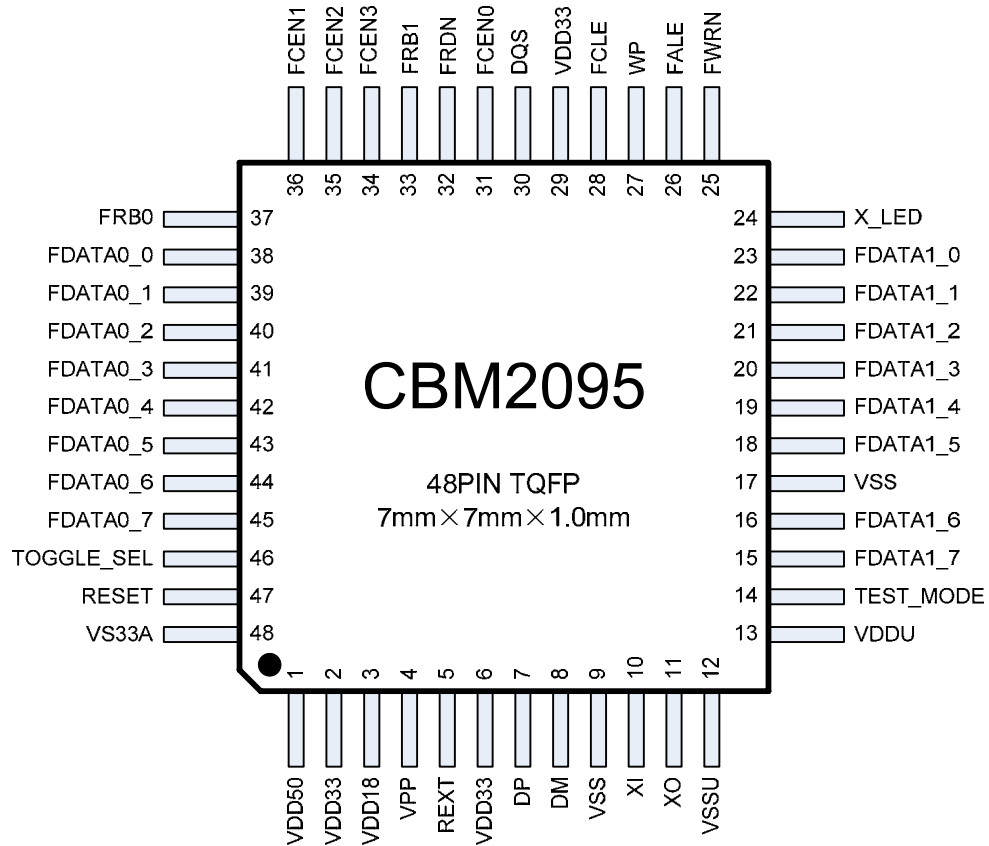
Windows, Mac and Linux compatible

3 Block Diagram



4 Pin Assignment

4.1 TQFP48 (Top Side)



5 Pin Description

Brief CBM2095 pin functions are shown in the following tables.

I:	Input signal
O:	Output signal
I/O:	Bi-direction signal
PWR:	Power signal
GND:	Ground signal
PU:	pull up
PD:	pull down

CBM2095 TQFP48 Pin Description

TQFP48 Pin No.	Pin Name	Type	Description
1	VDD50	PWR	Regulator 5V Power Input
2	VDD33	PWR	Regulator 3.3V Power OUT
3	VDD18	PWR	Regulator 1.8V Out
4	VPP	PWR	CORE 1.8V in
5	REXT	I	Connect External Resister for current reference
6	VDD33	PWR	Padring 3.3V Power
7	DP	I/O	USB Data D+
8	DM	I/O	USB Data D-
9	VSS	GND	Padring 3.3V / Logic 1.8V Ground
10	XI	I	Crystal Input (12 MHz)
11	XO	O	Crystal Output
12	VSSU	GND	Analog 1.8V Ground
13	VDDU	PWR	Analog 1.8V Power
14	TEST_MODE	I PD	Test Mode Enable Pin When high , test mode When low , normal mode
15	FDATA1_7 GPIO15	I/O PU	Group 1 Flash Data Bus - bit 7 General I/O port 15

			When select spi mode ,as spi chip select . (configure as GPIO and clear pin_64(detail in spi_ctl[13] .when select master mode , configure output , otherwise, configure as input.).
16	FDATA1_6 GPIO14	I/O PU	Group 1 Flash Data Bus - bit 6 General I/O port 14 When select spi mode, as clock out support ligh-tun sensor (configure as GPIO and clear pin_64(detail in spi_ctl[13] .when select ligh-tun mode , configure output).
17	VSS	GND	Padring 3.3V / Logic 1.8V Ground
18	FDATA1_5 GPIO13	I/O PU	Group 1 Flash Data Bus - bit 5 General I/O port 13
19	FDATA1_4 GPIO12	I/O PU	Group 1 Flash Data Bus - bit 4 General I/O port 12
20	FDATA1_3 GPIO11	I/O PU	Group 1 Flash Data Bus - bit 3 General I/O port 11
21	FDATA1_2 GPIO10	I/O PU	Group 1 Flash Data Bus - bit 2 General I/O port 10
22	FDATA1_1 GPIO9	I/O PU	Group 1 Flash Data Bus - bit 1 General I/O port 9
23	FDATA1_0 GPIO8	I/O PU	Group 1 Flash Data Bus - bit 0 General I/O port 8
24	X_LED	I/O	When TEST_MODE =1, as scan clock input. When TEST_MODE =0, as LED Indication
25	FWRN	O	Group Flash Write Enable (active low)
26	FALE	O	Group Flash Address Latch Enable
27	WP	I	Write Protect Switch Input
28	FCLE	O	Group Flash Command Latch Enable
29	VDD33	PWR	Padring 3.3V Power
30	DQS	I/O PD	DQS, only for onfi/toggle nand flash
31	FCEN0	O	Flash Chip Enable - Chip 0 (active low)
32	FRDN	O	Group Flash Read Enable (active low)
33	FRB1 /INTR	I	Group Flash Ready_Busy 1, when select flash_rb1 mode, as Group Flash Ready_Busy1 signal input(detail in soft_flag [25]). 2, when select intr mode, as external interrupt input signal(detail in soft_flag [25]).
34	/SCK(I2c) FCEN3	O	1, When select test-mode, as scan-chain output 2, When select i2c , as sck 3, When select chip select2/3 mode, as CE3 output
35	FCEN2	I/O PU	1, When select test_mode, As scan-chain input 2, when select chip select2/3 mode, as CE2 output .(active when disable test_mode)

36	X_CLK_OUT /FCEN1	I/O PU	1, When select clock input mode (1), X_CLK_OFF=1, as external input test clock. 2, When select chip select1 mode or spi master mode, as output. (only active when X_CLK_OFF =0 or de-select spi slave mode) (1), select chip select1 mode (detail in soft_flag [28]/[25]), as CE1 output (2), otherwise, as normal clock_out ,which defined at config_r[20].
37	FRB0	I	Group Flash Ready_Busy0
38	FDATA0_0 GPIO0	I/O PU	Group 0 Flash Data Bus - bit 0 General I/O port 0
39	FDATA0_1 GPIO1	I/O PU	Group 0 Flash Data Bus - bit 1 General I/O port 1
40	FDATA0_2 GPIO2	I/O PU	Group 0 Flash Data Bus - bit 2 General I/O port 2
41	FDATA0_3 GPIO3	I/O PU	Group 0 Flash Data Bus - bit 3 General I/O port 3
42	FDATA0_4 GPIO4	I/O PU	Group 0 Flash Data Bus - bit 4 General I/O port 4
43	FDATA0_5 GPIO5	I/O PU	Group 0 Flash Data Bus - bit 5 General I/O port 5
44	FDATA0_6 GPIO6	I/O PU	Group 0 Flash Data Bus - bit 6 General I/O port 6
45	FDATA0_7 GPIO7	I/O PU	Group 0 Flash Data Bus - bit 7 General I/O port 7
46	TOGGLE_SEL	I PU	Toggle nand flash select (active low)
47	RESET	I	Reset Sign (active low)
48	VSS33A	GND	Analog 3.3V Ground

6 Electrical Characteristics

6.1 Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

symbol	parameter	conditions		min	max	unit
VDD33	analog supply voltage			-0.5	5.5	v
VDD18	digital supply voltage			-0.5	4.5	v
VDD50	input voltage			-0.5	5.5	v
Vesd	electrostatic discharge voltage[1]	ILI < 1 A	DP, DM and GND pins	-4000	+4000	v
			other pins	-2000	+2000	
Tstg	storage temperature			-40	+125	

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 k resistor (Human Body Model).

6.2 Recommended operating conditions

symbol	Parameter	conditions	min	Typ	max	Unit
VDD33	analog supply voltage		3.0	3.3	3.6	V
VDD18	digital supply voltage		1.62	1.8	1.98	V
VDD50	input voltage		4.5	5	5.5	V
VI(AI/O)	input voltage on analog I/O pins DP DM	Low/Full speed	0	3.3	3.6	V
		High speed	0	400	-	mV
Tamb	ambient temperature		0	-	+70	

6.3 Static characteristics

All parameters are measured at $V_{CCA} = V_{CCD} = 3.0$ to 3.6 V; $V_{AGND} = V_{DGND} = 0$ V;
 $T_{amb} = 40$ to 85 ;

symbol	Parameter	Conditions	min	Typ	max	Unit
ICC	operating supply current	Full-speed transmitting and receiving;	-	29.5	-	mA
		high-speed transmitting and receiving	-	50		
ICC(susp)	suspend supply current	in suspend mode	-	500		uA

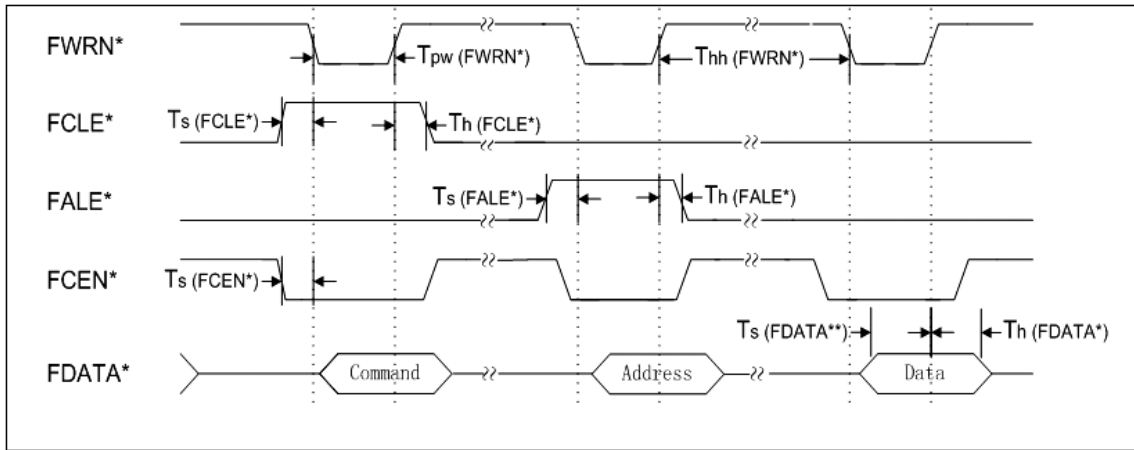
6.4 Dynamic characteristics

6.4.1 Normal NAND FLASH Dynamic characteristics

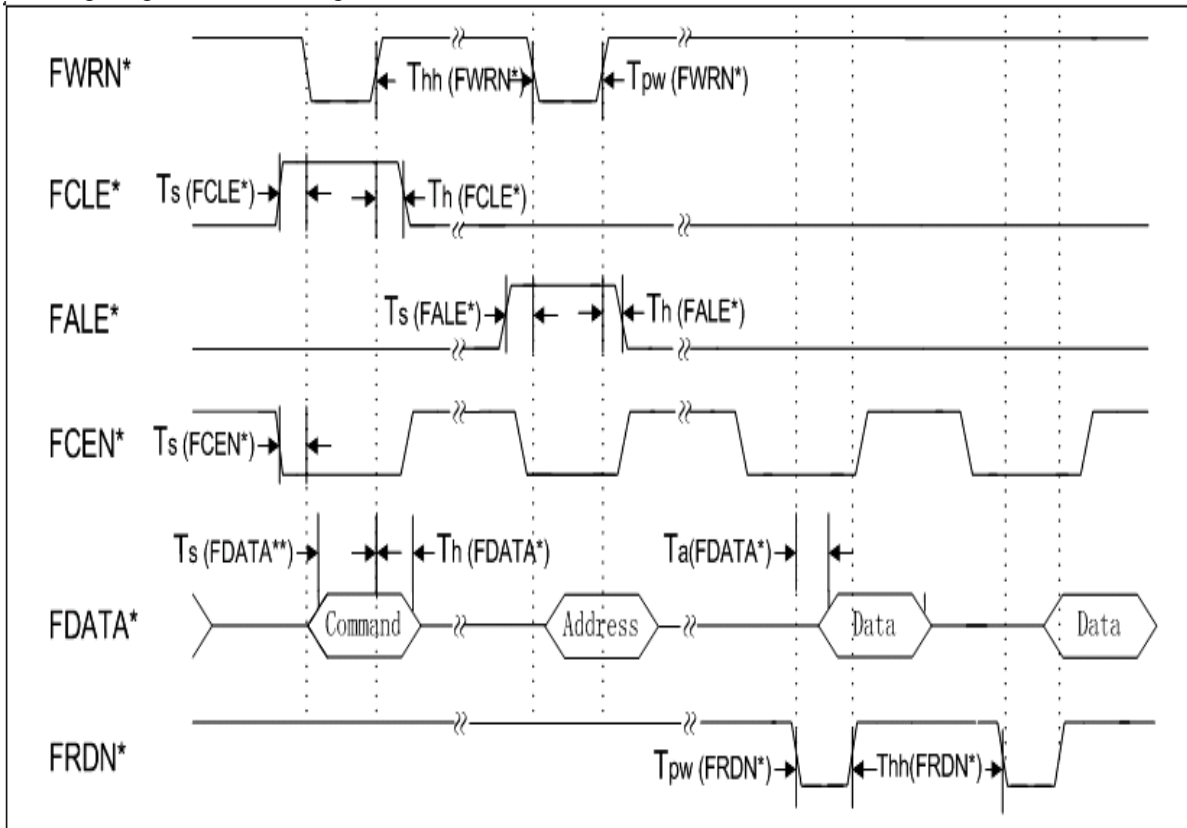
All parameters are measured at $V_{CCA} = V_{CCD} = 3.0$ to 3.6 V; $V_{AGND} = V_{DGND} = 0$ V;
 $T_{amb} = -40$ to 85 ;

symbol	Parameter	conditions	min	Typ	max	Unit
$T_s(\text{FDATA}^*)$	FDATA* setup time relative to rising FWRN* edge	Configured by firmware	8	33	75	ns
$T_h(\text{FDATA}^*)$	FDATA* hold time relative to falling FWRN* edge	Configured by firmware	8	33	75	ns
$T_s(\text{FCLE}^*)$	FCLE* setup time relative to falling FWRN* edge	Configured by firmware	8	16	25	ns
$T_h(\text{FCLE}^*)$	FCLE* hold time relative to rising FWRN* edge	Configured by firmware	10	16	75	ns
$T_s(\text{FALE}^*)$	FALE* setup time relative to falling FWRN* edge	Configured by firmware	8	16	25	ns
$T_h(\text{FALE}^*)$	FALE* hold time relative to rising FWRN* edge	Configured by firmware	10	16	75	ns
$T_s(\text{FCEN}^*)$	FCEN* setup time relative to falling FWRN* edge	Configured by firmware	-	99		ns
$T_{pw}(\text{FWRN}^*)$	FWRN* Pulse Width	Configured by firmware	8	33	75	ns
$T_{hh}(\text{FWRN}^*)$	FWRN* high hold time	Configured by firmware	8	33	75	ns
$T_a(\text{FDATA}^*)$	FDATA* access time relative to falling FRDN* edge		-5	0	5	ns
$T_{pw}(\text{FRDN}^*)$	FWRN* Pulse Width	Configured by firmware	8	33	75	ns
$T_{hh}(\text{FRDN}^*)$	FWRN* high hold time	Configured by firmware	8	33	75	ns

Timing diagram for Writing of Data



Timing diagram for Reading of Data



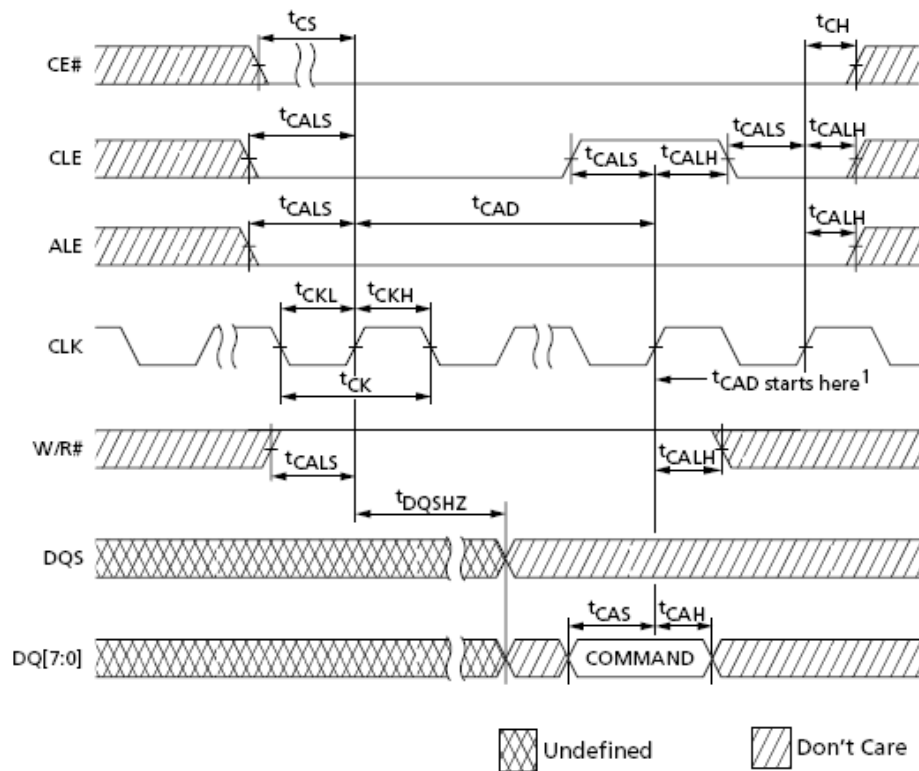
6.4.2 ONFI NAND FLASH Dynamic characteristics

CBM2095 only support Mode0/Mode1/Mode2.

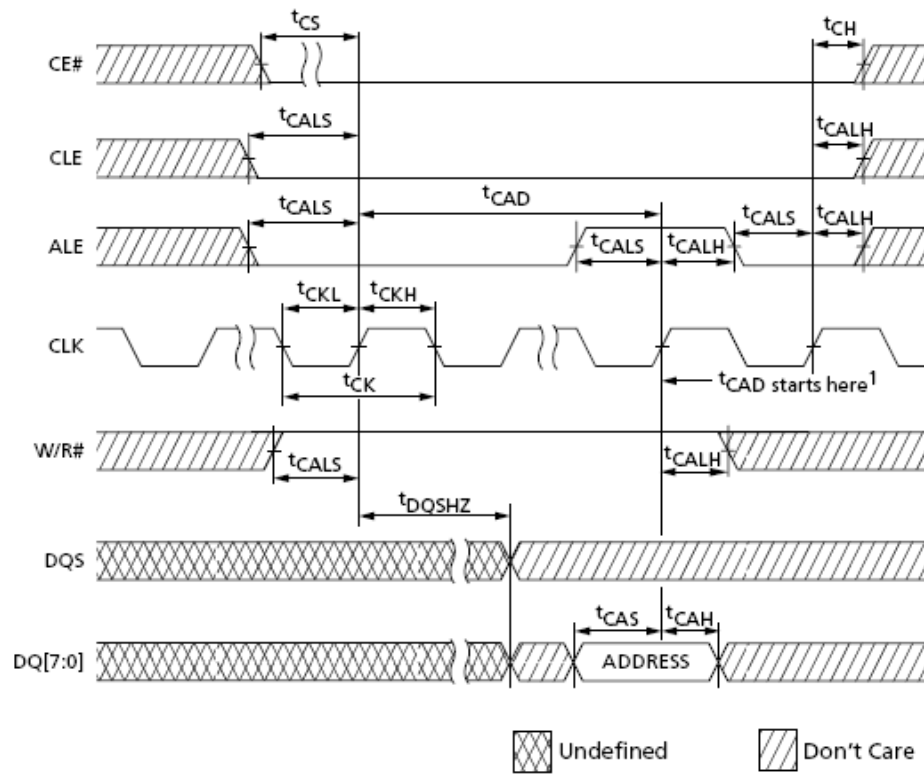
Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock Period		50		30		20		15		12		ns	-
Frequency		≈20		≈33		≈50		≈67		≈83		MHZ	-
Access window of DQ[7:0] from CLK	t_{AC}	-	20	-	20	-	20	-	20	-	20	ns	-
ALE to data loading time	t_{ADL}	100	-	100	-	70	-	70	-	70	-	ns	-
Cmd, Addr, Data delay	t_{CAD}	25	-	25	-	25	-	25	-	25	-	ns	1
ALE, CLE, W/R# hold	t_{CALH}	10	-	5	-	4	-	3	-	2.5	-	ns	-
ALE, CLE, W/R# setup	t_{CALS}	10	-	5	-	4	-	3	-	2.5	-	ns	-
DQ hold - Cmd, Addr	t_{CAH}	10	-	5	-	4	-	3	-	2.5	-	ns	-
DQ setup - Cmd, Addr	t_{CAS}	10	-	5	-	4	-	3	-	2.5	-	ns	-
Change column setup to data in/out or next command	t_{CCS}	200	-	200	-	200	-	200	-	200	-	ns	2
CE# hold	t_{CH}	10	-	5	-	4	-	3	-	2.5	2	ns	-
Average CLK cycle time	$t_{CK (avg)}$	50	100	30	50	20	30	15	20	12	15	ns	3
Absolute CLK cycle time, from rising edge to rising edge	$t_{CK (abs)}$	$t_{CK(abs) MIN} = t_{CK(avg)} + t_{JIT(per) MIN}$ $t_{CK(abs) MAX} = t_{CK(avg)} + t_{JIT(per) MAX}$										ns	-
CLK cycle HIGH	$t_{CKH (abs)}$	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	t_{CK}	4
CLK cycle LOW	$t_{CKL (abs)}$	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	0.43	0.57	t_{CK}	4
Data output end to W/R# HIGH	t_{CKWR}	$t_{CKWR(MIN)} = RoundUp[(t_{DQSCK(MAX)} + t_{CK}) / t_{CK}]$										t_{CK}	-
CE# setup	t_{CS}	35	-	25	-	15	-	15	-	15	-	ns	-
Data In hold	t_{DH}	5	-	2.5	-	1.7	-	1.3	-	1.1	-	ns	-
Access window of DQS from CLK	t_{DQSCK}	-	20	-	20	-	20	-	20	-	20	ns	-
DQS, DQ[7:0] Driven by NAND	t_{DQSD}	0	20	0	20	0	20	0	20	0	20	ns	-
DQS, DQ[7:0] to tri-state	t_{DQSHZ}	-	20	-	20	-	20	-	20	-	20	ns	5
DQS input high pulse width	t_{DQSH}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	-
DQS input low pulse width	t_{DQSL}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}	-
DQS-DQ skew	t_{DQSQ}	-	5	-	2.5	-	1.7	-	1.3	-	1.1	ns	-
Data input	t_{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	0.75	1.25	t_{CK}	-
Data In setup	t_{DS}	5	-	3	-	2	-	1.5	-	1.1	-	ns	-

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
DQS falling edge from CLK rising - hold	t_{DSH}	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	t_{CK}	-
DQS falling to CLK rising - setup	t_{DSS}	0.2	-	0.2	-	0.2	-	0.2	-	0.2	-	t_{CK}	-
Data Valid Window	t_{DVW}	$t_{DVW} = t_{OH} - t_{DQSQ}$										ns	-
Half Clock Period	t_{HP}	$t_{HP} = \text{Min}(t_{CKH}, t_{CKL})$										ns	-
The deviation of a given $t_{CK}(\text{abs})$ from $t_{CK}(\text{avg})$	$t_{JIT}(\text{per})$	-0.7	0.7	-0.7	0.7	-0.7	0.7	-0.6	0.6	-0.6	0.6	ns	-
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t_{QH}	$t_{QH} = t_{HP} - t_{QHS}$										ns	-
Data Hold Skew Factor	t_{QHS}	-	6	-	3	-	2	-	1.5	-	1.2	ns	-
Data output to command, address, or data input	t_{RHW}	100	-	100	-	100	-	100	-	100	-	ns	-
Ready to data output	t_{RR}	20	-	20	-	20	-	20	-	20	-	ns	-
Device reset time (Read/Program/Erase)	t_{RST}	-	5/10/500	-	5/10/500	-	5/10/500	-	5/10/500	-	5/10/500	μs	6
CLK high to R/B# low	t_{WB}	-	100	-	100	-	100	-	100	-	100	ns	-
Command cycle to data output	t_{WHR}	80	-	60	-	60	-	60	-	60	-	ns	-
DQS write preamble	t_{WPRE}	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	t_{CK}	-
DQS write postamble	t_{WPST}	1.5	-	1.5	-	1.5	-	1.5	-	1.5	-	t_{CK}	-
W/R# LOW to data output cycle	t_{WRCK}	20	-	20	-	20	-	20	-	20	-	ns	-
WP# transition to command cycle	t_{WW}	100	-	100	-	100	-	100	-	100	-	ns	-

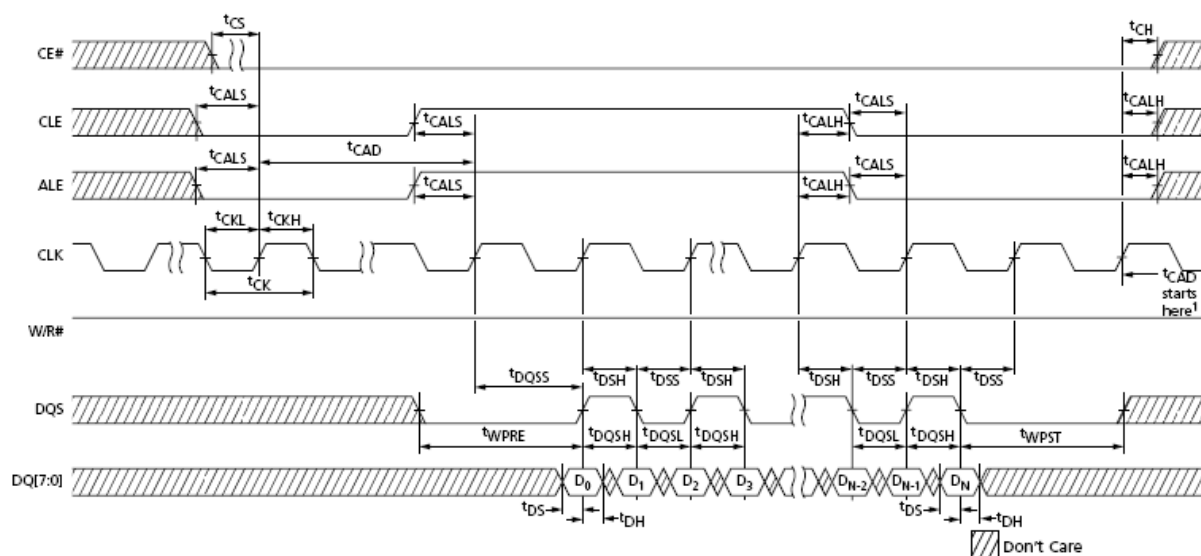
- Notes:
1. Delay is from start of command to next command, address, or data cycle; start of address to next command, address, or data cycle; and end of data to start of next command, address, or data cycle.
 2. This value is specified in the parameter page.
 3. $t_{CK}(\text{avg})$ is the average clock period over any consecutive 200-cycle window.
 4. $t_{CKH}(\text{abs})$ and $t_{CKL}(\text{abs})$ include static offset and duty cycle jitter.
 5. t_{DQSHZ} begins when W/R# is latched HIGH by CLK. This parameter is not referenced to a specific voltage level; it specifies when the device outputs are no longer driving.
 6. If RESET (FFh) is issued when the target is idle, the target goes busy for a maximum of 5 μs .



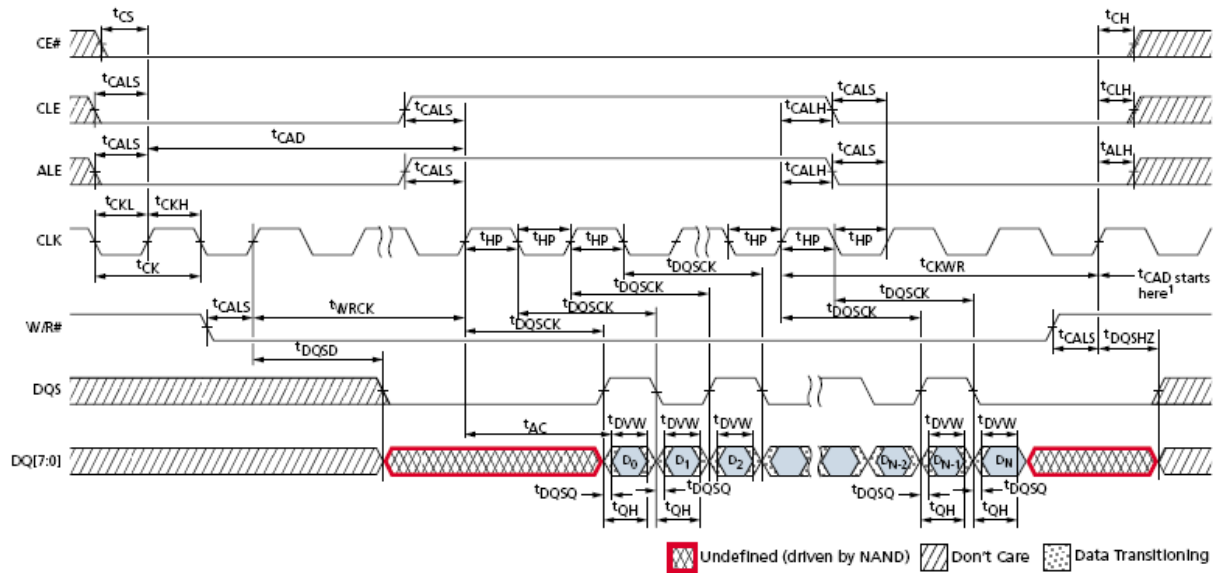
- Notes: 1. When CE# remains LOW, t_{CAD} begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).



Notes: 1. When CE# remains LOW, t_{CAD} begins at the rising edge of the clock from which the command cycle is latched for subsequent command, address, data input, or data output cycle(s).



- Notes:
1. When CE# remains LOW, t_{CAD} begins at the first rising edge of the clock after t_{WPST} completes.
 2. t_{DSH} (MIN) generally occurs during t_{DQSS} (MIN).
 3. t_{DSS} (MIN) generally occurs during t_{DQSS} (MAX).



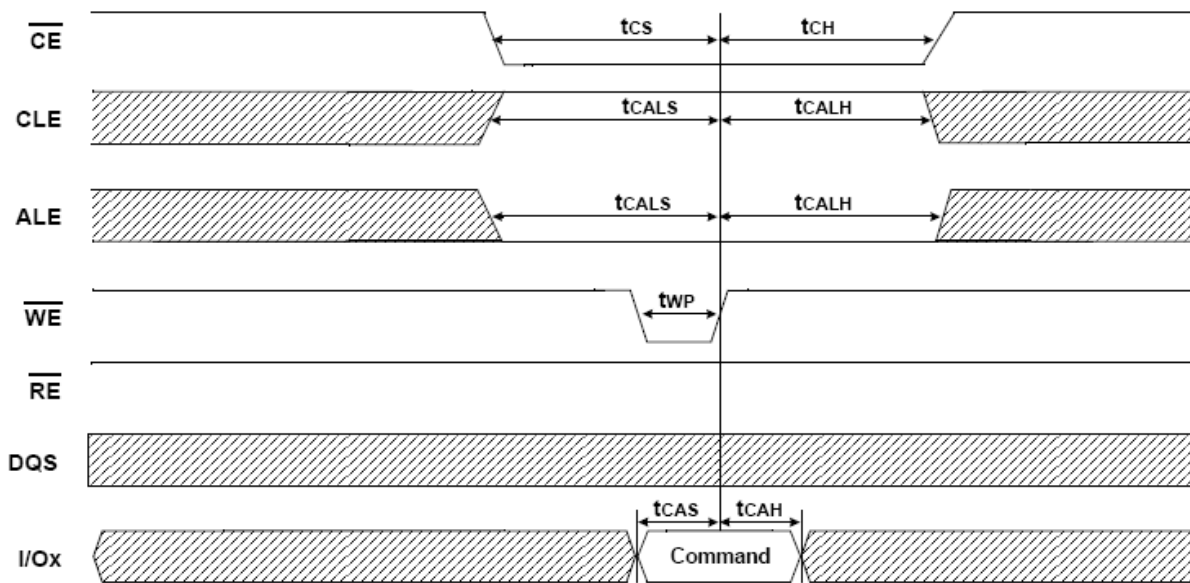
- Notes:
1. When CE# remains LOW, t_{CAD} begins at the rising edge of the clock after t_{CKWR} for subsequent command or data output cycle(s).
 2. See Figure 25 on page 33 for details of W/R# behavior.
 3. t_{AC} is the DQ output window relative to CLK and is the long-term component of DQ skew.
 4. For W/R# transitioning HIGH: DQ[7:0] and DQS go to tri-state.
 5. For W/R# transitioning LOW: DQ[7:0] drives current state and DQS goes LOW.
 6. After final data output, DQ[7:0] is driven until W/R# goes HIGH, but is not valid.

6.4.3 TOGGLE NAND FLASH Dynamic characteristics

CBM2095 only support 66Mbps/80Mbps.

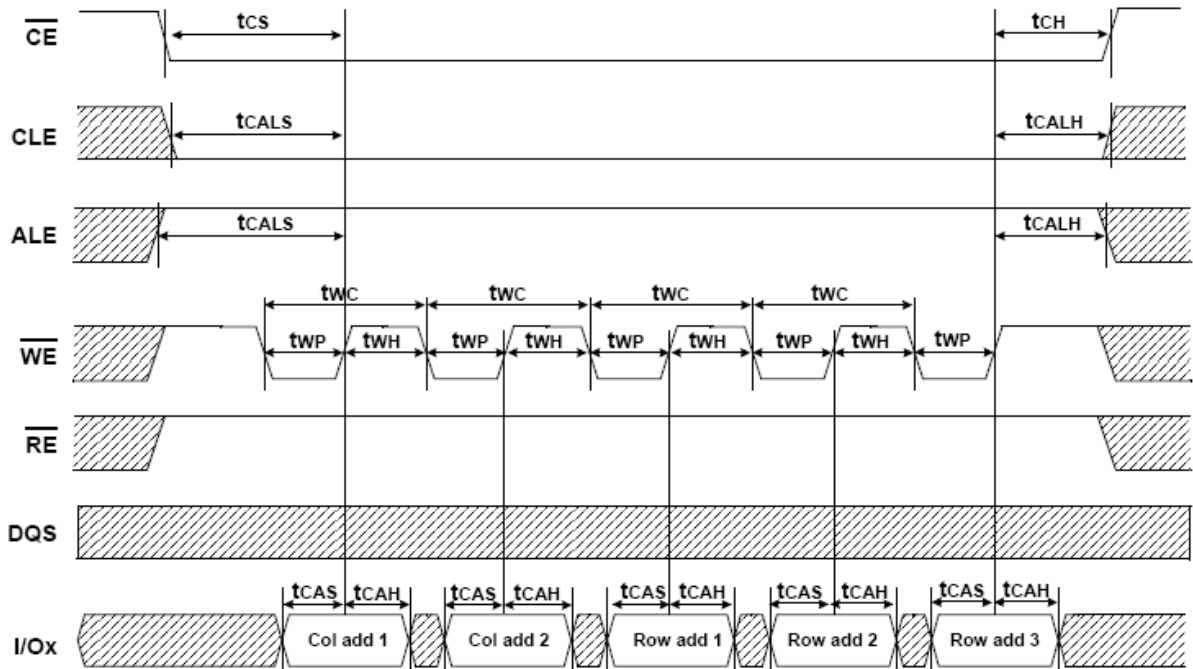
Parameter	Symbol	66Mbps		80Mbps		133Mbps		Unit
		Min	Max	Min	Max	Min	Max	
CLE/ALE Setup Time	tCALS	15	-	15	-	15	-	ns
CLE/ALE Hold Time	tCALH	5	-	5	-	5	-	ns
DQS Setup Time for data input start	tCDQSS	100	-	100	-	100	-	ns
DQS Hold Time for data input finish	tCDQSH	100	-	100	-	100	-	ns
Command Write cycle to Address Write cycle Time for Random data input	tCWAW	300	-	300	-	300	-	ns
\overline{CE} Setup Time	tCS	20	-	20	-	20	-	ns
\overline{CE} Hold Time	tCH	5	-	5	-	5	-	ns
Command/Address Setup Time	tCAS	5	-	5	-	5	-	ns
Command/Address Hold Time	tCAH	5	-	5	-	5	-	ns
Data Setup Time	tDS	4	-	3.3	-	2.0	-	ns
Data Hold Time	tDH	3.6	-	3	-	1.8	-	ns
Write Cycle Time	tWC	25	-	25	-	25	-	ns
\overline{WE} High pulse width	tWH	11	-	11	-	11	-	ns
\overline{WE} Low pulse Width	tWP	11	-	11	-	11	-	ns
Address to Data Loading Time	tADL	300	-	300	-	300	-	ns
Data Transfer from Cell to Register	tR	-	100	-	100	-	100	μ s
Ready to \overline{RE} High	tRR	20	-	20	-	20	-	ns
\overline{CE} Low to \overline{RE} Low	tCR	10	-	10	-	10	-	ns
ALE Low to \overline{RE} Low	tAR	10	-	10	-	10	-	ns
CLE to \overline{RE} Low	tCLR	10	-	10	-	10	-	ns
\overline{WE} High to Busy	tWB	-	100	-	100	-	100	ns
Read Cycle Time	tRC	30	-	25	-	15	-	ns
\overline{RE} High pulse width	tREH	13	-	11	-	6.5	-	ns
\overline{RE} Low pulse width	tRP	13	-	11	-	6.5	-	ns
\overline{CE} High to Output Hi-Z	tCHZ	-	30	-	30	-	30	ns
CLE High to Output Hi-Z	tCLHZ	-	30	-	30	-	30	ns
Data Strobe Cycle Time	tDSC	30	-	25	-	15	-	ns
DQS Input Low Pulse Width	tDQSL	13	-	11	-	6.5	-	ns
DQS Input High Pulse Width	tDQSH	13	-	11	-	6.5	-	ns
\overline{WE} High to \overline{RE} Low	tWHR	120	-	120	-	120	-	ns
\overline{WE} High to \overline{RE} Low for Random data out	tWHR2	300	-	300	-	300	-	ns

\overline{RE} to DQS and DQ delay	t_{DQSRE}	-	25	-	25	-	25	ns
Read Preamble	t_{RPRE}	15	-	15	-	15	-	ns
Read Postamble	t_{RPST}	$t_{DQSRE}+0.5t_{RC}$	-	$t_{DQSRE}+0.5t_{RC}$	-	$t_{DQSRE}+0.5t_{RC}$	-	ns
Read Postamble Hold Time	t_{RPSTH}	5	-	5	-	5	-	ns
Write Preamble	t_{WPRE}	15	-	15	-	15	-	ns
Write Postamble	t_{WPST}	6.5	-	6.5	-	6.5	-	ns
Write Postamble Hold Time	t_{WPSTH}	5	-	5	-	5	-	ns
Output skew among data output and corresponding DQS	t_{DQSQ}	-	2.5	-	2	-	1.4	ns
DQS hold skew factor	t_{QHS}	-	2.5	-	2	-	1.4	ns
Output hold time from DQS	t_{QH}	$t_{QH} = t_{REH}/RP - t_{QHS}$						ns
Output data valid window	t_{DVW}	$t_{DVW} = t_{QH} - t_{DQSQ}$						ns
Device Resetting Time (Read/Program/Erase)	$t_{RST}^{(1)}$	10/30/100						μs

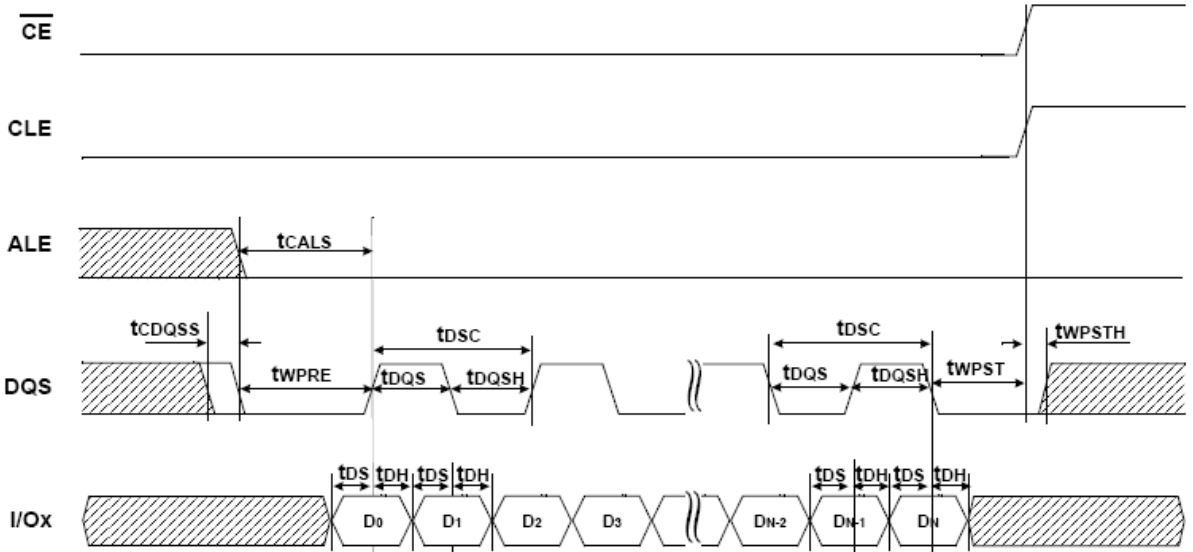


NOTE :

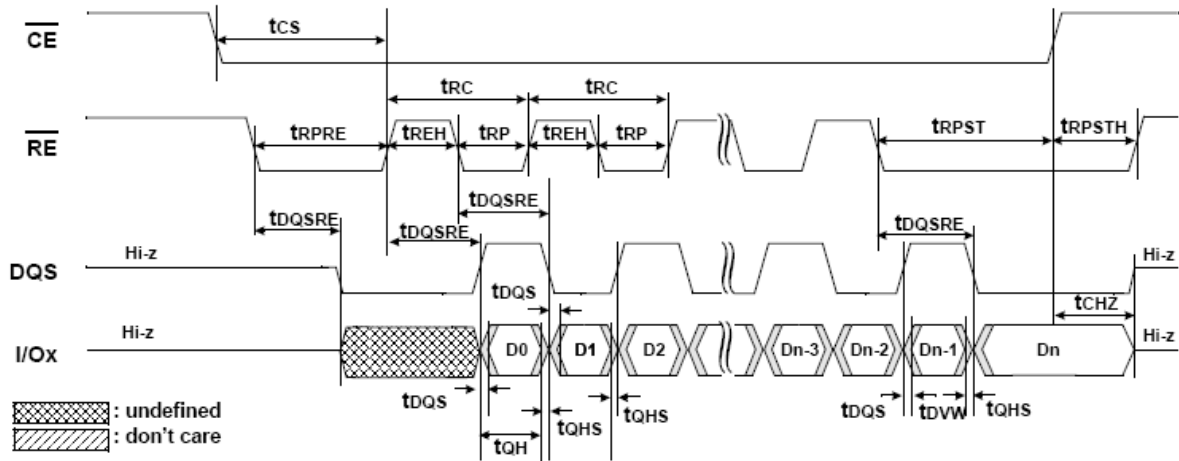
1. Command information is latched by \overline{WE} going high, when \overline{CE} is Low, CLE is High, and ALE is Low.
2. DQS should be set to 'Low' when these commands(85h, 10h, 11h) is input.



NOTE :
Row address consists of page address and block address.



- NOTE :
- 1) Data-input condition should be satisfied before DQS toggling for data input; data-input condition is that \overline{CE} & CLE & ALE are low and \overline{RE} & \overline{WE} are high
 - 2) DQS should be either high or low before data-input condition is set.
 - 3) Data-input condition should be kept during DQS toggling for data input including pre-amble and post-amble time.
 - 4) Because using toggle DDR interface, an even number of bytes should be always transferred when both data input and data output

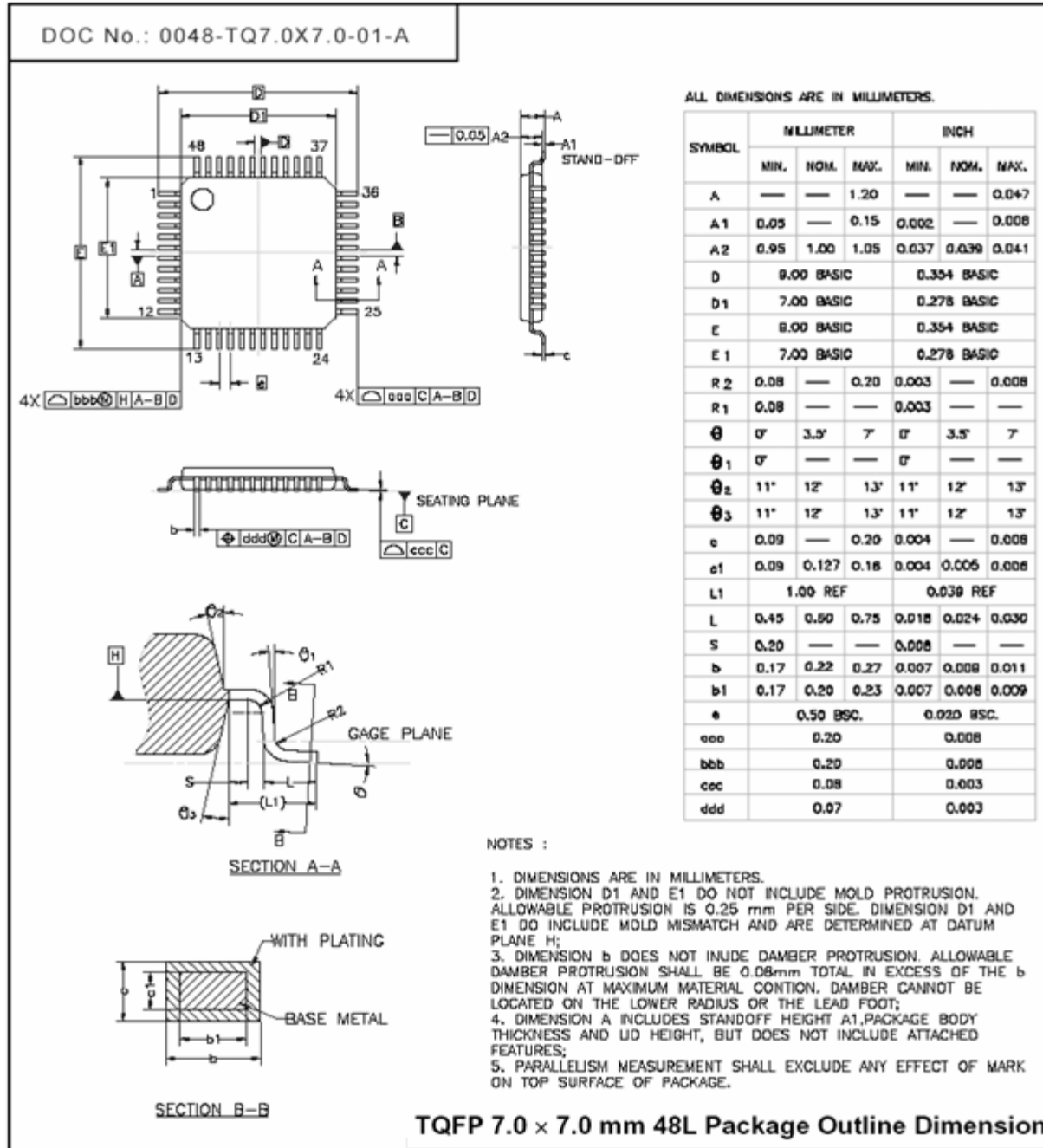


NOTE :

- 1) Data-output condition should be satisfied before \overline{RE} toggling for data output; data-output condition is that \overline{CE} & CLE & ALE are low and \overline{WE} is high
- 2) \overline{RE} should be either high or low before data-output condition is set.
- 3) Data-output condition should be kept during \overline{RE} toggling for data output including pre-able and post-able time.
- 4) DQS and Data out buffers are turned on when \overline{RE} is low for pre-able operation under data-out condition
- 5) DQS and Data out buffers turn from valid value to high-z if either \overline{CE} or CLE goes High.
- 6) an even number of bytes should be always transferred when both data input and data output

7 Mechanical Dimensions

7.1 48-Pin CBM2095 Package Outline Dimension



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