CBM3085C
Datasheet

Rev 1.0
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Revision History

Date	Rev No	Description
2010-03-23	1.0	Initial release

Contents

1 Description

Most flexible SD/MMC memory card Controller with dedicated 32-bit microprocessor

The CBM3085C is the most flexible SD/MMC memory card controller on the market. The proprietary 32 bit processor was specially tailored to handle both SD/MMC protocol and Flash access. Software change can be made easily on site to support new flash or solve potential compatibility issue.

CBM3085C support SD2.0 and MMC 4.2 standard. Which are backward compatible to the earlier SD/MMC version, such as SD1.0, SD1.01, SD1.1, and MMC 3.31, MMC4.0, MMC4.1 etc. Up to speed class 6 can be achieved with certain Flash type. CPRM is supported for SD card. It also supports sleep mode, which can cut down power consumption significantly.

CBM3085C can reach theoretical flash access speed up to 20MByte/s for read and 20MByte/s for write. The on-the-fly ECC engine is capable of correcting and detecting up to 8/12/15bit errors per 512bytes page. For data security, CBM3085C is designed with both hardware and software data protection technology to prevent data corruption even if it is powered off or unplugged during data transfer.

The CBM3085C supports all SLC/MLC/TLC flash memory available in the market. New flash can be supported by software re-configuration. Card with capacity up to 32GB can be made when configured as SDHC card. Card with capacity up to 128GB can be made when configured as MMCHC card.

The CBM3085C runs smoothly with various hosts. Substantial tests have been made to make sure the compatibility with different hosts.

2 Features

- **SD card standard**

  System specification SD2.0 compliance.
  eSD2.1 supported
  SPI mode supported
  Command class 0,2,4,5,6,7,8,10 supported
  CPRM supported
  Speed class up to 6
  Support host clock up to 50 MHz
  Supported bus width: X1, X4
  Supported sleep mode

- **MMC card standard**

  System specification MMC4.2 compliance.
  eMMC4.3 supported
  SPI mode supported
  Command class 0 to 8 supported
  Support host clock up to 52 MHz
  Supported bus width: X1, X4
  Supported sleep mode

- **Fastest data transfer rate on the market** :
  Up to 20MB/s Read/ Write speed for SD card

- **Hardware & Software Data Protection Technology**

  Prevent data corruption even if it is powered off or unplugged during data transfer.

- **Support TLC Flash By Hardware**
  Supports 8/15 bit ECC per 512 bytes flash
  Supports 24/30 bit ECC per 1K bytes flash
  Supports 512/2K/4K/8K bytes page flash

- **Nand Flash Interface**

  Supports Samsung flash memories
  Supports Toshiba & Sandisk flash memories
  Supports Infineon / Hynix flash memories
  Supports ST Microelectronics flash memories
  Supports Intel / Micron flash memories
  Software configuration to support various new flash memories
  Supports up to 4 flash chips.

- **Proprietary 32-bit CISC microprocessor feature**

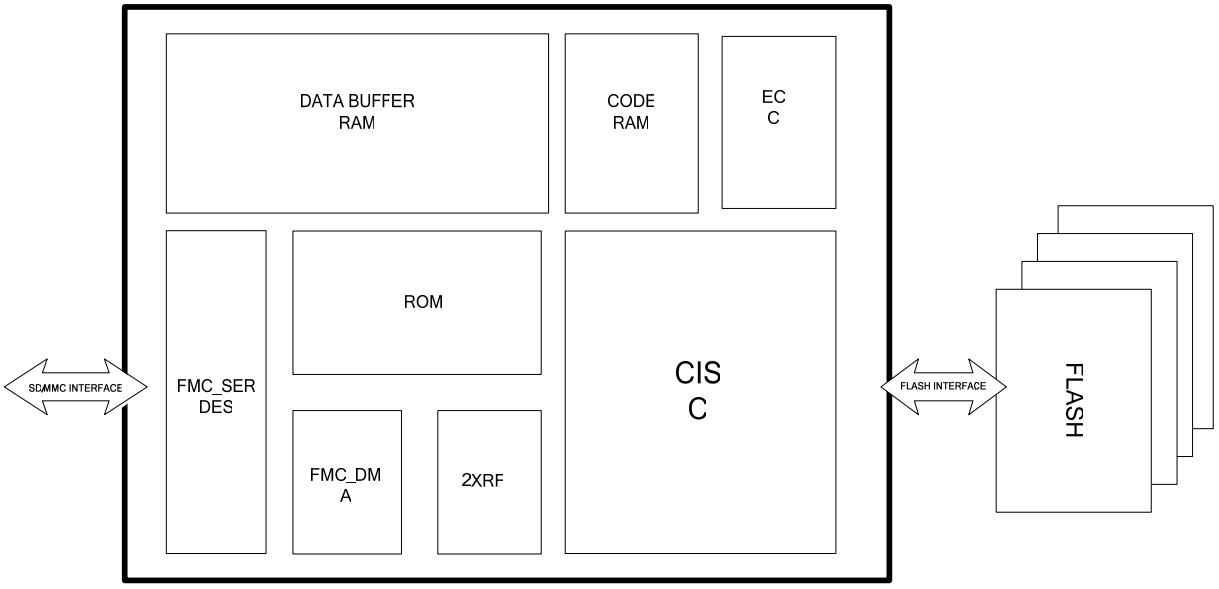
  Proprietary 32-bit CISC processor for SD/MMC protocol processing and flash access.

  Single cycle instruction period

- **Low power dissipation**

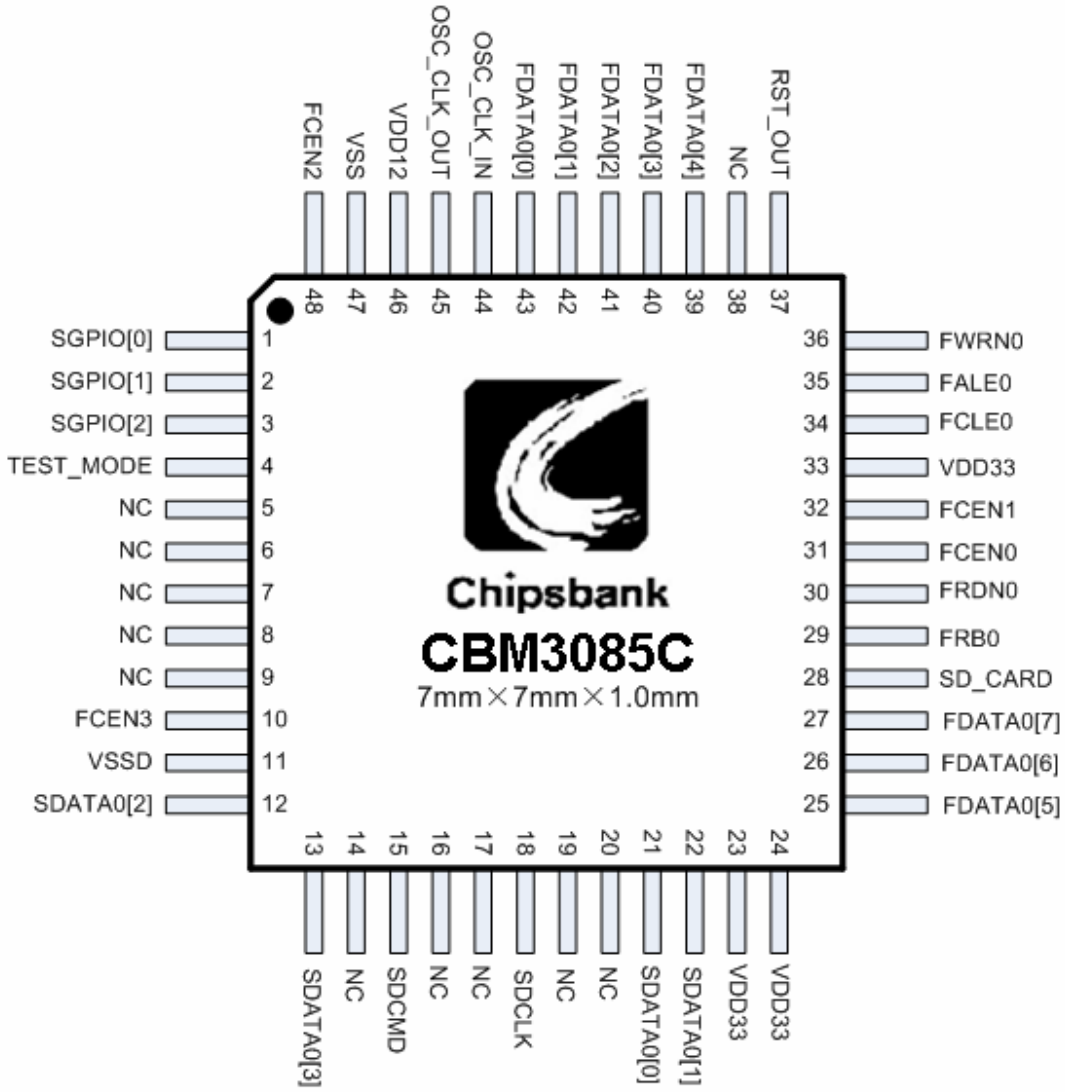
  Operating current 10 mA, suspend current less than 1 mA

3 Block Diagram



4 Pin Assignment

4.1 TSOP48 （Top View）



4.2 PIN Description

Brief CBM3085C pin functions are shown in the following tables.

I ： Input signal

O ： Output signal

I/O ： Bi-direction signal

PWR : Power signal

GND： Ground signal

NC: Not connect

PIN Description

PIN num	Pad Name	Type	Description
1	SGPIO0[0]	I/O	GPIO0
2	SGPIO0[1]	I/O	GPIO0
3	SGPIO0[2]	I/O	GPIO0
4	TEST_MODE	I	Test Mode Enable Pin
5	NC		
6	NC		
7	NC		
8	NC		
9	NC		
10	FCEN3	O	Flash Chip Enable - Chip 3 (active low)
11	VSSD	GND	Ground for pad
12	SDATA0[2]	I/O	SD/MMC data bus bit2
13	SDATA0[3]	I/O	SD/MMC data bus bit3
14	NC		
15	SDCMD	I/O	SD/MMC command line
16	NC		
17	NC		
18	SDCLK	I	SD/MMC clock input
19	NC		

20	NC		
21	SDATA0[0]	I/O	SD/MMC data bus bit0
22	SDATA0[1]	I/O	SD/MMC data bus bit1
23	VDD33	PWR	Regulator 3.3V input
24	VDD33	PWR	Regulator 3.3V input
25	FDATA0[5]	I/O	Flash Data Bus - bit 5
26	FDATA0[6]	I/O	Flash Data Bus - bit 6
27	FDATA0[7]	I/O	Flash Data Bus - bit 7
28	SD_CARD	I	When low as MMC mode; when high as SD card
29	FRB0	I	Group Flash Ready_Busy0
30	FRDN0	O	Group Flash Read Enable (active low)
31	FCEN0	O	Flash Chip Enable - Chip 0 (active low)
32	FCEN1	O	Flash Chip Enable - Chip 1 (active low)
33	VDD33	PWR	3.3V power input for pad
34	FCLE0	O	Group Flash Command Latch Enable
35	FALE0	O	Group Flash Address Latch Enable
36	FWRN0	O	Group Flash Write Enable (active low)
37	RST_OUT	O	Chip reset output/ External device reset signal
38	NC		
39	FDATA0[4]	I/O	Flash Data Bus - bit 4
40	FDATA0[3]	I/O	Flash Data Bus - bit 3
41	FDATA0[2]	I/O	Flash Data Bus - bit 2
42	FDATA0[1]	I/O	Flash Data Bus - bit 1
43	FDATA0[0]	I/O	Flash Data Bus - bit 0
44	OSC_CLK_IN	I	External clock for debug
45	OSC_CLK_OUT	O	Oscillator clock output when under test mode(normal mode, keep high)
46	VDD12	PWR	Regulator 1.2V output
47	VSS	GND	Regulator Ground
48	FCEN2	O	Flash Chip Enable - Chip 2 (active low)

NOTES: All the IO type according to the normal working only (when TEST_MODE = 0).

5 Electrical Characteristics

5.1 Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134).

symbol	parameter	conditions		min	max	unit
VDD33	supply voltage			3.0	3.6	V
VI	input voltage			3.0	3.6	V
Vesd	electrostatic discharge voltage[1]	ILI < 1 A	SD/MMC pins	-4000	+4000	V
			other pins	-2000	+2000	
Tstg	storage temperature			-40	+125	℃

[1] Equivalent to discharging a 100 pF capacitor via a 1.5 k . resistor (Human Body Model).

5.2 Recommended operating conditions

symbol	Parameter	conditions	min	Typ	max	Unit
VDD33	digital supply voltage		3.0	3.3	3.6	V
VI	input voltage		0	-	VDD33	V
Tamb	ambient temperature		0	-	+70	℃

5.3 Static characteristics

All parameters are measured at V33_IN = 3.0 to 3.6 V; VSS = 0 V; Tamb = 40 to 85 ℃;

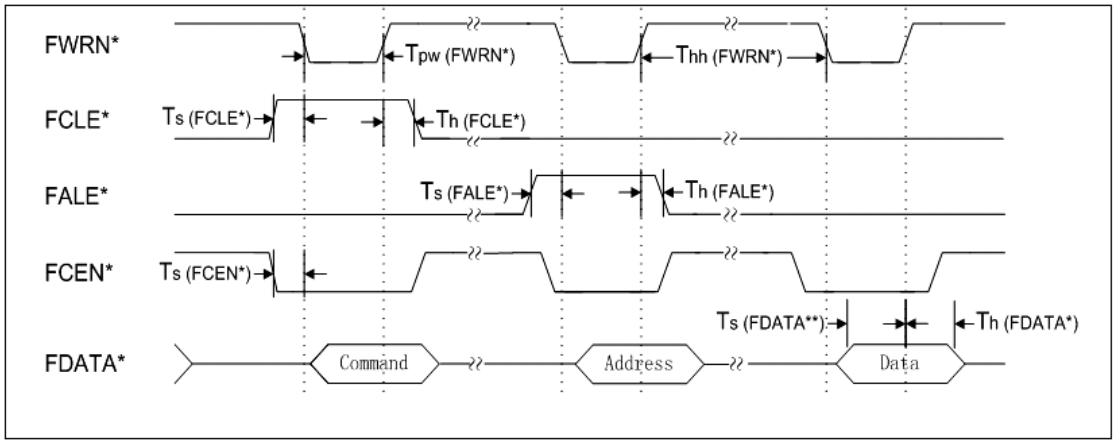
symbol	Parameter	Conditions	min	Typ	max	Unit
ICC	operating supply current	In operational mode		10		mA
ICC(susp)	suspend supply current	in suspend mode	-	1		mA

5.4 Dynamic characteristics

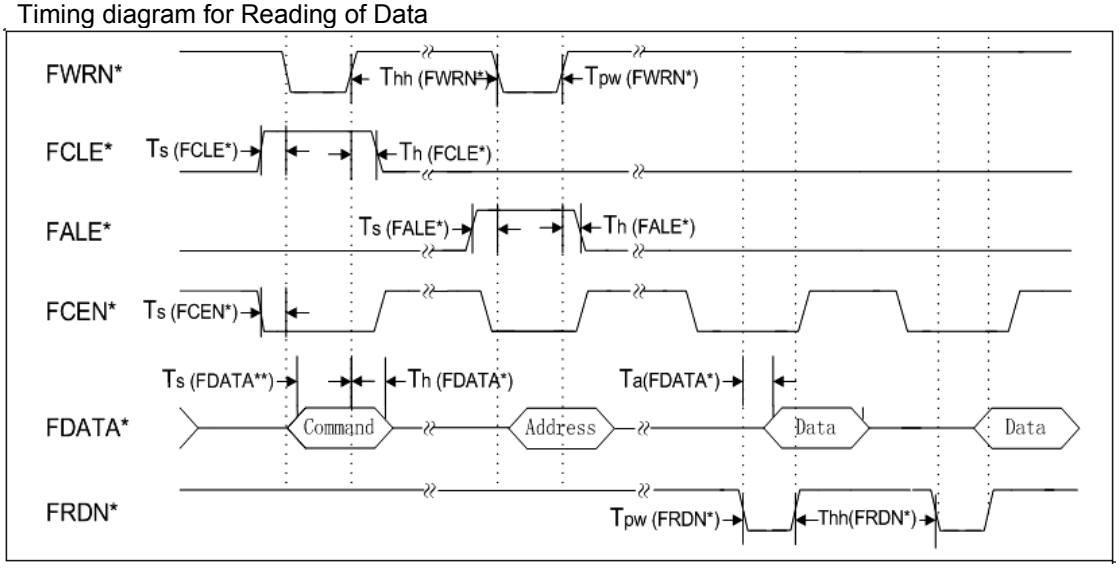
All parameters are measured at V33_IN = 3.0 to 3.6 V; VSS = 0 V; Tamb = -40 to 85 ℃;

symbol	Parameter	conditions	min	Typ	max	Unit
Ts(FDATA*)	FDATA* setup time relative to rising FWRN* edge		-	33	-	ns
Th(FDATA*)	FDATA* hold time relative to falling FWRN* edge		-	33	-	ns
Ts (FCLE*)	FCLE* setup time relative to falling FWRN* edge		-	33	-	ns
Th (FCLE*)	FCLE* hold time relative to rising FWRN* edge		-	33	-	ns
Ts (FALE*)	FALE* setup time relative to falling FWRN* edge		-	33	-	ns
Th (FALE*)	FALE* hold time relative to rising FWRN* edge		-	33	-	ns
Ts (FCEN*)	FCEN* setup time relative to falling FWRN* edge		-	99	-	ns
Tpw (FWRN*)	FWRN* Pulse Width		-	33	-	ns
Thh (FWRN*)	FWRN* high hold time		-	33	-	ns
Ta(FDATA*)	FDATA* access time relative to falling FRDN* edge		-	-	40	ns
Tpw (FRDN*)	FWRN* Pulse Width		-	33	-	ns
Thh (FRDN*)	FWRN* high hold time		-	33	-	ns

Timing diagram for Writing of Data



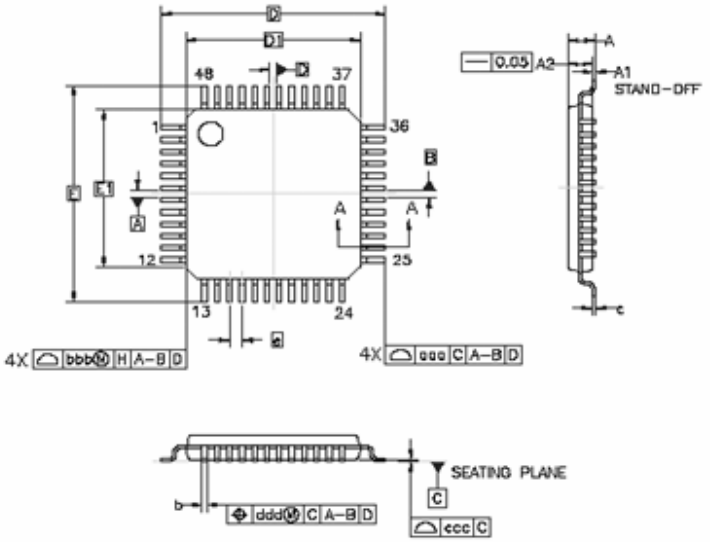
Timing diagram for Reading of Data

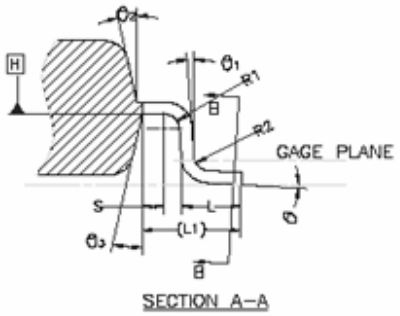


6 Mechanical Dimensions

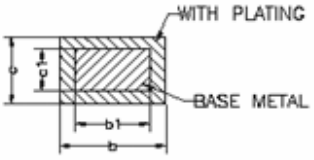
6.1 48-Pin CBM3085C TQFP Package Outline Dimension

DOC No.: 0048-TQ7.0X7.0-01-A





SECTION A–A



SECTION B–B

ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
D	9.00 BASIC			0.354 BASIC		
D1	7.00 BASIC			0.276 BASIC		
E	9.00 BASIC			0.354 BASIC		
E1	7.00 BASIC			0.276 BASIC		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	0.127	0.16	0.004	0.005	0.006
L1	1.00 REF			0.039 REF		
L	0.45	0.60	0.75	0.018	0.024	0.030
S	0.20	—	—	0.008	—	—
b	0.17	0.22	0.27	0.007	0.009	0.011
b1	0.17	0.20	0.23	0.007	0.008	0.009
e	0.50 BSC.			0.020 BSC.		
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

NOTES :

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSION D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H;
3. DIMENSION b DOES NOT INUDE DAMBER PROTRUSION. ALLOWABLE DAMBER PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONTION. DAMBER CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT;
4. DIMENSION A INCLUDES STANDOFF HEIGHT A1,PACKAGE BODY THICKNESS AND UD HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES;
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

TQFP 7.0 × 7.0 mm 48L Package Outline Dimension

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