CBM4081
USB 2.0 Memory Card Reader
Datasheet

Contents

1 Description

High speed USB 2.0 memory card reader Controller with dedicated 32-bit microprocessor, the cost down version for CBM4080.

CBM4081 is the cost down version for CBM4080. It is the fastest USB 2.0 memory card reader with embedded 32-bit microprocessor. It can attain 30MByte/s for read and 20MByte/s for write.

CBM4081 supports all available hosts and the PC platforms with both USB 2.0 and 1.1 interfaces. Complied with USB 2.0 mass storage specification, CBM4081 is fully PnP (plug-and-play) without loading additional driver under Windows Vista, Windows XP, Windows 2000, and MAC 10.x. With device driver installed, it can support Windows 98/98SE as well.

CBM4081 supports SD 2.0/1.1, MMC 3.x/4.0/4.2 specification.

2 Features

- **USB Interface**

  High-speed USB 2.0 interface; backward compatible with USB 1.1
  Integrated USB 2.0/USB1.1 PHY and controller

- **Fastest data transfer rate on the market**

  High speed mode: 30MB/s for Read, 20MB/s for Write

- **General feature list**

  Internal regulators
  Internal POR
  Internal power MOSFET for controlling card power supply
  Support multiple disk drives emulation
  Support passive crystal oscillator

- **MMC card support feature**
  Support MMC version 4.2/4.0/3.3
  Support high voltage mode
  Support high speed mode
  Support 1/4/8 bit bus mode
  Support high capacity card up to 32GB
  Support MMC card hot plug and removal

- **SD card support feature**

  Support SD version 2.0/1.1
  Support high voltage mode
  Support 1/4 bit bus mode
  Support SDHC card up to 32GB
  Support SD card write protection
  Support SD card hot plug and removal

- **Proven 32-bit microprocessor**

- **Integrated dual voltage regulators**

- **LED indicator to display access status**

  Three modes: busy, waiting, and off

- **USB suspend and resume**
- **Low power dissipation**
- **User friendly Windows based GUI application for value-added applications production**
- **Support value-added memory card applications using CBM3080 SD/MMC controller.**
- **CMOS 0.16um technology**
- **Windows Vista/XP/2000/98/ME, Mac10.x and Linux compatible**

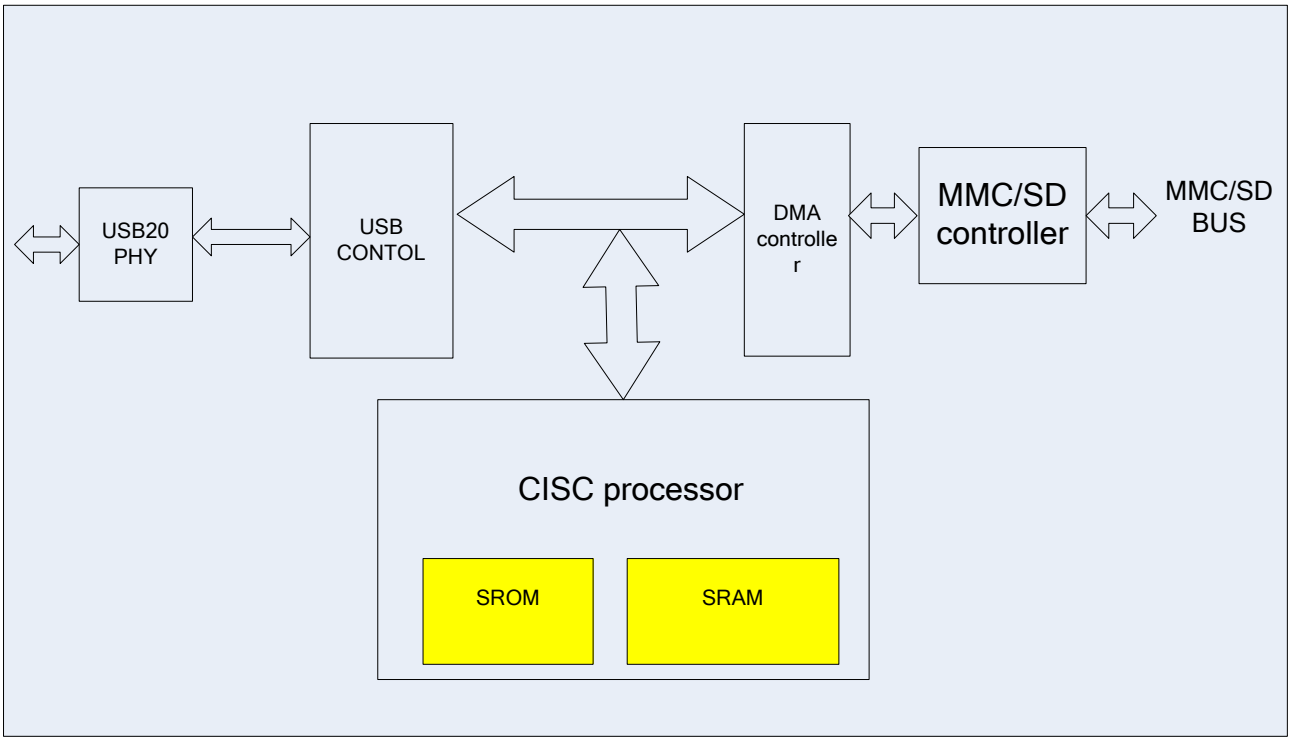
Compares with CBM4080, 4081 make the following modifications.

1 CBM4081 removes SPI / I2C interfaces.
5 PINS: E2P_WPn、SPI_CSn、SPI_CLK、SPI_MISO_I、SPI_MOSI_O are removed on 4081 chip.

2 PACK_SEL pin on 4081 is a little difference from 4080.
For 4081: when PACK_SEL=1, do NOT support 8bit MMC mode;
For 4080: when PACK_SEL=0, do NOT support 8bit MMC mode.
By default, PACK_SEL pulls up in both 4080 and 4081 cases.

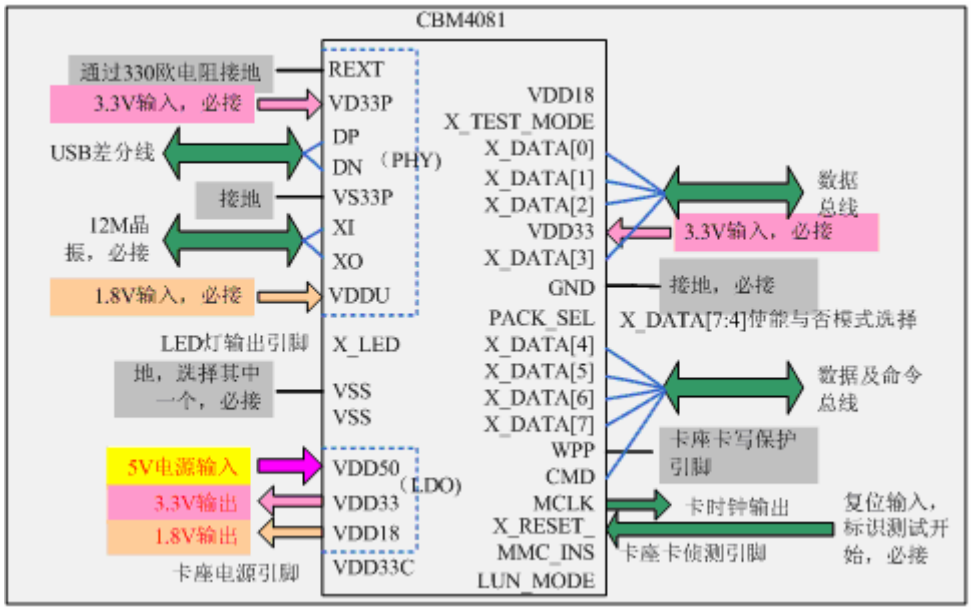
3 New Pin LUN_MODE PAD added.
If high (by default), disk driver emulation enabled once connecting with USB host; else, disk driver emulation enabled only if card insertion happens.

3 Block Diagram



4 Pin Assignment

4.1 Die outline and PAD information

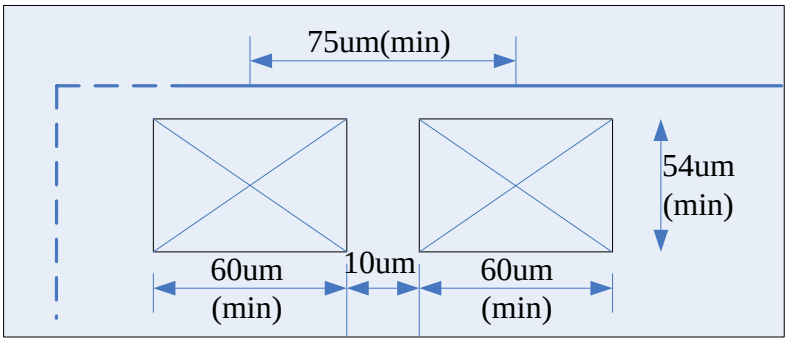


CBM4081 Die outlines and PAD information

【DIE SIZE】

DIE SIZE (Width × Height): 1924.542um × 789.363um = 1519162.246746 (um×um)

【PITCH & SLICE】



CBM4081 minimum pad size is 54um×60um, minimum pad pitch is 75um

4.2 PIN Description

Brief CBM4081 pin functions are shown in the following tables.

I: Input signal

O: Output signal

I/O: Bi-direction signal

PWR: Power signal

PU: Pull up

PD: Pull down

GND: Ground signal

NOTE: **TBD**—to be defined later.

CBM4081 pad description

BOTTOM BAR			
Pad No.	**Pad Name**	**Type**	**Description**
1	REXT	**I**	To connect an external reference resistor for current source of the USB high-speed driver.
2	VD33P	**PWR**	PHY analog 3.3V power input
3	DP	**I/O**	USB D+
4	DM	**I/O**	USB D-
5	VS33P	**GND**	PHY ground
6	XI	**I**	12MHz Crystal input
7	XO	**O**	12MHz Crystal output
8	VDDU	**PWR**	PHY digital power 1.8V input
9	X_LED	**I/O**	LED indication ①
10	VSS	**GND**	Ground
11	VSS	**GND**	Ground
12	VDD50	**PWR**	Regulator power input, connect with USB Connector VBUS line
13	VDD33	**PWR**	regulator 3.3V power output
14	VDD18	**PWR**	regulator 1.8V power output
15	VDD33C	**PWR**	Output 3.3V Power Source for SD/ MMC Card

TOP BAR			
16	LUN_MODE	**I(PU)**	LUN mode deciding pin. If high (by default), disk driver emulation enabled once connecting with USB host; else, disk driver emulation enabled only if card insertion happens.
17	MMC_INS	**I(PU)**	MMC card inserted indication signal. When low, card inserted; else, card un-inserted.
18	X_RESET_	**I(PU)**	Globe Reset, active low ③
19	MCLK	**O**	MMC/SD clock bus
20	CMD	**I/O(PU)**	MMC/SD CMD bus
21	WPP	**I(PU)**	MMC/SD write protected, active low ②
22	X_DATA[7]	**I/O(PU)**	MMC/SD data7
23	X_DATA[6]	**I/O(PU)**	MMC/SD data6
24	X_DATA[5]	**I/O(PU)**	MMC/SD data5
25	X_DATA[4]	**I/O(PU)**	MMC/SD data4
26	PACK_SEL	**I(PU)**	When high (default), DO NOT use X_DATA [7:4], so please NOT bond X_DATA [7:4] out; when prefer to bond X_DATA [7:4] out, be sure that it is also bonded out and pulled-down.
27	GND	**GND**	Digital ground
28	X_DATA[3]	**I/O(PU)**	MMC/SD data3
29	VDD33	**PWR**	Digital I/O 3.3V power input
30	X_DATA[2]	**I/O(PU)**	MMC/SD data2
31	X_DATA[1]	**I/O(PU)**	MMC/SD data1
32	X_DATA[0]	**I/O(PU)**	MMC/SD data0
33	X_TEST_MODE	**I(PD)**	When high, as chip test mode. When low , as normal mode
34	VDD18	**PWR**	Core 1.8V input ④

【Notes】

① Inside resistance for X_LED, no peripheral resistance needed to connect X_LED in series.

② WPP pulls up by default, no need to connect a pulling up resistance outside the chip.

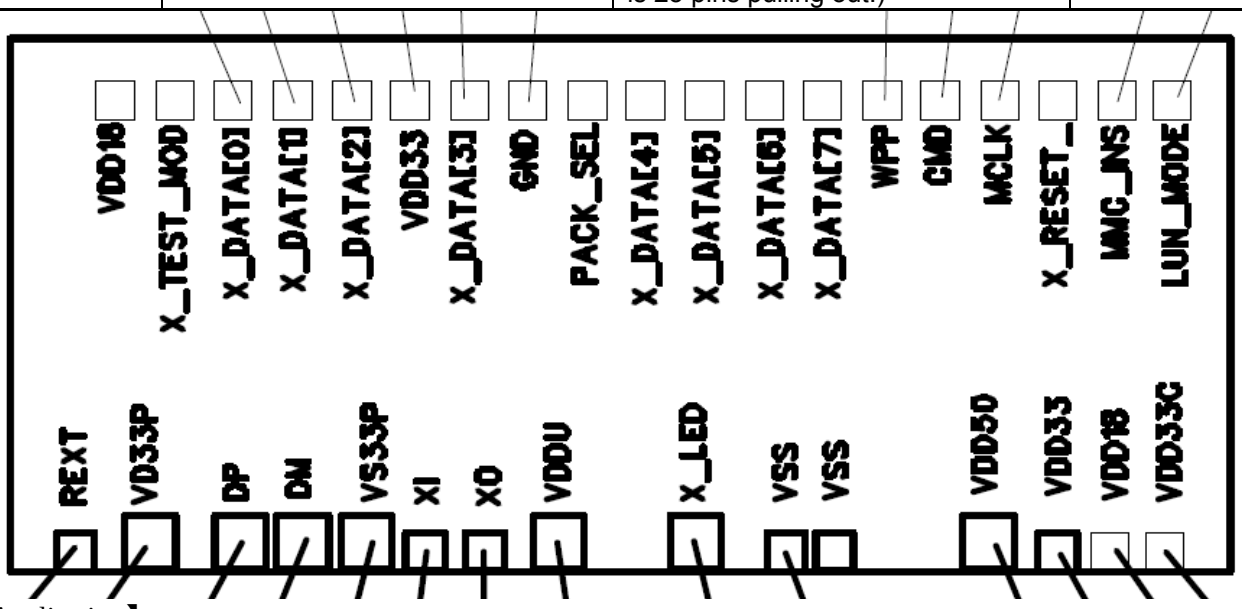
③ X_RESET pulls up by default, no need to connect a pulling up resistance to avoid unexpected reset.

④ No need to connect this PIN to the 14th PIN.

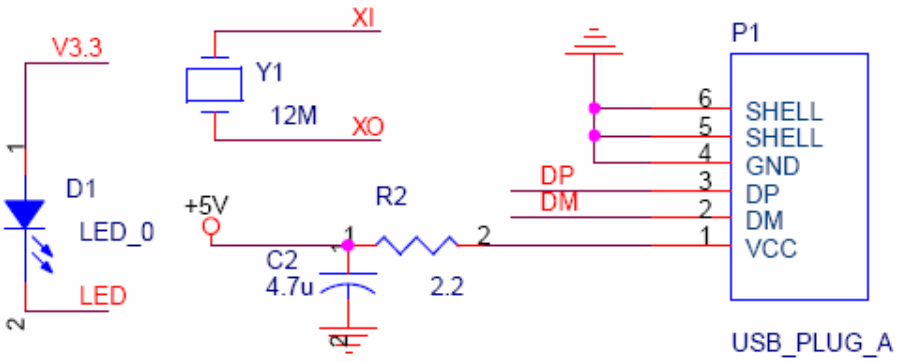
5 COB Resolutions

5.1 4-bit MMC/SD available

COB schematic examples			
EG. INDEX	**Description**		**NOTE**
NO.1	4-bit-MMC/SD available	24 pins pulls out (If LUN_MODE pulls out and connects with GND, it is 25 pins pulling out.)	Most common COB schematic

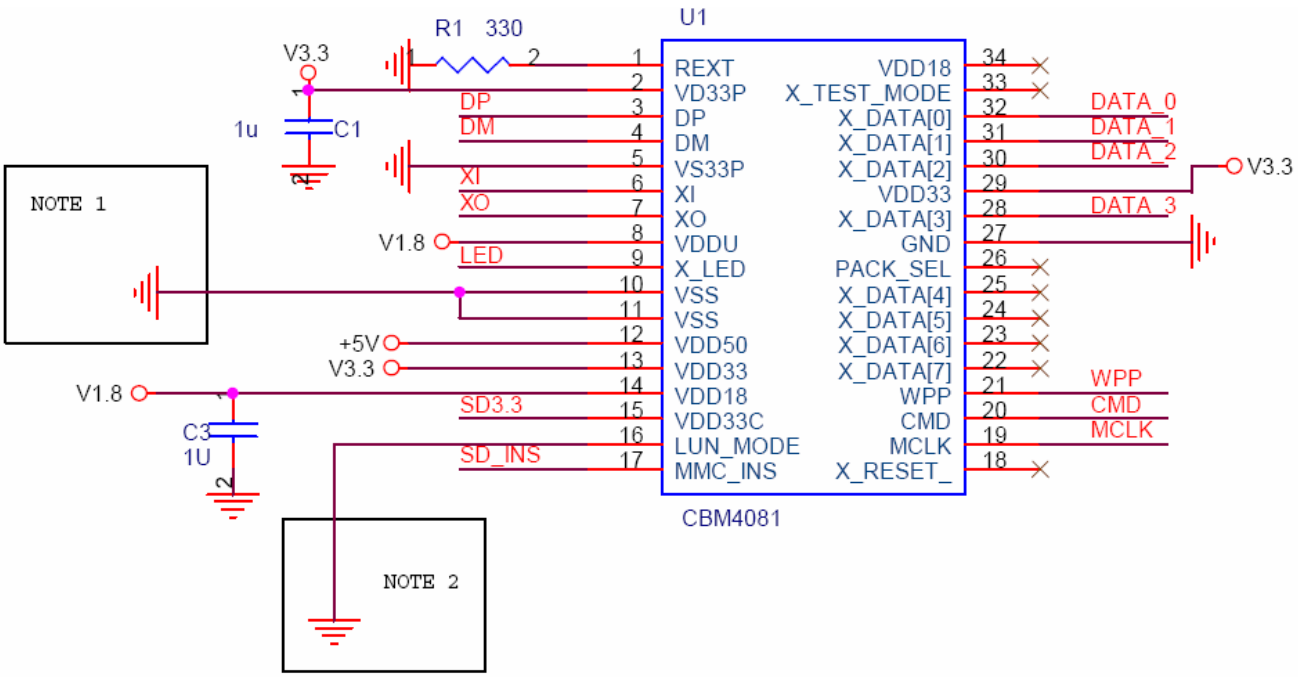


【Application】



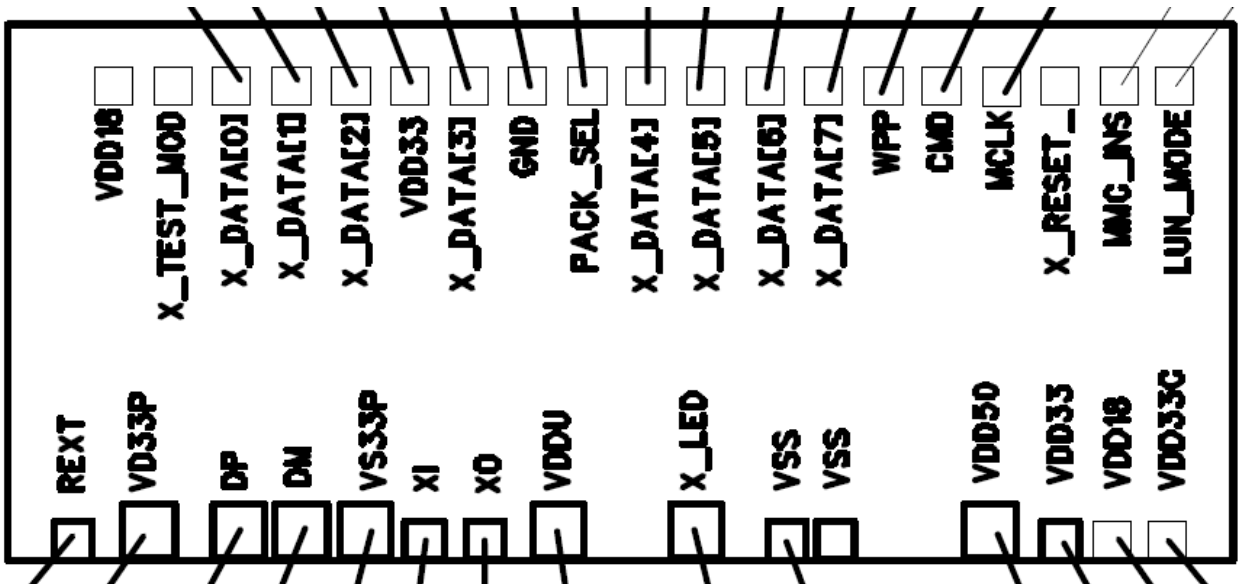
NOTE 1:
只需邦出一根地线即可，可参照邦定图

NOTE 2:
邦出接地则读卡器插卡上盘、拔卡去盘，
如果不邦出悬空则上电上盘，插卡、拔卡均不去盘符

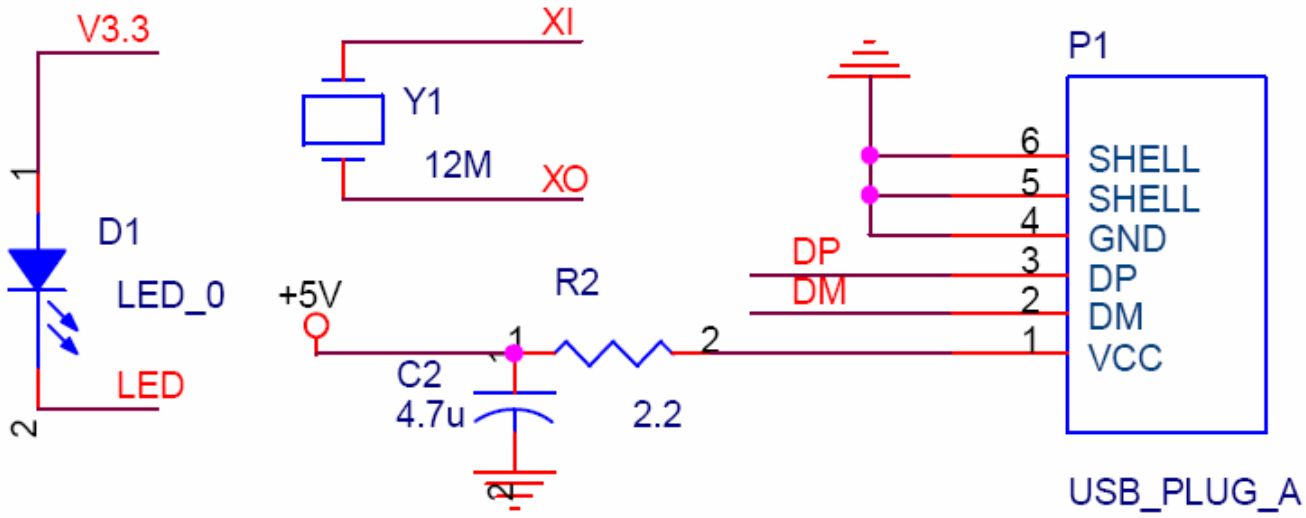


5.2 8-bit MMC/SD available

COB schematics examples			
EG. INDEX	**Description**		**NOTE**
NO.2	8-bit-MMC/SD available	PACK_SEL should be bonded out and connected with low.	



【Application】



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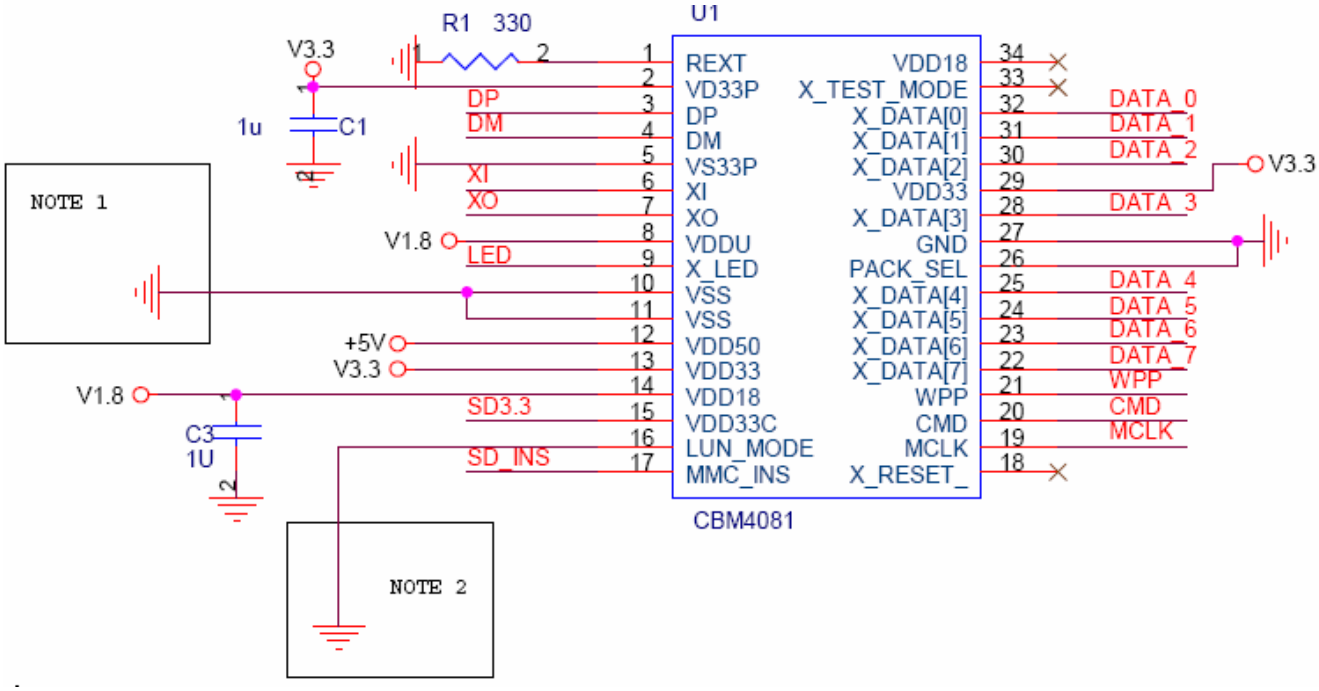


Peripheral component lists:

R1	330ohm	USB PHY
R2	2.2ohm	USB VBUS restraining resistance
C1	1uF	VDD33 filter Capacity
C2	4.7uF	VBUS filter Capacity
C3	1uF	VDD18filter Capacity

Total: 5

6 Electrical Characteristics

6.1 Absolute maximum ratings

In accordance with the Absolute Maximum Rating System (IEC 60134)

symbol	parameter	conditions		min	max	unit
VCCA	analog supply voltage			-0.5	5.5	v
VCCD	digital supply voltage			-0.5	4.5	v
VI	input voltage			-0.5	5.5	v
Vesd	electrical static discharge voltage[1]	ILI < 1 A	DP, DM and GND pins, SD/MMC bus	-4000	+4000	v
			other pins	-2000	+2000	
Tstg	storage temperature			-40	+125	℃

[1] Equivalent to discharging a 100 pf capacitor via a 1.5 K ohm resistor (Human Body Model).

6.2 Recommended operating conditions

symbol	Parameter	conditions	min	typ	max	Unit
VDD50	USB supply voltage		4.5	5.0	5.5	V
VI	input voltage		0	-	VDD50	V
Tamb	ambient temperature		0	-	+70	℃

6.3 Static characteristics

All parameters are measured at VCCA = VCCD = 3.0 to 3.6 V; VAGND = VDGND = 0 V; Tamb = -40 to 85 ℃;

symbol	Parameter	conditions	min	typ	max	Unit

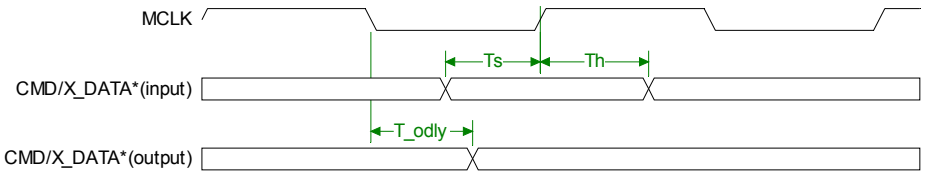
ICC	operating supply current	Full-speed transmitting and receiving;	-	29.5	-	mA
		high-speed transmitting and receiving	-	50		
ICC(susp)	suspend supply current	in suspend mode, auto disconnect current card	-	500		uA

6.4 Dynamic characteristics

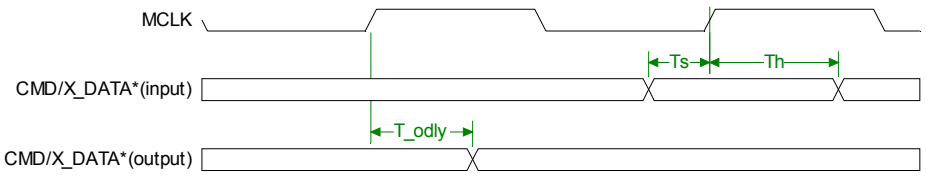
symbol	Parameter	conditions	min	typ	max	Unit
fpp[1]	MCLK frequency in Data Transfer Mode		0		50	MHz
fOD	MCLK frequency in Identification Mode		0		300	KHz
Ts(CMD/X_DATA*)	CMD/X_DATA* setup time relative to MCLK		6			ns
Th(CMD/X_DATA*)	CMD/X_DATA* hold time relative to MCLK		3			ns
Todly(CMD/X_DATA*)	CMD/X_DATA* output delay relative to MCLK				14(for data transfer mode); 50(for identification mode)	ns
Ts(SPI_MISO_I)	SPI_MISO_I setup time relative to SPI_CLK			5		ns
Th(SPI_MISO_I)	SPI_MISO_I hold time relative to SPI_CLK			5		ns
Todly(SPI_MOSI_O)	SPI_MOSI_O output delay relative to SPI_CLK			5		ns
Th(SPI_MOSI_O)	SPI_MOSI_O hold time relative to SPI_CLK			5		ns

[1] For different card, the maximum frequency differs.

Timing diagram for SD/MMC normal speed read/write operation



Timing diagram for SD/MMC high speed read/write operation



7 Typical Application

TBD by application engineer

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