CBT3125

Quadruple FET bus switch

Rev. 2 — 1 October 2018 Product data sheet

1. General description

The CBT3125 quadruple FET bus switch features independent line switches. Each switch is disabled when the associated output enable ($n\overline{OE}$) input is HIGH.

2. Features and benefits

- Standard ’125’-type pinout
- 5 Ω switch connection between two ports
- TTL-compatible input levels
- Latch-up performance exceeds 500 mA per JESD78
- ESD protection:
  - HBM JESD22-A114 exceeds 2000 V
  - MM JESD22-A115 exceeds 200 V
  - CDM JESD22-C101 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
CBT3125D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
CBT3125DB	-40 °C to +85 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
CBT3125PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

nexperia

4. Functional diagram

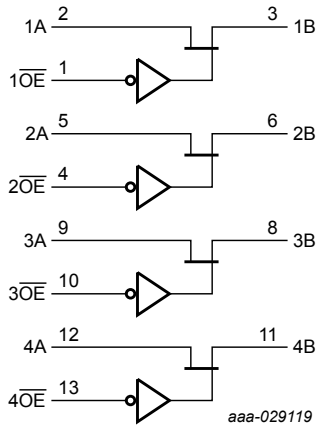


Fig. 1. Logic diagram

5. Pinning information

5.1. Pinning

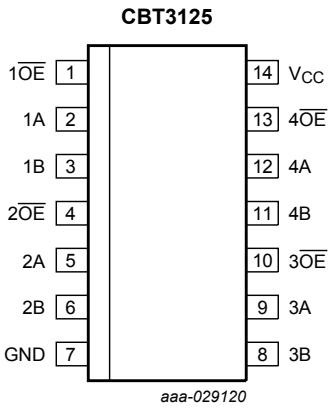


Fig. 2. Pin configuration SOT108-1 (SO14)

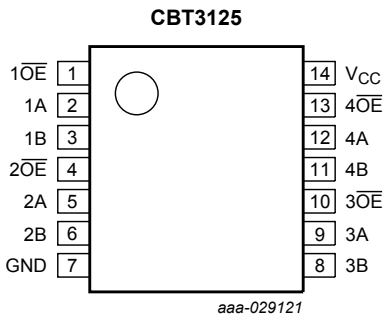


Fig. 3. Pin configuration SOT337-1 (SSOP14) and SOT402-1 (TSSOP14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	1, 4, 10, 13	output enable input (active LOW)
1A, 2A, 3A, 4A	2, 5, 9, 12	data input
1B, 2B, 3B, 4B	3, 6, 8, 11	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Output enable input $n\overline{OE}$	Function switch
L	ON-state (nA = nB)
H	OFF-state

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134); T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[1]	-0.5	+7.0	V
I_O	output current		-	128	mA
I_{IK}	input clamping current	$V_{I/O}$ < 0 V	-	−50	mA
T_{stg}	storage temperature		−65	+150	°C

[1] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	[1]	4.5	-	5.5	V
T_{amb}	ambient temperature	operating in free air	-40	-	+85	°C

[1] All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{IH}	HIGH-level input voltage	$n\overline{OE}$	2.0	-	-	V
V_{IL}	LOW-level input voltage	$n\overline{OE}$	-	-	0.8	V
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_I = -18 mA	-	-	-1.2	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	-	-	±1	µA
I_{CC}	supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND	-	-	3	µA
ΔI_{CC}	additional supply current	$n\overline{OE}$; per input pin; V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND [2]	-	-	2.5	mA
V_{pass}	pass voltage	V_I = V_{CC} = 5.0 V	-	3.8	-	V
C_I	input capacitance	$n\overline{OE}$; V_I = 3 V or 0 V	-	1.7	-	pF
$C_{io(off)}$	off-state input/output capacitance	V_O = 3 V or 0 V; $n\overline{OE}$ = V_{CC}	-	3.4	-	pF
R_{ON}	ON resistance	V_{CC} = 4.5 V; V_I = 0 V; I_I = 64 mA [3]	-	5	7	Ω
		V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA [3]	-	5	7	Ω
		V_{CC} = 4.5 V; V_I = 2.4 V; I_I = −15 mA [3]	-	10	15	Ω

[1] All typical values are measured at V_{CC} = 5 V, unless otherwise noted, T_{amb} = 25 °C.
[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
[3] Measured by the voltage level between the nA and the nB terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (nA, nB) terminals.

10. Dynamic characteristics

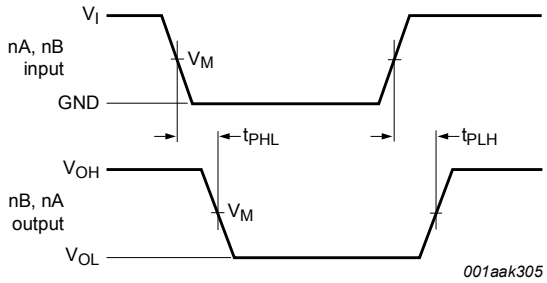
Table 7. Dynamic characteristics

At recommended operating conditions; Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{pd}	propagation delay	nA to nB; nB to nA; see Fig. 4 [1] [2]	-	-	0.25	ns
t_{en}	enable time	$n\overline{OE}$ to nA; $n\overline{OE}$ to nB; see Fig. 5 [2]	1.0	-	5.4	ns
t_{dis}	disable time	$n\overline{OE}$ to nA; $n\overline{OE}$ to nB; see Fig. 5 [2]	1.0	-	4.7	ns

[1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

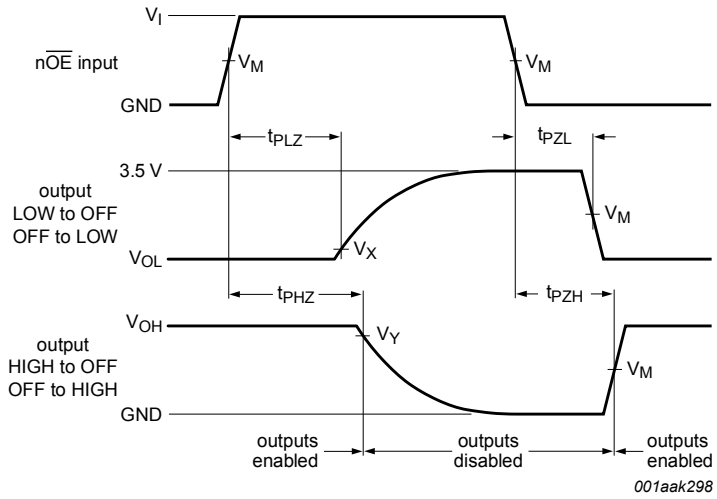
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The data input (nA, nB) to output (nB, nA) propagation delay times



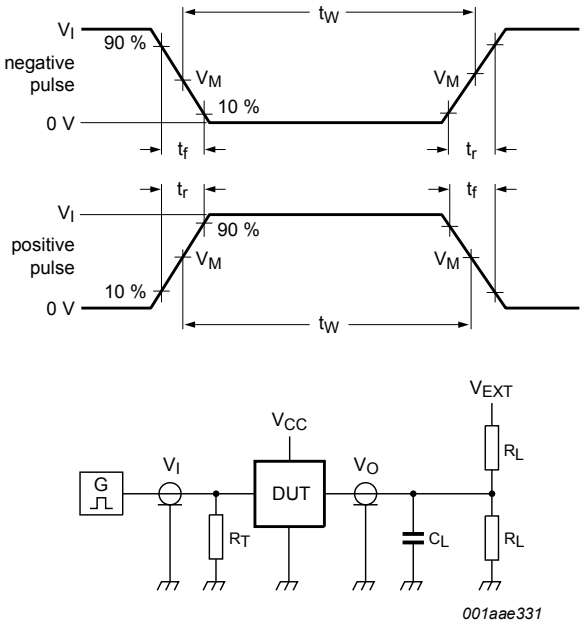
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
V_{CC} = 5.0 V ± 0.5 V	GND to 3.0 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator (Z_o = 50 Ω).

V_{EXT} = External voltage for measuring switching times.

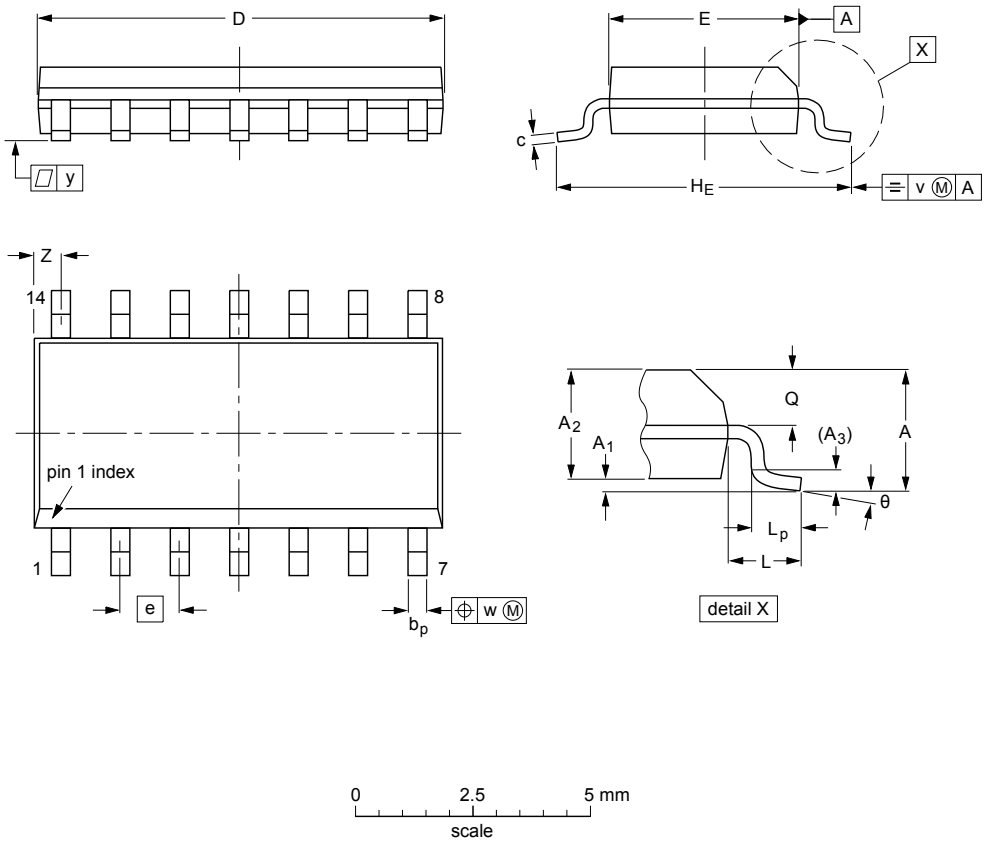
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input			Load		V_{EXT}		
	V_I	t_r, t_f	f_{max}	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
V_{CC} = 5.0 V ± 0.5 V	GND to 3.0 V	≤ 2.5 ns	≤ 10 MHz	50 pF	500 Ω	open	7.0 V	open

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

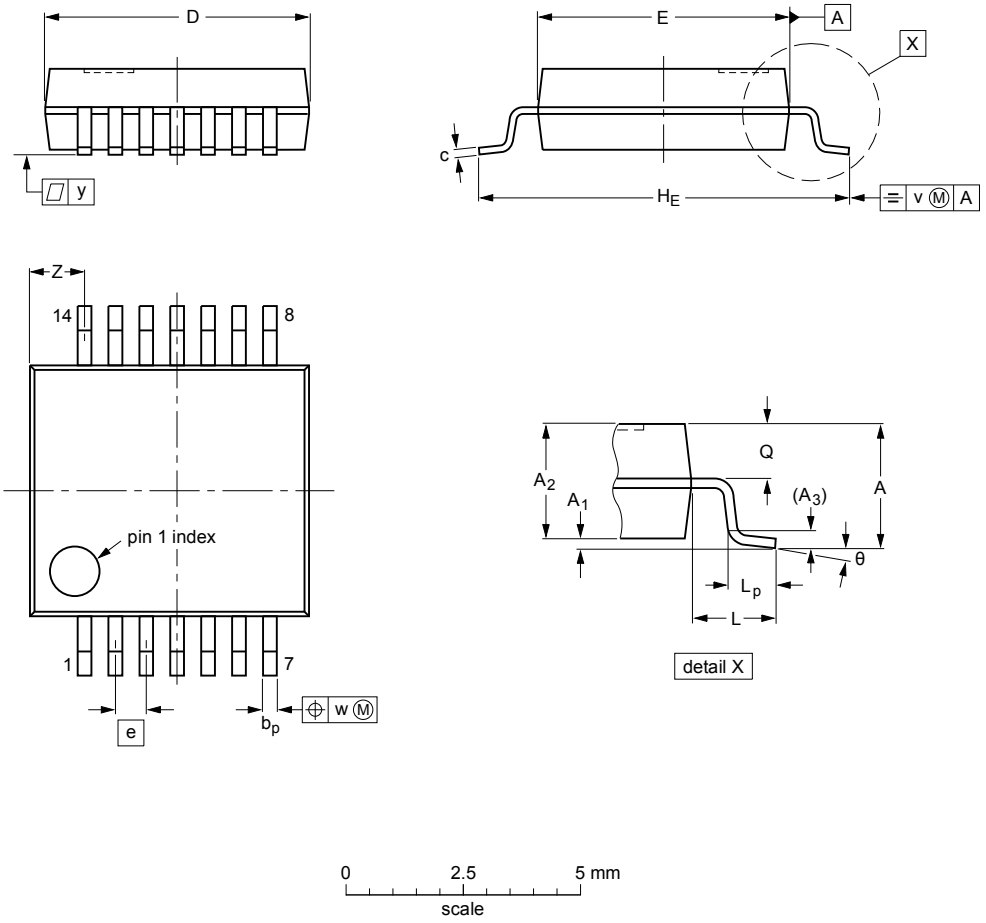
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig. 7. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm **SOT337-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8^o 0^o

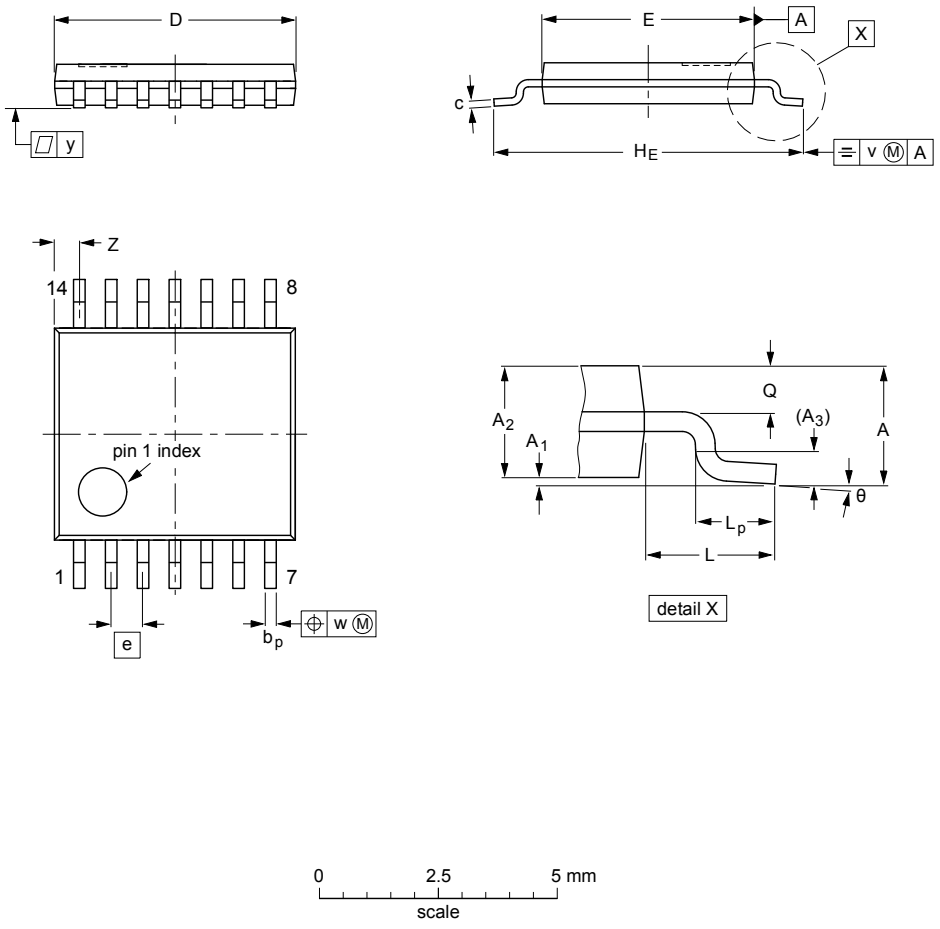
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT337-1		MO-150				~~99-12-27~~ 03-02-19

Fig. 8. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 9. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3125 v.2	20181001	Product data sheet	-	CBT3125 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number CBT3125DS (SOT519-1) removed.			
CBT3125 v.1	20011212	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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