DATA SHEET

CBT3251

1-of-8 FET multiplexer/demultiplexer

Preliminary data

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Philips
Semiconductors

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1-of-8 FET multiplexer/demultiplexer CBT3251

FEATURES

- 5 Ω switch connection between two ports
- TTL-compatible input levels
- Minimal propagation delay through the switch
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 100 mA

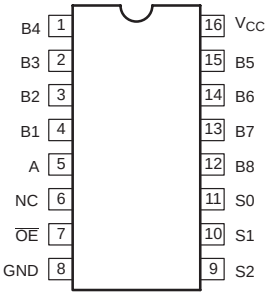
DESCRIPTION

The CBT3251 is a 1-of-8 high-speed TTL-compatible FET multiplexer/demultiplexer. The low on resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

When output enable ($\overline{OE}$) is low, the CBT3251 is enabled. S0, S1, and S2 select one of the B outputs for the A-input data.

The CBT3251 is characterized for operation from –40 to +85°C.

PIN CONFIGURATION



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PIN DESCRIPTION

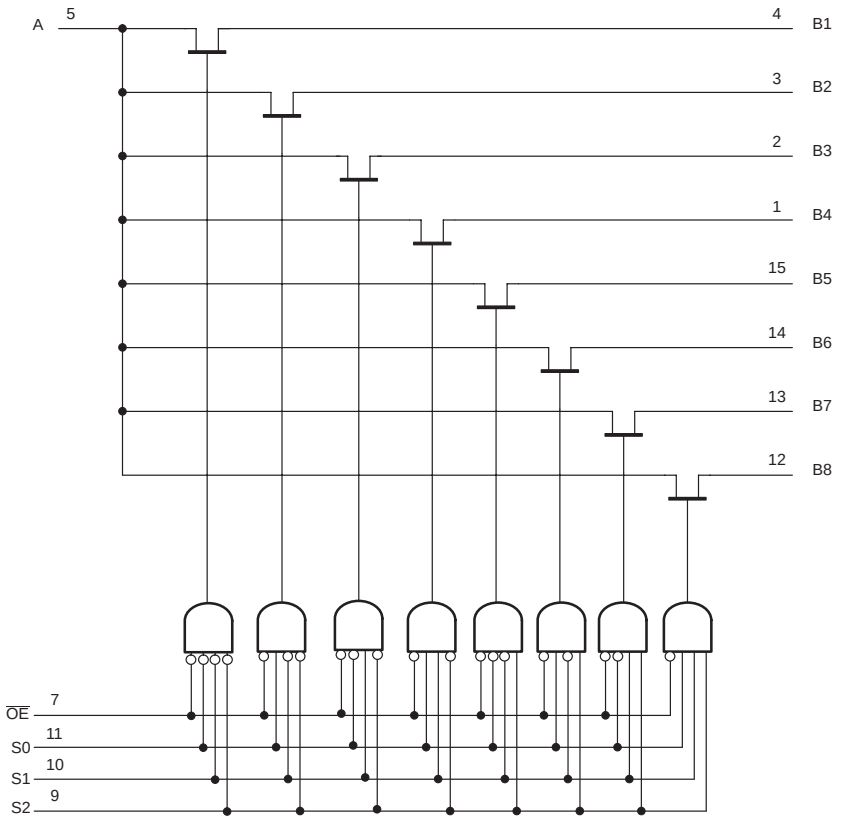
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 12, 13, 14, 15	B1, B2, B3, B4, B5, B6, B7, B8	B outputs
5	A	A input
6	NC	No internal connection
7	$\overline{OE}$	Output enable
8	GND	Ground (0 V)
9, 10, 11	S0, S1, S2	Select-control input
16	V_{CC}	Positive supply voltage

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DWG NUMBER
16-pin plastic SOIC	–40 to 85 °C	CBT3251D	CBT3251D	SOT109-1
16-pin plastic SSOP	–40 to 85 °C	CBT3251DB	CT3251	SOT338-1
16-pin plastic SSOP (QSOP)	–40 to 85 °C	CBT3251DS	CBT3251	SOT519-1
16-pin plastic TSSOP	–40 to 85 °C	CBT3251PW	CBT3251	SOT403-1

Standard packing quantities and other packaging data is available at www.philipslogic.com/packaging.

LOGIC DIAGRAM (positive logic)



FUNCTION TABLE

INPUTS				FUNCTION
$\overline{OE}$	S2	S1	S0	
L	L	L	L	A port = B1 port
L	L	L	H	A port = B2 port
L	L	H	L	A port = B3 port
L	L	H	H	A port = B4 port
L	H	L	L	A port = B5 port
L	H	L	H	A port = B6 port
L	H	H	L	A port = B7 port
L	H	H	H	A port = B8 port
H	X	X	X	Disconnect

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
V_I	DC input voltage[2]		–0.5 to +7.0	V
	Continuous channel current		128	mA
I_{IK}	Input clamp current	$V_{I/O} < 0$	–50	mA
T_{stg}	Storage temperature range		–65 to +150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V_{CC}	DC supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2.0	—	V
V_{IL}	Low-level Input voltage	—	0.8	V
T_{amb}	Operating free-air temperature range	–40	+85	°C

NOTE:
1. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS T_{amb} = –40 to +85 °C			UNIT
				MIN	TYP[1]	MAX	
V_{IK}	Input clamp voltage		V_{CC} = 4.5 V; I_I = –18 mA	—	—	–1.2	V
V_P	Pass voltage		$V_I = V_{CC}$ = 5.5 V; I/O = –100 mA	3.4	3.6	3.9	V
I_I	Input leakage current		V_{CC} = 5.5 V; V_I = GND or 5.5 V	—	—	±1	µA
I_{CC}	Quiescent supply current		V_{CC} = 5.5 V; I_O = 0, $V_I = V_{CC}$ or GND	—	—	3	µA
ΔI_{CC}	Control inputs[2]		V_{CC} = 5.5 V, one input at 3.4 V, other inputs at V_{CC} or GND	—	—	2.5	mA
C_I	Control pins		V_I= 3 V or 0	—	3.5	—	pF
$C_{IO(OFF)}$	Power-off leakage current	A port	V_O = 3 V or 0; $\overline{OE} = V_{CC}$	—	17.5	—	pF
		B port	V_O = 3 V or 0; $\overline{OE} = V_{CC}$	—	4.0	—	pF
r_{on}[3]	On-resistance		V_{CC} = 4 V; TYP @ V_{CC} = 4 V; V_I = 2.4 V; I_I = 15 mA	—	14	20	Ω
			V_{CC} = 4.5 V; V_I = 0 V; I_I = 64 mA	—	5	7	Ω
			V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA	—	5	7	Ω
			V_{CC} = 4.5 V; V_I = 2.4 V; I_I = 15 mA	—	10	15	Ω

NOTES:
1. All typical values are at V_{CC} = 5 V, T_{amb} = 25 °C.
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

AC CHARACTERISTICS

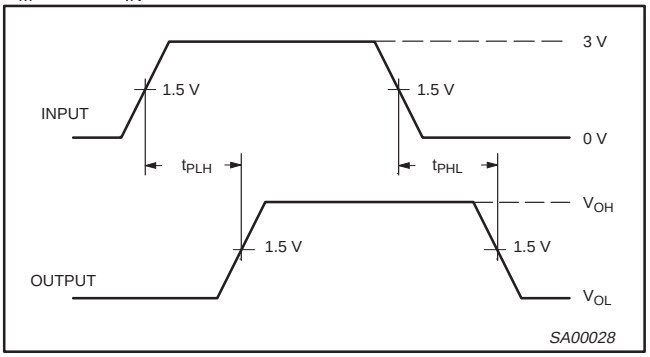
T_{amb} = –40 to +85 °C; C_L = 50 pF

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	LIMITS		UNIT
				V_{CC} = +5.0 V ±0.5 V		
				MIN	MAX	
t_{pd}	Propagation delay[1]	A or B	B or A	—	0.25	ns
t_{pd}	Propagation delay	S	A	2	5.5	ns
t_{en}	Output enable time to High and Low level	S	B	1.5	5.6	ns
		$\overline{OE}$	A or B	1.6	5.8	ns
t_{dis}	Output disable time from High and Low level	S	B	1.9	6.4	ns
		$\overline{OE}$	A or B	2.3	6.2	ns

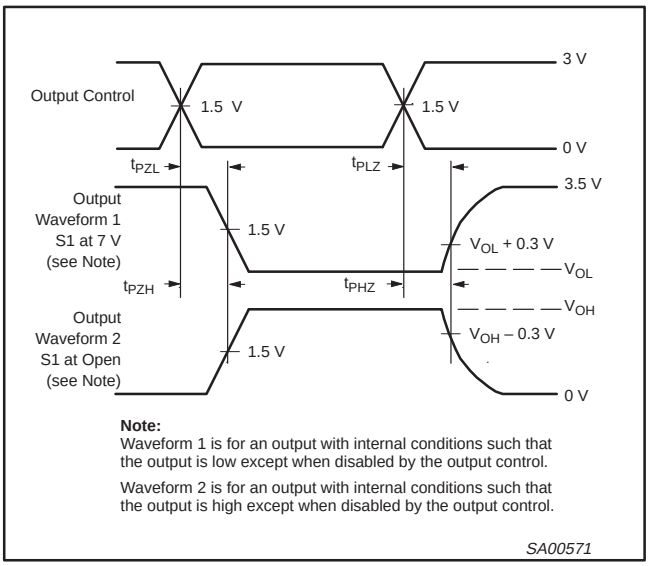
NOTE:
1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

AC WAVEFORMS

V_M = 1.5V, V_{IN} = GND to 3.0V



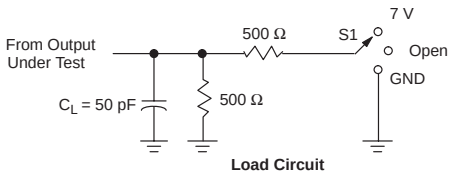
Waveform 1. Input to Output Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

NOTES:
1. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
2. t_{PZL} and t_{PZH} are the same as t_{en}.
3. t_{PLH} and t_{PHL} are the same as t_{pd}.

TEST CIRCUIT AND WAVEFORMS



Load Circuit

TEST	S1
t_{pd}	open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	open

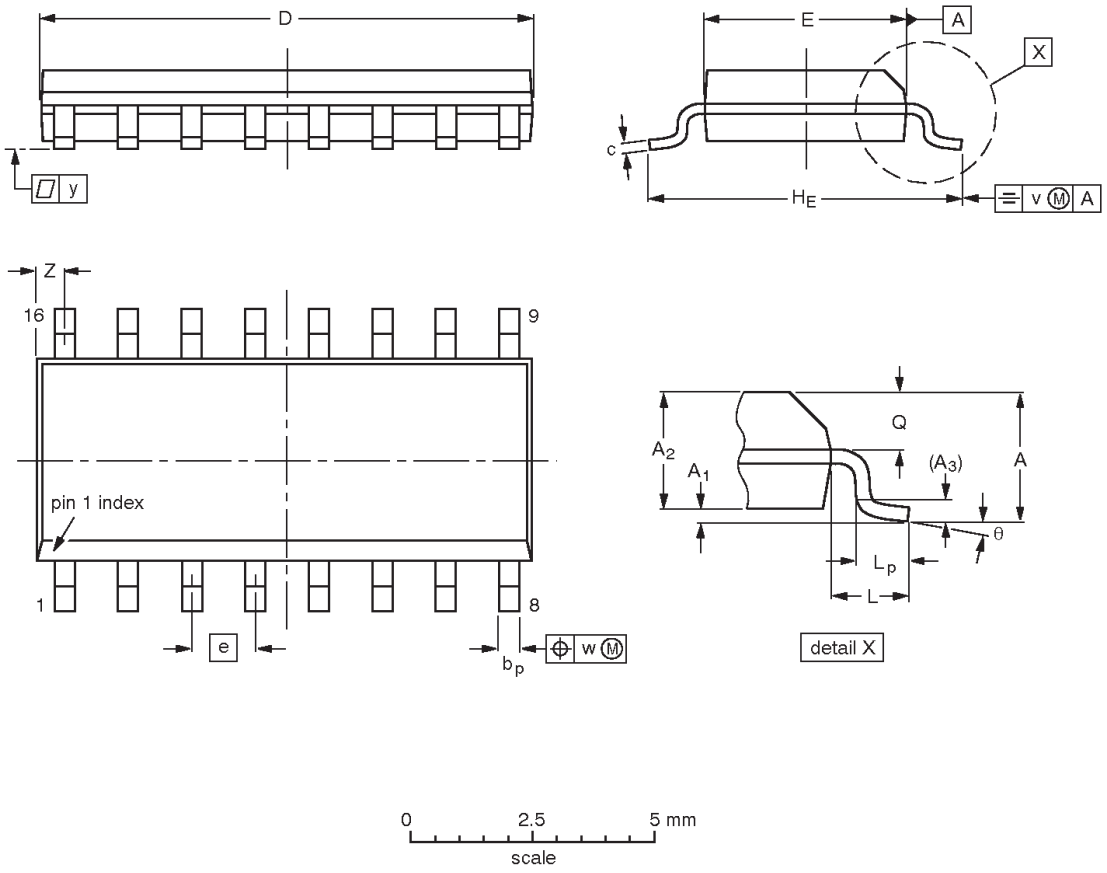
DEFINITIONS

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

SA00012

NOTES:
1. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
2. The outputs are measured one at a time with one transition per measurement.

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

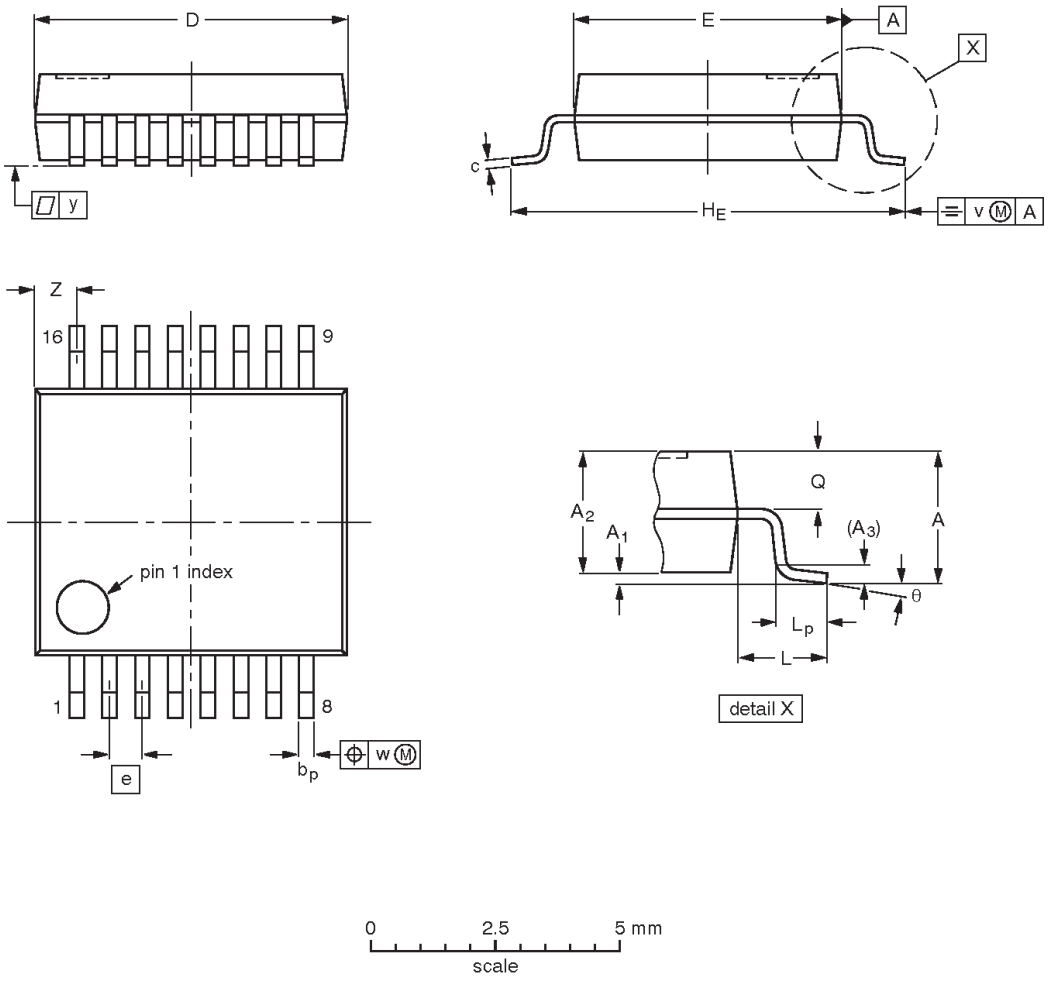
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07	MS-012				~~97-05-22~~ 99-12-27

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

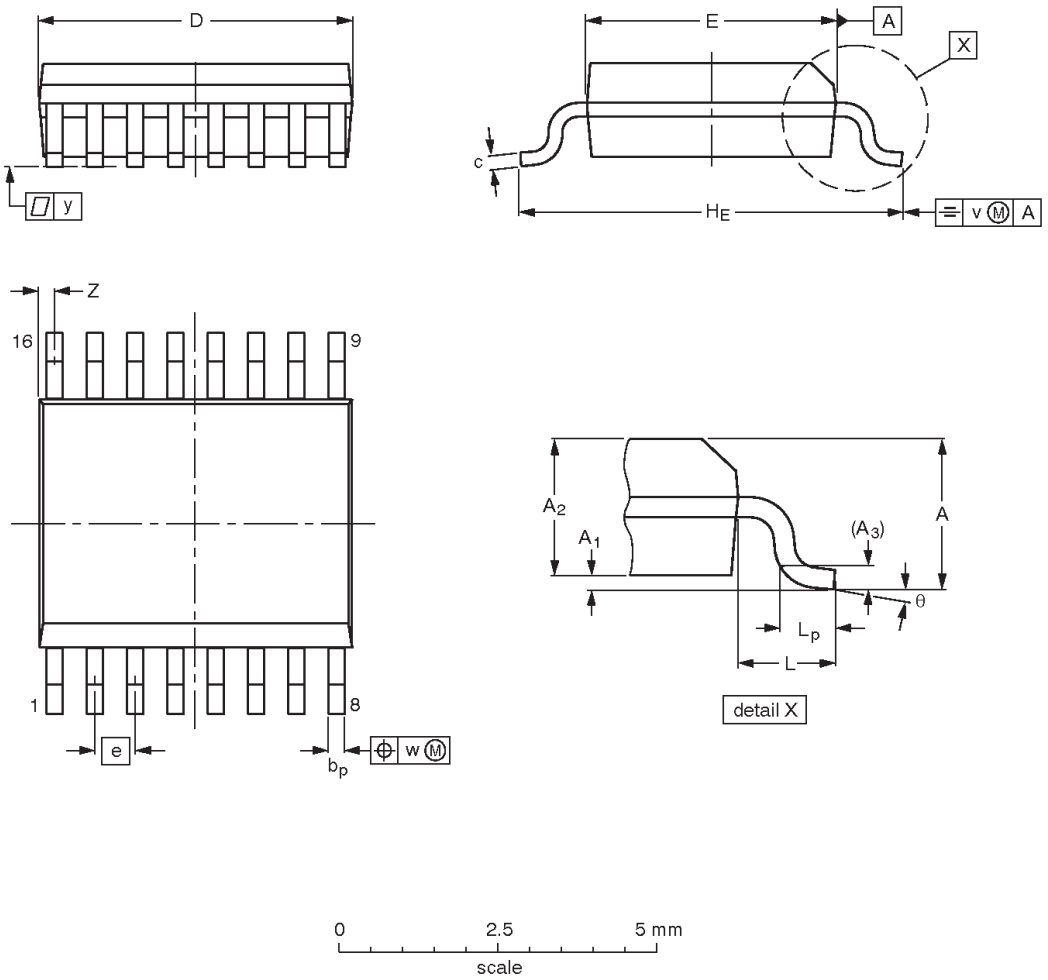
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150				~~95-02-04~~ 99-12-27

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm **SOT519-1**



DIMENSIONS (mm are the original dimensions)

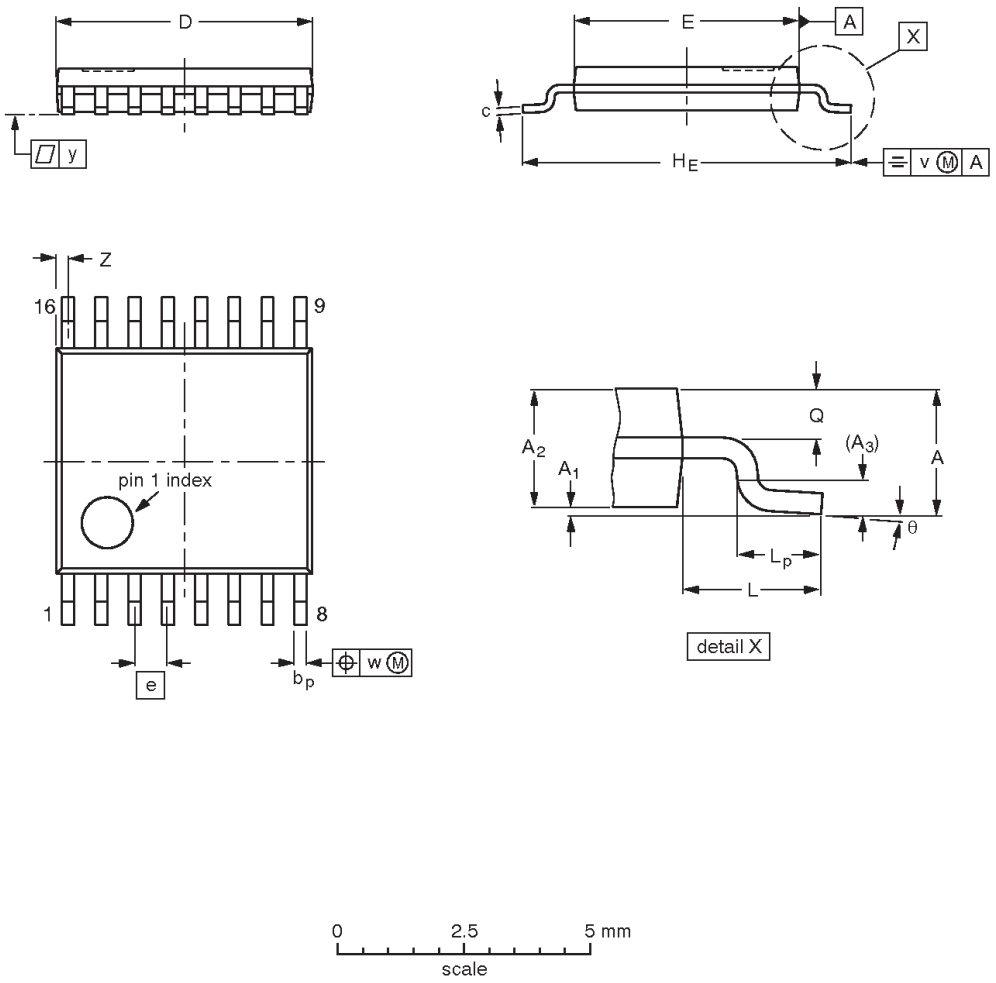
UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	v	w	y	Z (1)	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	5.0 4.8	4.0 3.8	0.635	6.2 5.8	1.0	0.89 0.41	0.2	0.18	0.09	0.18 0.05	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT519-1						99-05-04

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~95-04-04~~ 99-12-27

Data sheet status

Data sheet status [1]	Product status [2]	Definitions
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

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