CBT3861

10-bit bus switch with output enable

Rev. 4 — 6 March 2019 Product data sheet

1. General description

The CBT3861 provides ten bits of high-speed TTL-compatible bus switching. The low ON resistance of the switch allows connections to be made with minimal propagation delay.

The CBT3861 device is organized as one 10-bit bus switches with one output enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the switch is on and port A is connected to the B port. When $\overline{OE}$ is HIGH, each switch is disabled.

The CBT3861 is characterized for operation from -40 °C to +85 °C.

2. Features and benefits

- 5 Ω switch connection between two ports
- TTL-compatible control input levels
- Latch-up protection exceeds 100 mA per JESD78
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - CDM JESD22-C101C exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
CBT3861PW	-40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
CBT3861BQ	-40 °C to +85 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm	SOT815-1

4. Functional diagram

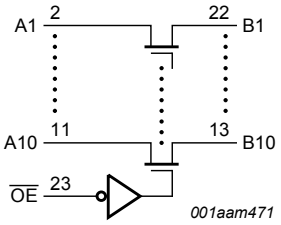


Fig. 1. Logic diagram

5. Pinning information

5.1. Pinning

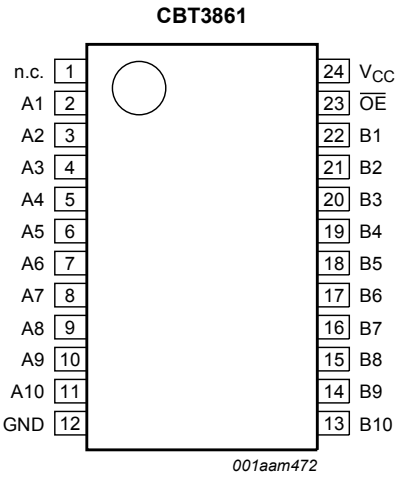
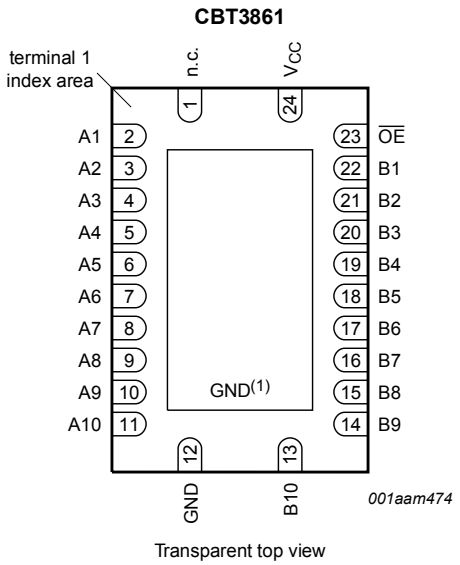


Fig. 2. Pin configuration for TSSOP24 (SOT355-1)



Transparent top view

(1) This is not a supply pin. The substrate is attached to this pad using conductive die attach material. There is no electrical or mechanical requirement to solder this pad. However, if it is soldered, the solder land should remain floating or be connected to GND.

Fig. 3. Pin configuration for DHVQFN24 (SOT815-1)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
nc	1	not connected
A1 to A10	2, 3, 4, 5, 6, 7, 8, 9, 10, 11	data input/output (A port)
GND	12	ground (0 V)
B1 to B10	22, 21, 20, 19, 18, 17, 16, 15, 14, 13	data input/output (B port)
$\overline{OE}$	23	output enable input (active LOW)
V_{CC}	24	positive supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	Input/output
$\overline{OE}$	**An, Bn**
L	An = Bn
H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

T_{amb} = -40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[1]	-0.5	+7.0	V
I_O	output current	V_O < 0 V	-	±128	mA
I_{IK}	input clamping current	$V_{I/O}$ = 0 V	-50	-	mA
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
T_{amb}	ambient temperature	operating in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_I = -18 mA	-	-	-1.2	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	-	-	±1	µA
I_{CC}	supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND	-	-	3	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND [2]	-	-	2.5	mA
V_{pass}	pass voltage	output HIGH; V_I = V_{CC} = 5.0 V; I_O = -100 µA	3.6	3.9	4.2	V
C_I	input capacitance	control pins; V_I = 3 V or 0 V	-	3.0	-	pF
$C_{io(off)}$	off-state input/output capacitance	port off; V_I = 3 V or 0 V; $\overline{OE}$ = V_{CC}	-	5.0	-	pF
R_{ON}	ON resistance	V_{CC} = 4.5 V; V_I = 0 V; I_I = 64 mA [3]	-	5	7	Ω
		V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA [3]	-	5	7	Ω
		V_{CC} = 4.5 V; V_I = 2.4 V; I_I = -15 mA [3]	-	10	15	Ω

[1] All typical values are measured at V_{CC} = 5 V, T_{amb} = 25 °C.

[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

[3] Measured by the voltage drop between the An and the Bn terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (An or Bn) terminals.

10. Dynamic characteristics

Table 7. Dynamic characteristics

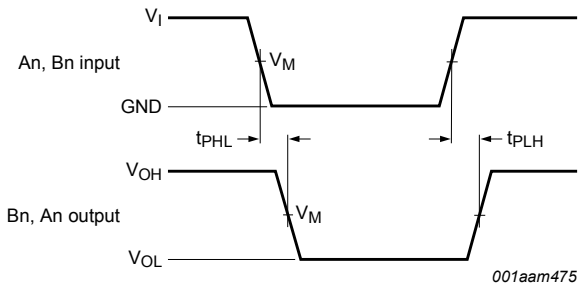
Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = -40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{pd}	propagation delay	An, Bn to Bn, An; see Fig. 4 [1][2]						
		V_{CC} = 5.0 V ± 0.5 V	-	-	0.25	-	0.25	ns
t_{en}	enable time	$\overline{OE}$ to An or Bn; see Fig. 5 [2]						
		V_{CC} = 5.0 V ± 0.5 V	-	3.3	-	1.6	7.5	ns
t_{dis}	disable time	$\overline{OE}$ to An or Bn; see Fig. 5 [2]						
		V_{CC} = 5.0 V ± 0.5 V	-	3.4	-	2.1	6.6	ns

[1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

10.1. Waveforms and test circuit



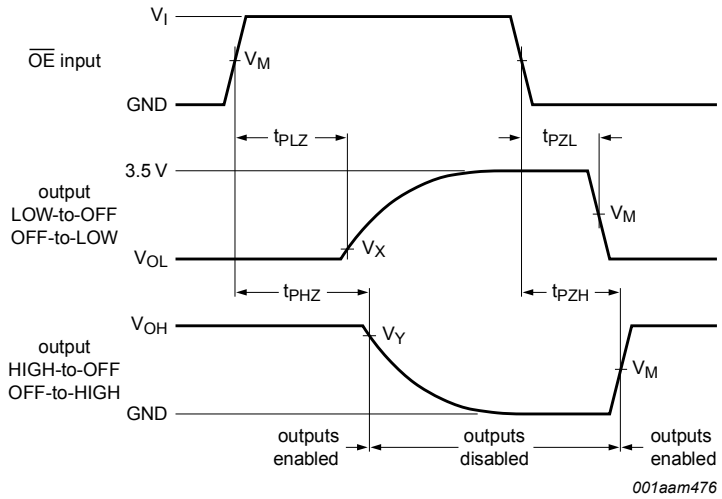
Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The data input (An, Bn) to output (Bn, An) propagation delay times

Table 8. Measurement points

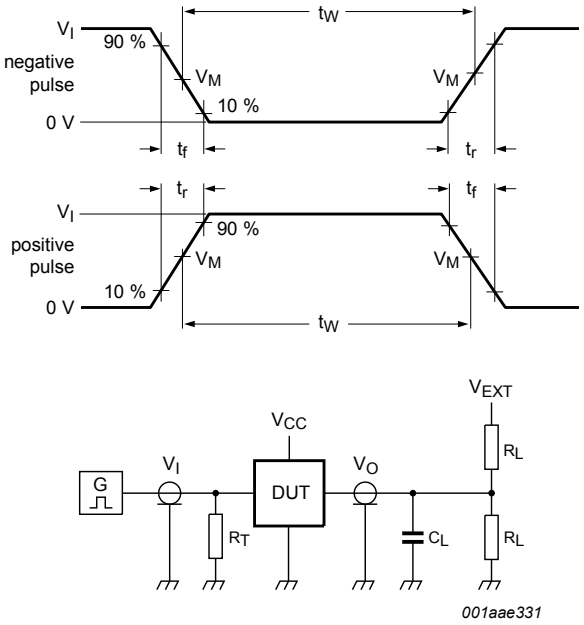
Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
V_{CC} = 5.0 V ± 0.5 V	GND to 3.0 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Measurement points are given in Table 8.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Enable and disable times



Test data is given in Table 9.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω.

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

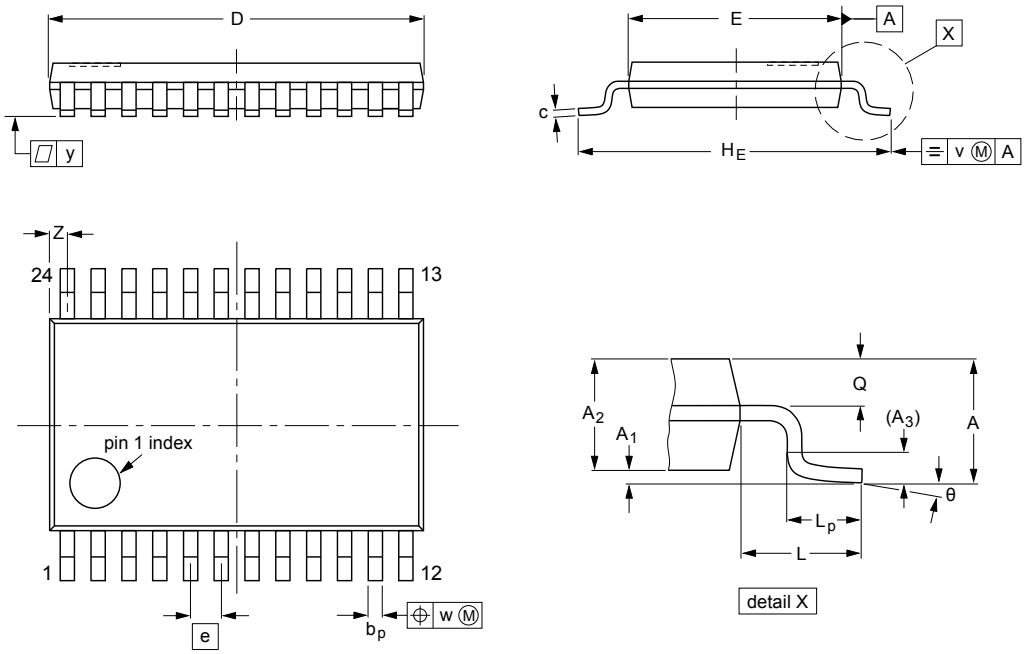
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
V_{CC} = 5.0 V ± 0.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

11. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

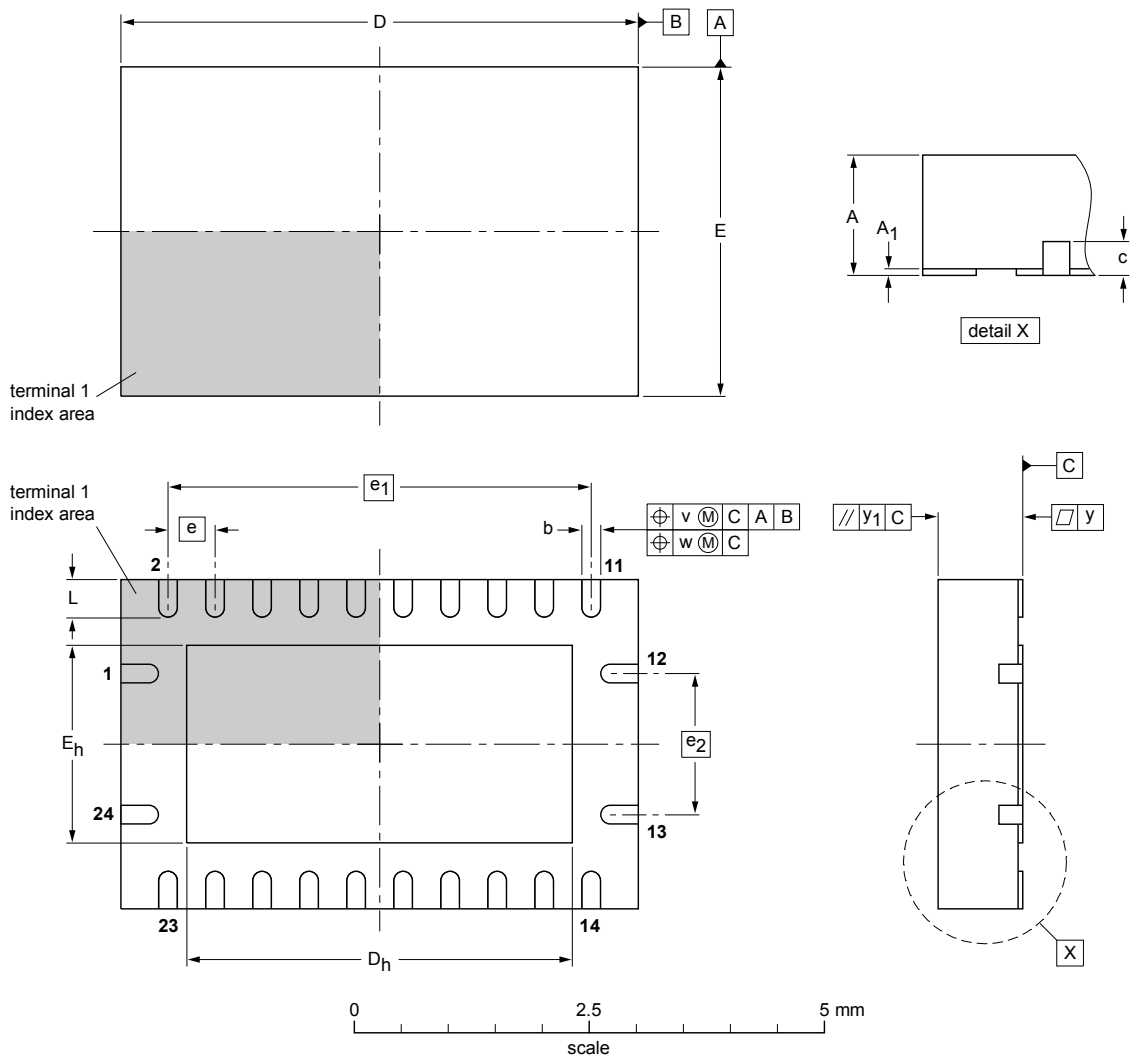
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 7. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

Fig. 8. Package outline SOT815-1 (DHVQFN24)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3861 v.4	20190306	Product data sheet	-	CBT3861 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number CBT3861DK (SOT556-1) removed.			
CBT3861 v.3	20111121	Product data sheet	-	CBT3861 v.2
Modifications:	• Legal pages updated.			
CBT3861 v.2	20101124	Product data sheet	-	CBT3861 v.1
CBT3861 v.1	20100819	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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