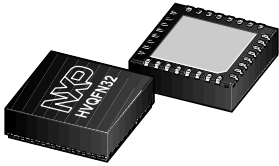


CD1020

22-channel multiple switch detection interface

Rev. 5 — 20 August 2024

Product data sheet



1 General description

The CD1020 is a cost-optimized switch detection interface device (MSDI) designed to detect the closing and opening of up to 22 switch contacts. The switch status, either open or closed, is transferred to the microprocessor unit (MCU) through a Serial Peripheral Interface (SPI). This SMARTMOS device also features a 22-to-1 analog multiplexer for reading the input channels as analog inputs. The analog selected input signal is buffered and provided on the AMUX output pin for the MCU to read.

The CD1020 device has three modes of operation, normal mode, low-power mode (LPM), and polling mode. Normal mode allows programming of the device and supplies switch contacts with pullup or pulldown current as it monitors the change of state on the switches. The LPM provides low quiescent current, which makes the CD1020 ideal for automotive and industrial products requiring low sleep-state currents. Polling mode periodically interrogates the input pins to determine the state the pins are in, and to decide whether there was a change of state from normal mode.

The low-cost MSDI is available in a high-power, space-saving wettable flank 5x5 mm QFN package.

2 Features and benefits

Features and benefits

- Fully functional operation from 6.0 V to 36 V
- Full parametric operation from 6.0 V to 28 V
- Low-power mode current $I_{BATP} = 30 \mu\text{A}$ and $I_{DDQ} = 10 \mu\text{A}$
- 22 Switch detection channels
 - 14 Switch-to-Ground (SG) inputs
 - Eight Programmable switch (SP) inputs
 - Switch-to-Ground (SG) or Switch-to-Battery (SB)
 - Operating switch input voltage range from -1.0 V to 36 V
 - Selectable wetting current (2, 8, 12, 16 mA)
 - Programmable wetting operation (pulse or continuous)
 - Selectable wake-up on change of state
- 22-to-1 Analog Multiplexer
 - Buffered AMUX output from SG/SP channels
- Active interrupt (INT_B) on change-of-switch state
- Direct MCU Interface through 3.3 V / 5.0 V SPI protocol

3 Ordering information

This section describes the part numbers available to be purchased along with their differences.

Table 1. Orderable part variations

Part number	Temperature (T _A)	Package	Notes
MC33CD1020AES	−40 °C to 125 °C	32-pin QFN (WF-type)	(1)
Notes			
1. To order parts in tape and reel, add the R2 suffix to the part number.			

4 Functional block diagram

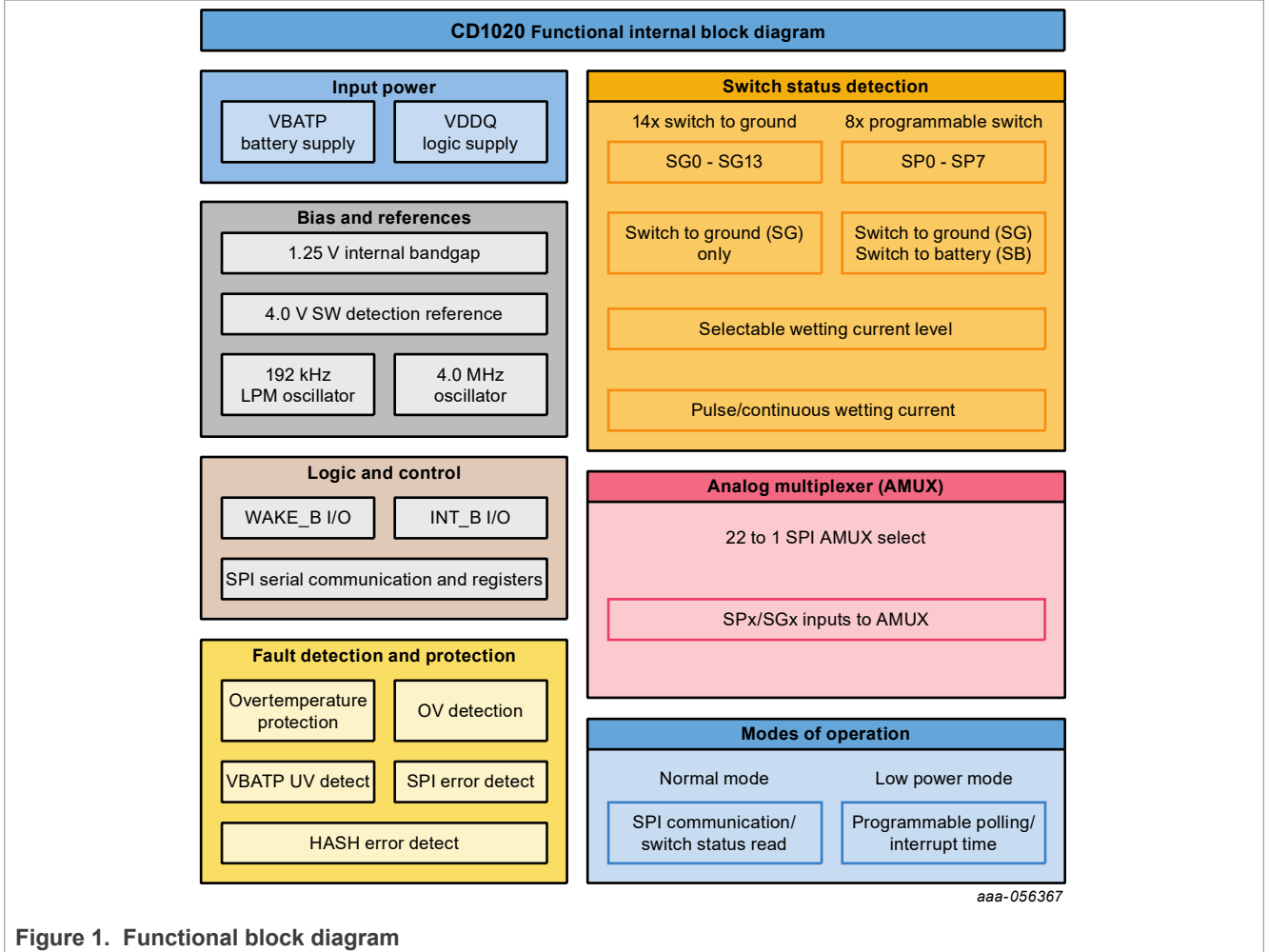


Figure 1. Functional block diagram

5 Internal block diagram

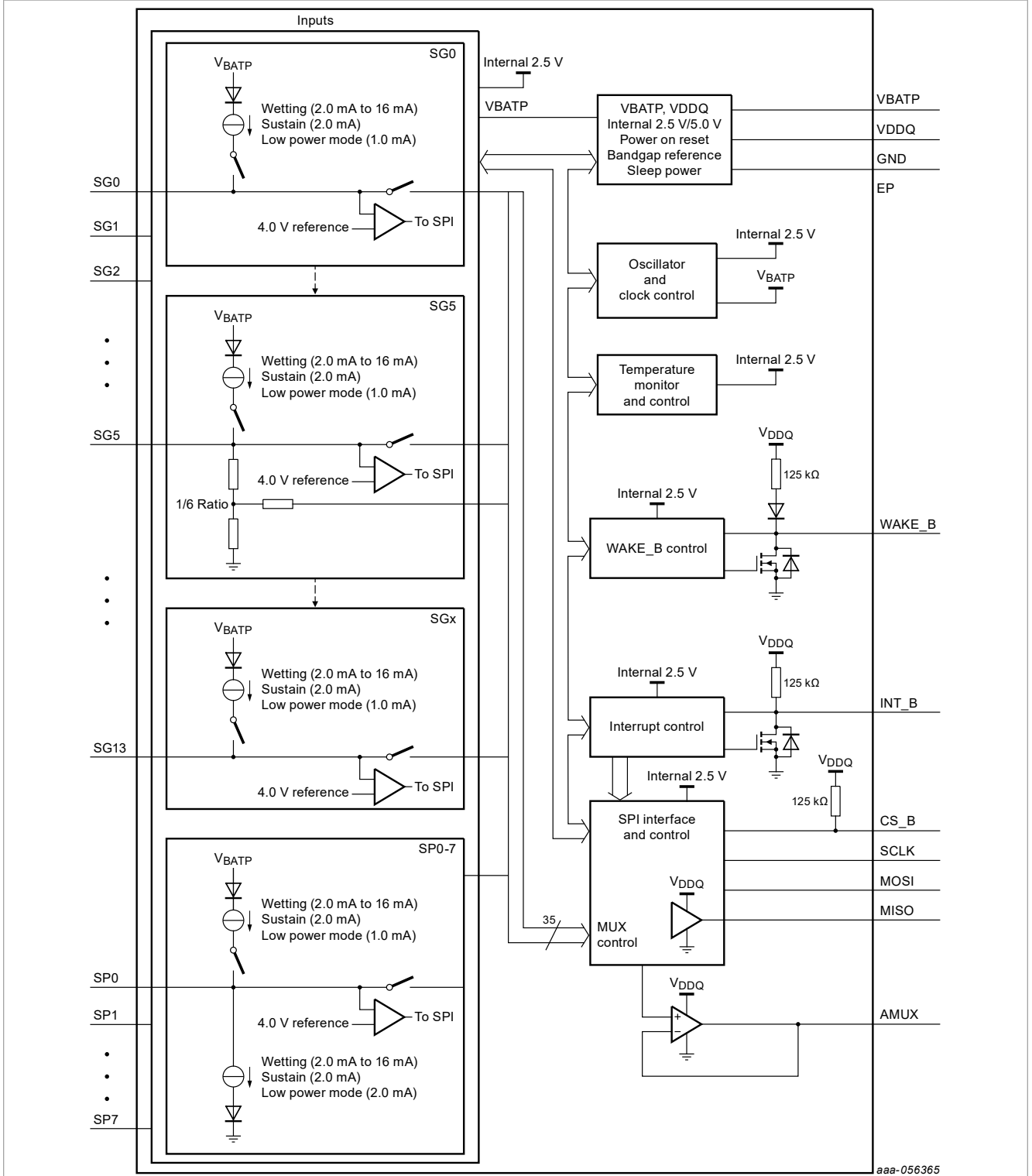


Figure 2. CD1020 internal block diagram

6 Pinning information

6.1 Pinout

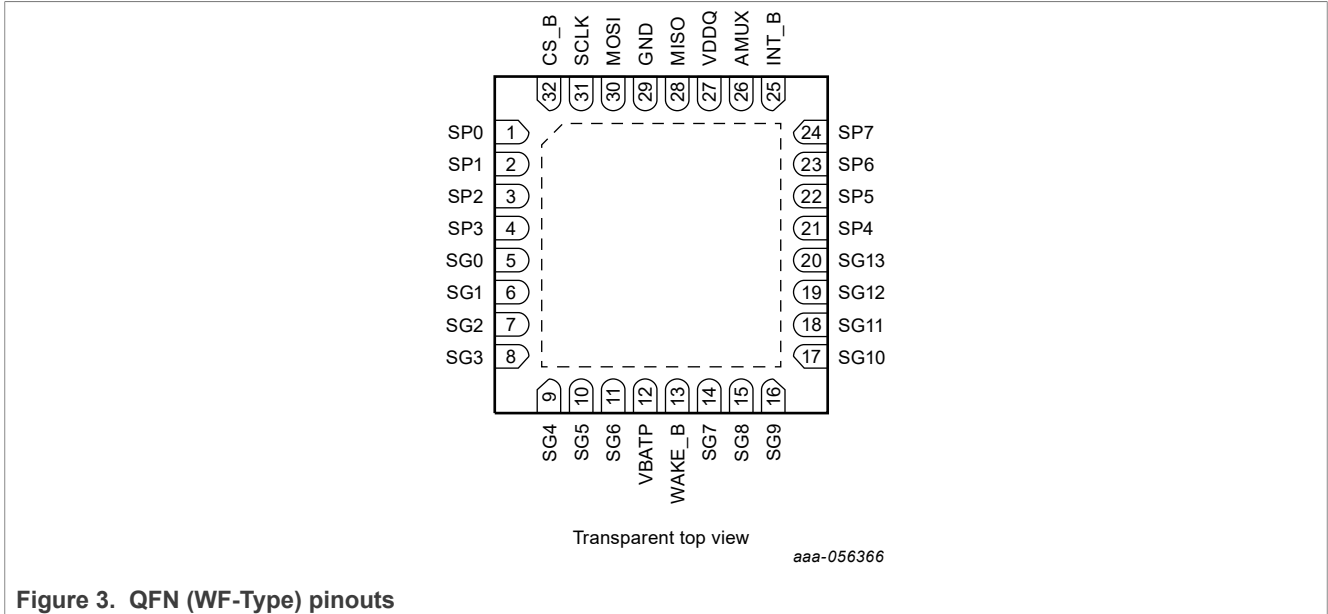


Figure 3. QFN (WF-Type) pinouts

6.2 Pin definitions

Table 2. CD1020 pin definitions

Pin number QFN	Pin name	Pin function	Formal name	Definition
29	GND	Ground	Ground	Ground for logic, analog
30	MOSI	Input/SPI	SPI Secondary In	SPI control data input pin from the MCU
31	SCLK	Input/SPI	Serial Clock	SPI control clock input pin
32	CS_B	Input/SPI	Chip Select	SPI control chip select input pin
1 – 4 21 – 24	SP0 – 3 SP4 – 7	Input	Programmable Switches 0 – 7	Switch to programmable input pins (SB or SG)
5 – 11 14 – 20	SG0 – 6, SG7 – 13	Input	Switch-to-Ground Inputs 0 – 13	Switch-to-ground input pins
12	VBATP	Power	Battery Input	Battery supply input pin. Pin requires external reverse battery protection
13	WAKE_B	Input/Output	Wake-up	Open drain wake-up output. Designed to control a power supply enable pin. Input used to allow a wake-up from an external event.
25	INT_B	Input/Output	Interrupt	Open-drain output to MCU. Used to indicate an input switch change of state. Used as an input to allow wake-up from LPM via an external INT_B falling event.
26	AMUX	Output	Analog Multiplex Output	Analog multiplex output

Table 2. CD1020 pin definitions...continued

Pin number QFN	Pin name	Pin function	Formal name	Definition
27	VDDQ	Input	Voltage Drain Supply	3.3 V/ 5.0 V supply. Sets SPI communication level for the MISO driver and I/O level buffer
28	MISO	Output/SPI	SPI Secondary Out	Provides digital data from the CD1020 to the MCU
	EP	Ground	Exposed Pad	It is recommended that the exposed pad is terminated to GND (pin 1) and system ground.

7 General IC functional description

The CD1020 device interacts with many connections outside the module and near the end user. The IC detects changes in switch state and reports the information to the MCU via the SPI protocol. The input pins generally connect to switches located outside the module and in proximity to battery in car harnesses. Consequently, the IC must have some external protection including an ESD capacitor and series resistors, to ensure the energy from the various pulses are limited at the IC.

The IC requires a blocking diode be used on the VBATP pin to protect from a reverse battery condition. The inputs are capable of surviving reverse battery without a blocking diode, due to an internal blocking diode from the input to the power supply (V_{BATP}). This arrangement ensures that there is no backfeeding of voltage/current into the IC, when the voltage on the input is higher than the VBATP pin.

7.1 Battery voltage ranges

The CD1020 device operates from $6.0\text{ V} \leq V_{BATP} \leq 36\text{ V}$ and is capable to withstand up to 40 V. Voltages in excess of 40 V must be clamped externally in order to protect the IC from destruction. The VBATP pin must be isolated from the main battery node by a diode.

7.1.1 Load dump (overvoltage)

During load dump, the CD1020 operates properly up to the V_{BATP} overvoltage. Voltages greater than load dump (~32 V) cause the current sources to be limited to ~2.0 mA, but the register values are maintained. Upon leaving this overvoltage condition, the original setup is returned and normal operation begins again.

7.1.2 Jump start (double battery)

During a jump start (double battery) condition, the device functions normally and meets all the specified parametric values. No internal faults are set and no abnormal operation noted as a result of operating in this range.

7.1.3 Normal battery range

The normal voltage range is fully functional with all parametrics in the given specification.

7.1.4 Undervoltage

In the undervoltage range, the SPI can work normally, but the device functions are not guaranteed.

7.1.5 Undervoltage lockout

During undervoltage lockout, the MISO output is tristated to avoid any data from being transmitted from the CD1020. Any CS_B pulses are ignored in this voltage range. If the battery enters this range at any point (even during a SPI word), the CD1020 ignores the word and enters lockout mode. A SPI bit register is available to notify the MCU that the CD1020 has seen an undervoltage lockout condition once the battery is high enough to leave this range.

7.1.6 Power-On-Reset (POR) activated

The Power-On-Reset is activated when the VBATP is within the 2.7 V to 3.8 V range. During the POR all SPI registers are reset to default values and SPI operation is disabled. The CD1020 is initialized after the POR is de-asserted. A SPI bit in the device configuration register is used to note a POR occurrence and all SPI registers are reset to the default values.

7.1.7 No operation

The device does not function and no switch detection is possible.

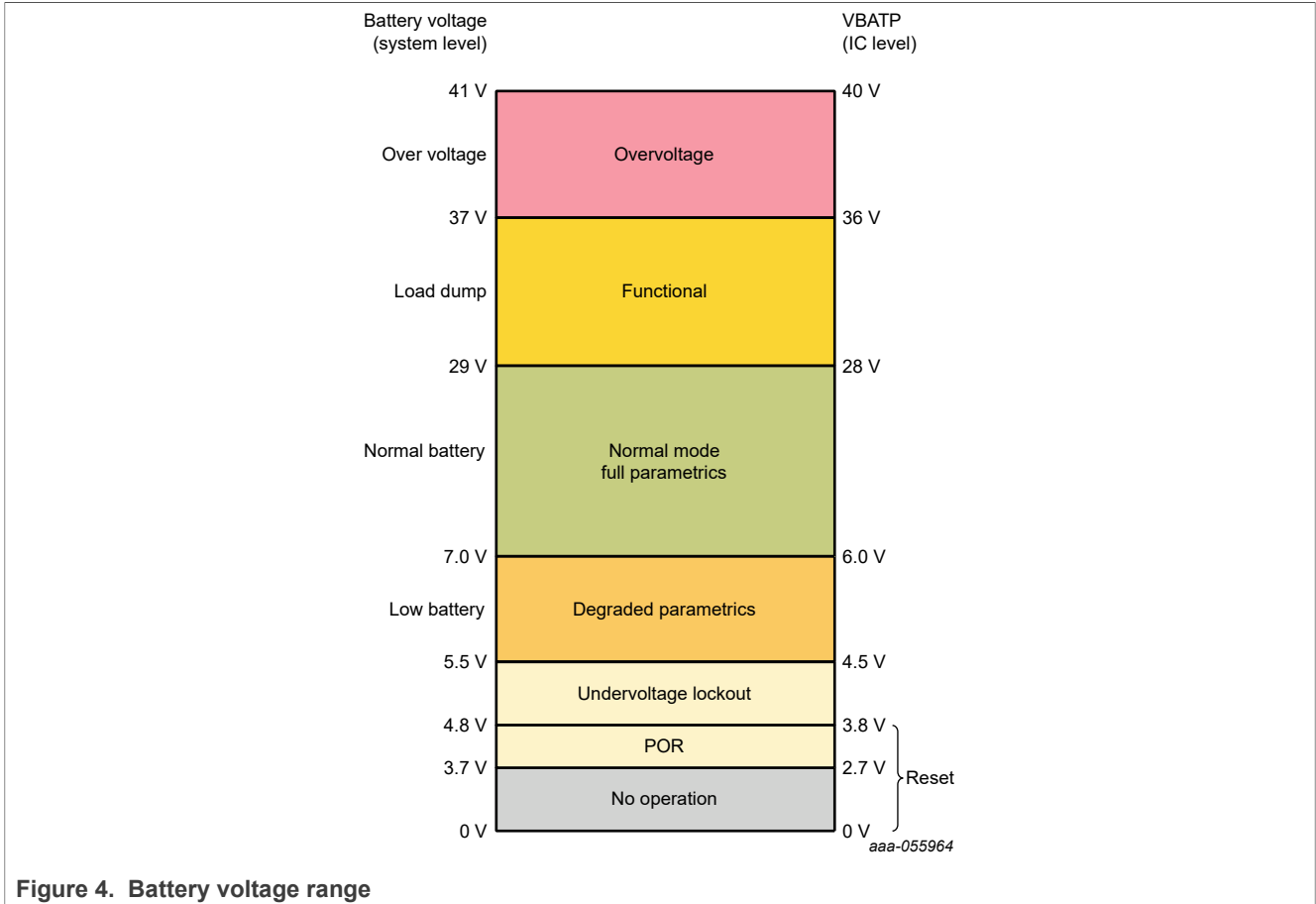


Figure 4. Battery voltage range

7.2 Power sequencing conditions

The chip uses two supplies as inputs into the device for various usage. The pins are VBATP and VDDQ. The VBATP pin is the power supply for the chip where the internal supplies are generated and power supply for the SG circuits. The VDDQ pin is used for the I/O buffer supply to talk to the MCU or other logic level devices, as well as AMUX. The INT_B pin is held low upon POR until the IC is ready to operate and communicate. Power can be applied in various ways to the CD1020. The following sections describe the possible states.

7.2.1 V_{BATP} before V_{DDQ}

The normal condition for operation is the application of V_{BATP} and then V_{DDQ}. The chip begins to operate logically in the default state but without the ability to drive logic pins. When the V_{DDQ} supply is available, the chip is able to communicate correctly. The IC maintains its logical state (register settings) with functional behavior consistent with logical state. No SPI communications can occur.

7.2.2 V_{DDQ} before V_{BATP}

The V_{DDQ} supply in some cases may be available before the V_{BATP} supply is ready. In this scenario, there is no back feeding current into the VDDQ pin that could potentially turn on the device into an unknown state. VDDQ is isolated from VBATP circuits and the device is off until VBATP is applied; when V_{BATP} is available the device

powers up the internal rails and logic within t_{ACTIVE} time. Communication is undefined until the t_{ACTIVE} time and becomes available after this time frame.

7.2.3 V_{BATP} okay, V_{DDQ} lost

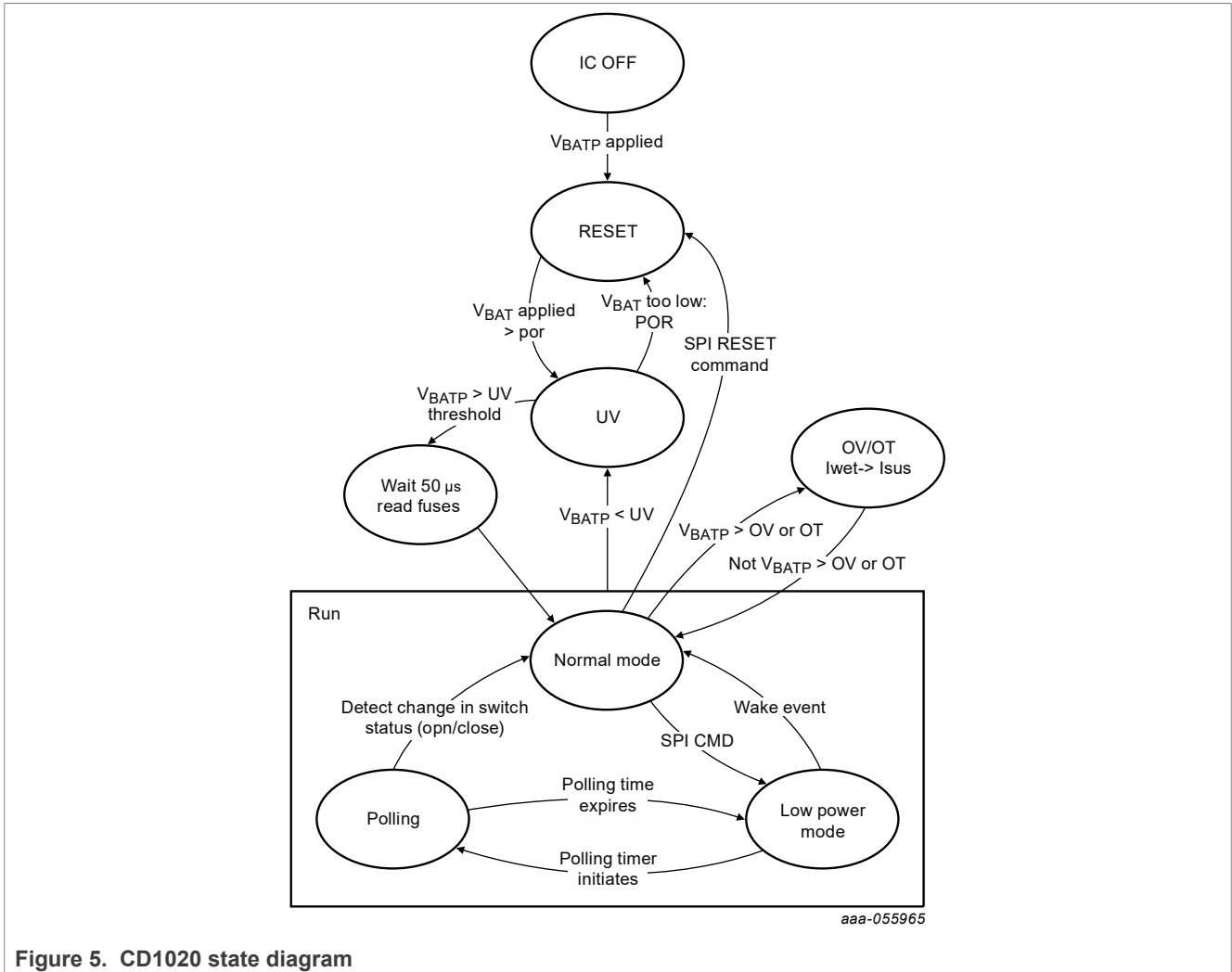
After power up, it is possible that the V_{DDQ} may turn off or be lost. In this case, the chip remains in the current state but is not able to communicate. After the V_{DDQ} pin is available again, the chip is ready to communicate.

7.2.4 V_{DDQ} okay, V_{BATP} lost

After power up, the V_{BATP} supply could be lost. The operation is consistent as when V_{DDQ} is available before V_{BATP} .

8 Functional block description

8.1 State diagram



8.1.1 State machine

After power up, the IC enters into the device state machine, as illustrated in Figure 11. The voltage on VBATP begins to power the internal oscillators and regulator supplies. The POR is based on the internal 2.5 V digital core rail. When the internal logic regulator reaches approximately 1.8 V (typically 3.3 V on the VBATP node), the IC enters into the UV range. Below the POR threshold, the IC is in RESET mode where no activity occurs.

8.1.2 UV: undervoltage lockout

After the POR circuit has reset the logic, the IC is in undervoltage. In this state, the IC remembers all register conditions, but is in a lockout mode, where no SPI communication is allowed. The AMUX is inactive and the current sources are off. The user does not receive a valid response from the MISO, as it is disabled in this state. The chip oscillators (4.0 MHz for most normal mode activities, 192 kHz for LPM, and limited normal mode functions) are turned on in the UV state. The chip moves to the Read fuses state when the VBATP voltage rises

above the UV threshold (~4.3 V rising). The internal fuses read in approximately 50 μ s and the chip enters the normal mode.

8.1.3 Normal mode

In normal mode, the chip operates as selected in the available registers. Any command may be loaded in normal mode, although not all (low-power mode) registers are used in the normal mode. All the LPM registers must be programmed in Normal mode as the SPI is not active in LPM. The normal mode of the chip is used to:

- Operate the AMUX
- Communicate via the SPI
- Interrupt the IC, wetting and sustain currents, and the thresholds available to use

The WAKE_B pin is asserted (low) in normal mode and can be used to enable a power supply (ENABLE_B). Various fault detections are available in this mode including overvoltage, overtemperature, thermal warning, SPI errors, and Hash faults.

8.1.4 Low-power mode

When the user needs to lower the IC current consumption, a low-power mode is used. The only method to enter LPM is through a SPI word. After the chip is in low-power mode, the majority of circuitry is turned off including most power rails, the 4.0 MHz oscillator, and all the fault detection circuits. This mode is the lowest current consumption mode on the chip. If a fault occurs while the chip is in this mode, the chip does not see or register the fault (does not report via the SPI when awakened). Some items may wake the IC in this mode, including the interrupt timer, falling edge of INT_B, CS_B, or WAKE_B (configurable), or a comparator-only mode switch detection.

8.1.5 Polling mode

The CD1020 uses a polling mode that periodically (selectable in LPM config register) interrogates the input pins to determine in what state the pins are, and decides if there was a change of state from when the chip was in normal mode. There are various configurations for this mode, which allow the user greater flexibility in operation. This mode uses the current sources to pull up (SG) or pull down (SB) to determine if a switch is open or closed. More information is available in section [7.2, "Low-power mode operation"](#).

In the case of a low V_{BATP} , the polling pauses and waits until the V_{BATP} rises out of UV or a POR occurs. The pause of the polling ensures all of the internal rails, currents, and thresholds are up at the required levels to accurately detect open or closed switches. The chip does not wake-up in this condition and simply waits for the V_{BATP} voltage to rise or cause a POR.

After the polling ends, the chip either returns to the low-power mode, or enters normal mode when a wake event is detected. Other events may wake the chip as well, such as the falling edge of CS_B, INT_B, or WAKE_B (configurable). A comparator only mode switch detection is always on in LPM or Polling mode, therefore, a change of state for those inputs would effectively wake the IC in Polling mode as well.

If the Wake-up enable bits are disabled on all channels (SG and SP), the device will not wake up with a change of state on any of the input pins. In this case, the device will disable the polling timer to allow the lowest current consumption during low-power mode.

8.2 Low-power mode operation

Low-power mode (LPM) is used to reduce system quiescent currents. LPM may be entered only by sending the Enter Low-power mode command. All register settings programmed in normal mode are maintained while in LPM.

The CD1020 exits LPM and enter normal mode when any of the following events occur:

- Input switch change of state (when enabled)
- Falling edge of WAKE_B (as set by the device configuration register)
- Falling edge of INT_B (with $V_{DDQ} = 5.0\text{ V}$)
- Falling edge of CS_B (with $V_{DDQ} = 5.0\text{ V}$)
- Power-On-Reset (POR)

The V_{DDQ} supply may be removed from the device during LPM, however removing V_{DDQ} from the device disables a wake-up from falling edge of INT_B and CS_B. The IC checks the status of V_{DDQ} after a falling edge of WAKE_B (as selected in the device configuration register), INT_B and CS_B. The IC returns to LPM and does not report a Wake event, if V_{DDQ} is low. If the V_{DDQ} is high, the IC wakes up and reports the Wake event. In cases where CS_B is used to wake the device, the first MISO data message is not valid.

The LPM command contains setting of the polling timer, as shown in [Table 23](#). The polling timer is used periodically to poll the inputs during low-power mode to check for change of states. The $t_{ACTIVEPOLL}$ time is the length of time the part is active during the polling timer to check for change of state. The low-power mode voltage threshold allows the user to determine the noise immunity versus lower current levels that polling allows. [Figure 13](#) shows the polling operation.

When an input is determined to meet the condition Open (when entering LPM), yet while Open (on polling event) the chip does not continue the polling event for that input(s) to lower current in the chip ([Figure 12](#) shows SG, SB is logically the same).

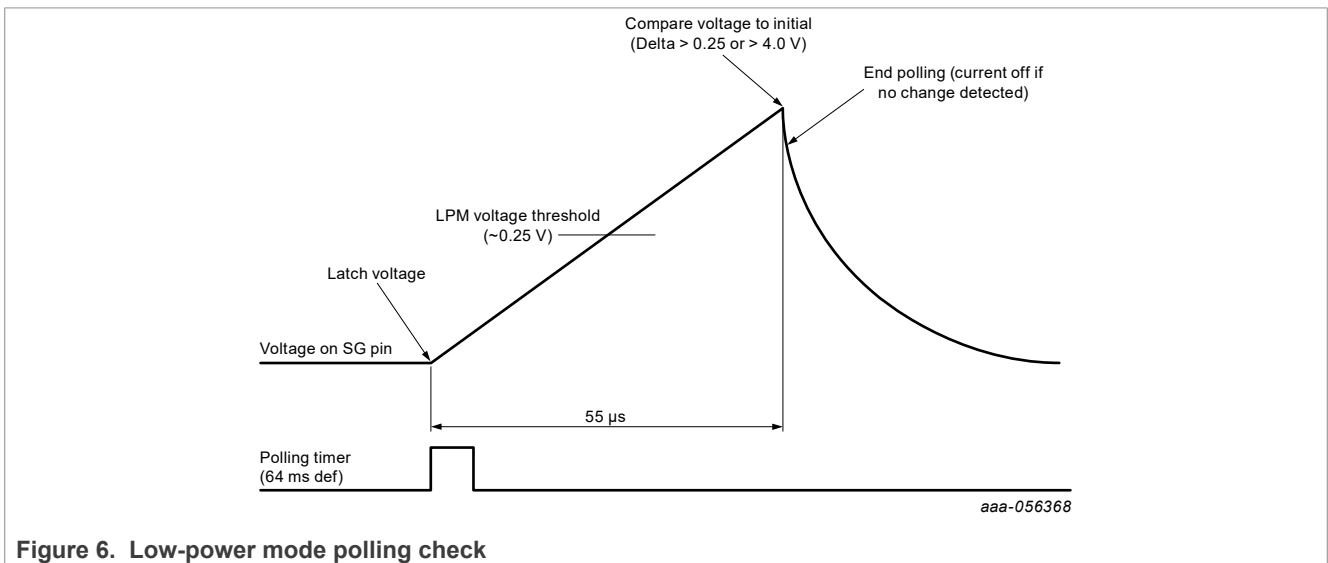


Figure 6. Low-power mode polling check

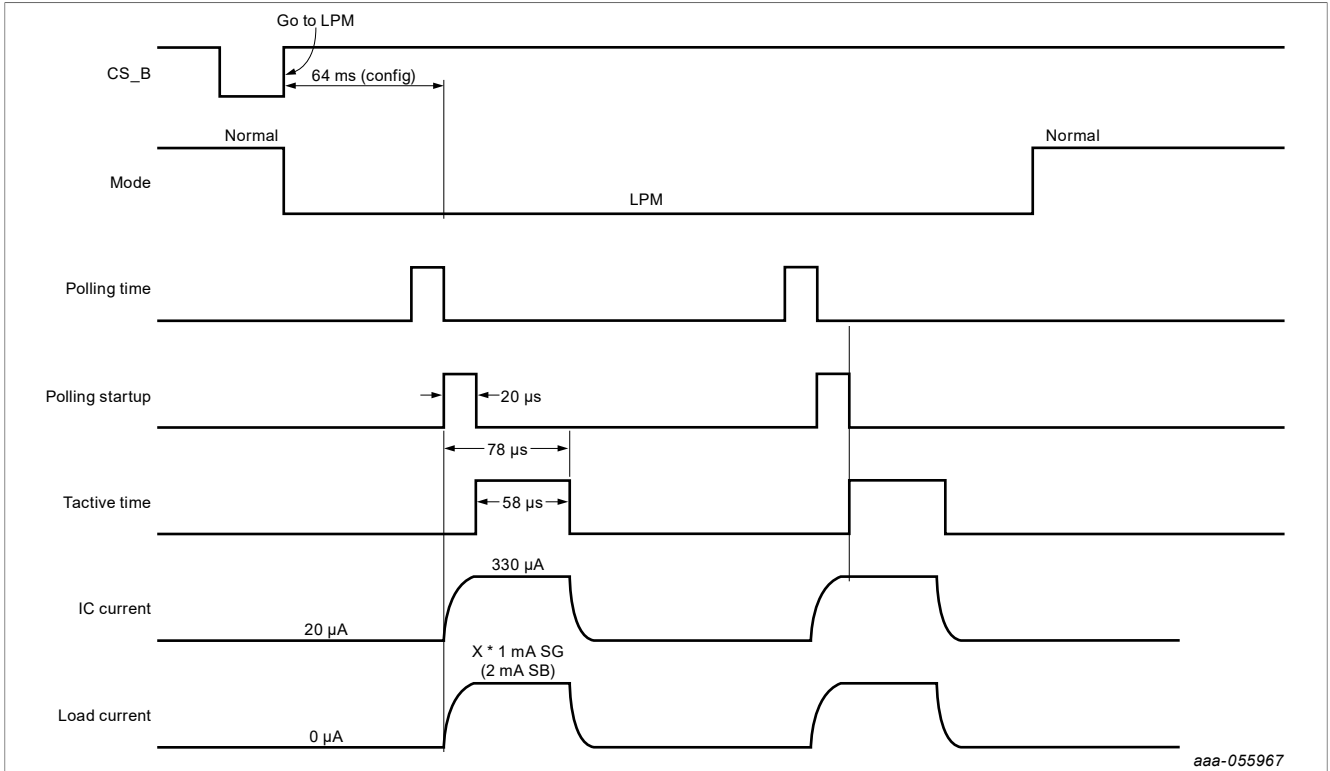


Figure 7. Low-power mode typical timing

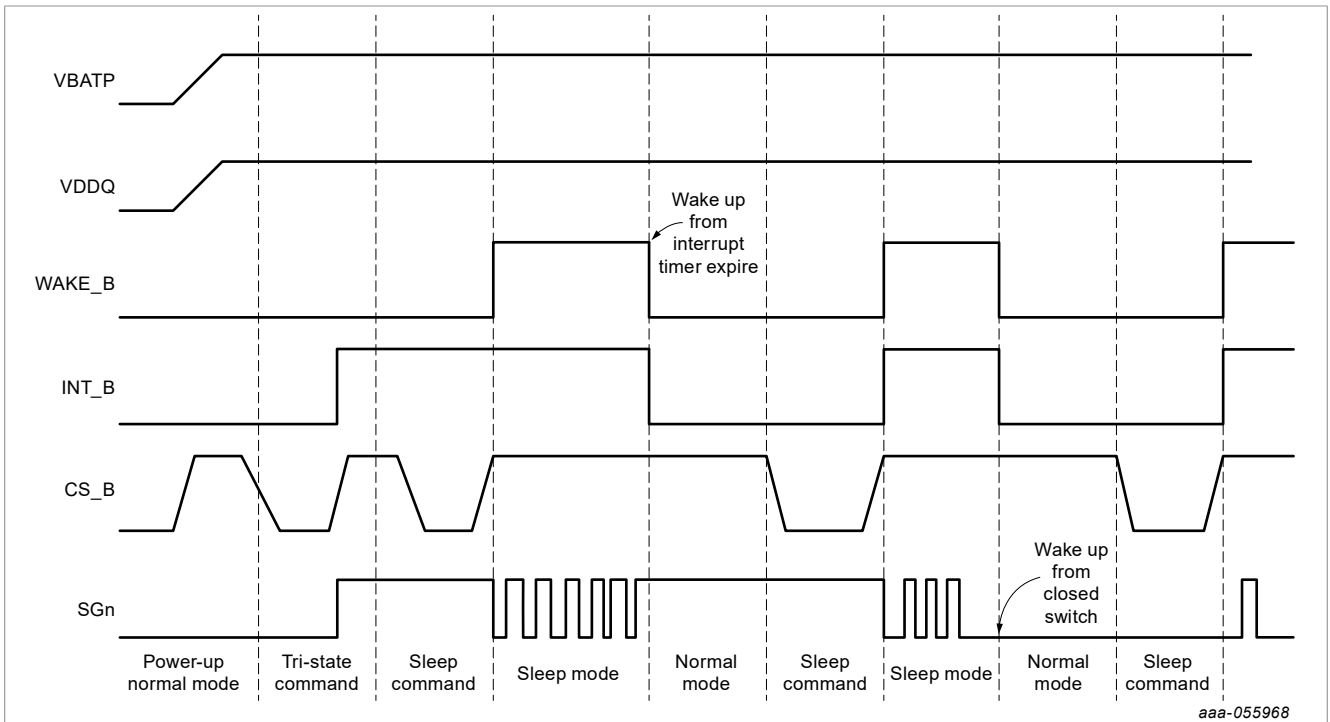


Figure 8. Low-power mode to normal mode operation

8.3 Input functional block

The SGx pins are switch-to-ground inputs only (pull-up current sources).

The SPx pins are configurable as either switch-to-ground or switch-to-battery (pull-up and pull-down current sources).

The input is compared with a 4.0 V (input comparator threshold configurable) reference. Voltages greater than the input comparator threshold value are considered open for SG pins and closed for SB configuration.

Voltages less than the input comparator threshold value are considered closed for SG pins and open for the SB configurations.

Programming features are defined in the [SPI control register definition](#) section of this data sheet.

The input comparator has hysteresis with the thresholds based on the closing of the switch (falling on SG, rising on SB).

The user must take care to keep power conditions within acceptable limits (package is capable of 2.0 W). Using many of the inputs with continuous wetting current levels causes overheating of the IC and may cause an overtemperature (OT) event to occur.

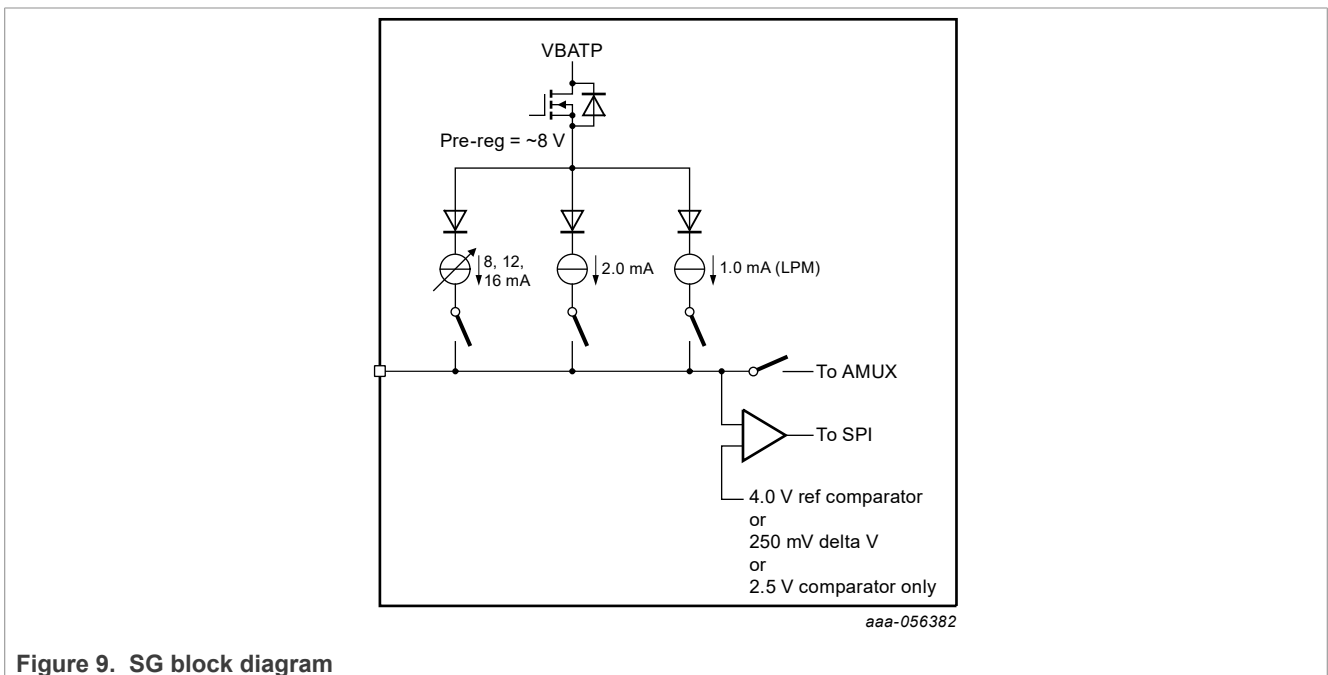


Figure 9. SG block diagram

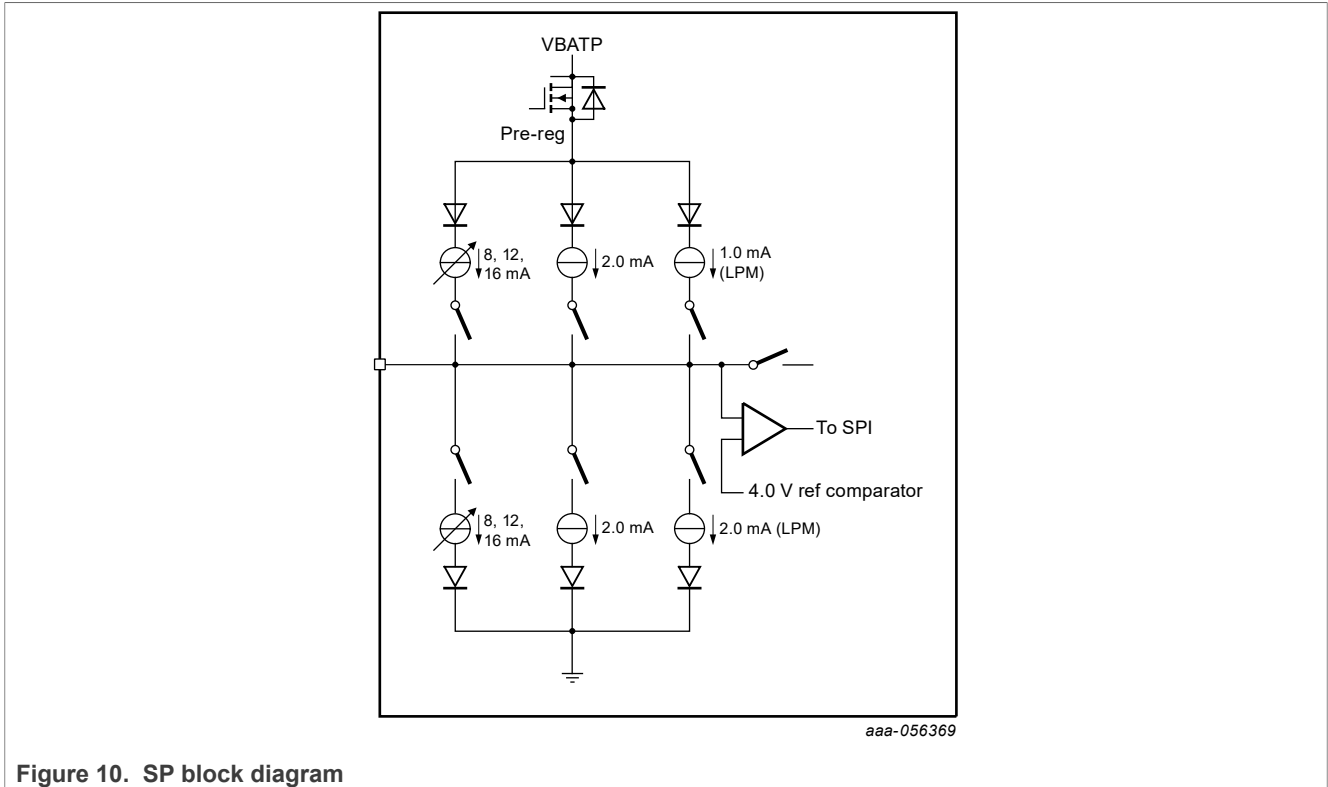


Figure 10. SP block diagram

8.4 Oscillator and timer control functional block

Two oscillators are generated in this block. A 4.0 MHz clock is used in normal mode only, as well as a low-power mode 192 kHz clock, which is on all the time. All timers are generated from these oscillators. The oscillator accuracy is 15 % for both, the 4.0 MHz clock and the 192 kHz clock. No calibration is needed and the accuracy is over voltage and temperature.

8.5 Temperature monitor and control functional block

The device has multiple thermal limit (t_{LIM}) cells to detect thermal excursions in excess of 155 °C. The t_{LIM} cells from various locations on the IC are logically ORed together and communicated to the MCU as one t_{LIM} fault. When the t_{LIM} value is seen, the wetting current is lowered to 2.0 mA until the temperature has decreased beyond the $t_{LIM(HYS)}$ value (the sustain current remains on or as selected). A hysteresis value of 15 °C exists to keep the device from cycling.

A thermal flag also exists to alert the system to increasing temperatures more than approximately 120 °C.

8.6 WAKE_B control functional block

The WAKE_B pin can operate as an open-drain output or a wake-up input. In the normal mode, the WAKE_B pin is LOW. In the low-power mode, the WAKE_B pin is pulled HIGH. The WAKE_B pin has an internal pull-up to VDDQ supply with an internal series diode to allow an external pull-up to VBATP if required.

As an input, in low-power mode with the WAKE_B pin pulled HIGH, when commanded LOW by MCU, the falling edge of WAKE_B places the CD1020 in normal mode. In low-power mode if VDDQ goes low, the WAKE_B pin can still wake the device based on the status of the WAKE_B bit in the device configuration register, this allows the user to pull the WAKE_B pin up to VBATP such that it can be used in VDDQ off setup.

As an output, WAKE_B pin can drive either an MCU input or the EnableB of a regulator (possibly for V_{DDQ}). WAKE_B is driven low during normal mode regardless of the state of V_{DDQ} . When the CD1020 is in LPM, the WAKE_B pin is released and is expected to be pulled up internally to V_{DDQ} or externally to V_{BATP} . When a valid wake-up event is detected, the CD1020 wakes up from LPM and the WAKE_B is driven Low (regardless of the state of V_{DDQ}).

8.7 INT_B functional block

INT_B is an input/output pin in the CD1020 device to indicate an interrupt event has occurred, as well as receiving interrupts from other devices when the INT_B pins are wired ORed. The INT_B pin is an open-drain output with an internal pull-up to V_{DDQ} . In normal mode, a switch state change triggers the INT_B pin (when enabled). The INT_B pin and INT_B bit in the SPI register are latched on the falling edge of CS_B. This permits the MCU to determine the origin of the interrupt. When two CD1020 devices are used, only the device initiating the interrupt has the INT_B bit set. The INT_B pin and INTflg bit are cleared 1.0 μ s after the falling edge of CS_B. The INT_B pin does not clear with the rising edge of CS_B if a switch contact change has occurred while CS_B was Low.

In a multiple CD1020 device system with WAKE_B High and V_{DDQ} on (low-power mode), the falling edge of INT_B places the device in normal mode. The INT_B has the option of a pulsed output (pulsed low for INT_{pulse} duration) or a latched low output. The default case is the latched low operation; the pulsed option is selectable via the SPI.

An INT_B request by the MCU can be done by a SPI word and results in an INT_{PULSE} of 100 μ s duration on the INT_B pin.

The chip causes an INT_B assertion for the following cases:

- A change of state is detected
- Any Wake-up event
- Any faults detected
- After a POR, the INT_B pin states asserted during startup until the chip is ready to communicate

8.8 AMUX functional block

The analog voltage-on-switch inputs may be read by the MCU using the analog command. See [Table 36](#). Internal to the IC is a 22-to-1 analog multiplexer. The voltage present on the selected input pin is buffered and made available on the AMUX output pin. The output pin is clamped to a maximum of V_{DDQ} , regardless of the higher voltages present on the input pin. After an input has been selected as the analog, the corresponding bit in the next MISO data stream is logic [0]. When selecting a channel to be read as analog input, the user can also set the current level allowed in the AMUX output. Current level can be set to the programmed wetting current for the selected channel or set to high impedance as defined in [Table 35](#).

When selecting an input to be sent to the AMUX output, that input is not polled or a wake-up enabled input from low-power mode. The user should set the AMUX to 'No input selected' before entering low-power mode. The AMUX pin is not active during low-power mode.

8.9 Serial peripheral interface (SPI)

The CD1020 contains a serial peripheral interface consisting of Serial Clock (SCLK), Serial Data Out (MISO), Serial Data In (MOSI), and Chip Select Bar (CS_B). The SPI interface is used to provide configuration, control, and status functions; the user may read the registers' contents as well as read some status bits of the IC. This device is configured as a SPI secondary device.

All SPI transmissions to the CD1020 must be done in exact increments of 32 bits (modulo 0 is ignored as well). The CD1020 contains a data valid method via SCLK input to keep non-modulo 32-bit transmissions from being

written into the IC. The SPI module also provides a daisy chain capability to accommodate MOSI to MISO wrap around (see [Figure 20](#)).

The SPI registers have a hashing technique to ensure that the registers are consistent with the programmed values. If the hashed value does not match the register status, a SPI bit is set as well as an interrupt to alert the MCU to this issue.

8.9.1 Chip select low (CS_B)

The CS_B input selects this device for serial transfers. On the falling edge of CS_B, the MISO pin is released from tri-state mode, and all status information are latched in the SPI shift register. While CS_B is asserted, register data is shifted in the MOSI pin and shifted out the MISO pin on each subsequent SCLK. On the rising edge of CS_B, the MISO pin is tri-stated and the fault register reloaded (latched) with the current filtered status data. To allow sufficient time to reload the fault registers, the CS_B pin must remain low for a minimum of t_{CSN} prior to going high again.

The CS_B input contains a pull-up current source to VDDQ to command the de-asserted state should an open-circuit condition occur. This pin has threshold compatible voltages allowing proper operation with microprocessors using a 3.3 V to 5.0 V supply.

8.9.2 Serial clock (SCLK)

The SCLK input is the clock signal input for synchronization of serial data transfer. This pin has threshold-compatible voltages allowing proper operation with microprocessors using a 3.3 V to 5.0 V supply.

When CS_B is asserted, both the Primary Microprocessor and this device latch input data on the rising edge of SCLK. The SPI primary device typically shifts data out on the falling edge of SCLK, while this device shifts data out on the rising edge of SCLK, to allow more time to drive the MISO pin to the proper level.

This input is used as the input for the modulo 32-bit counter validation. Any SPI transmissions which are NOT exact multiples of 32 bits (i.e. clock edges) is treated as an illegal transmission. The entire frame is aborted and no information is changed in the configuration or control registers.

8.9.3 Serial data output (MISO)

The MISO output pin is in a tri-state condition when CS_B is negated. When CS_B is asserted, MISO is driven to the state of the MSB of the internal register and start shifting out the requested data from the MSB to the LSB. This pin supplies a 'rail to rail' output, depending on the voltage at the VDDQ pin.

8.9.4 Serial data input (MOSI)

The MOSI input takes data from the primary microprocessor while CS_B is asserted. The MSB is the first bit of each word received on MOSI and the LSB is the last bit of each word received on MOSI. This pin has threshold-level compatible input voltages allowing proper operation with microprocessors using a 3.3 V to 5.0 V (V_{DDQ}) supply.

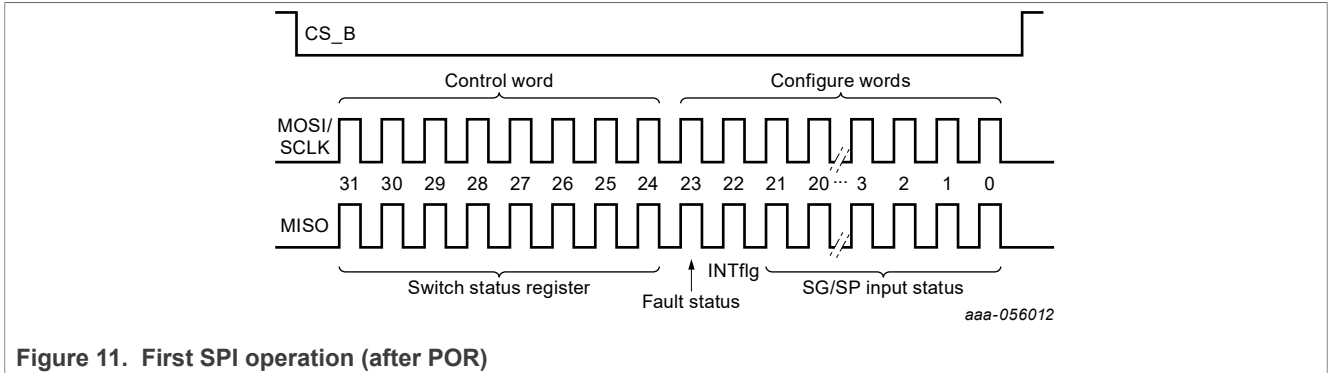


Figure 11. First SPI operation (after POR)

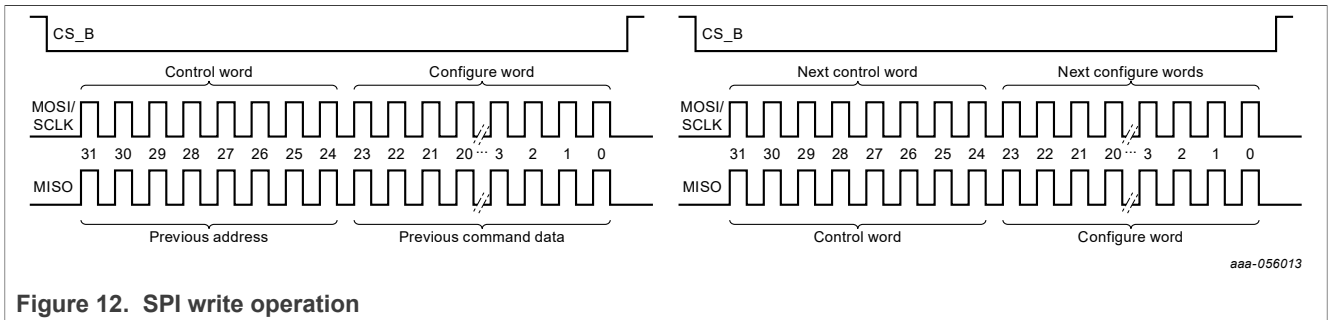


Figure 12. SPI write operation

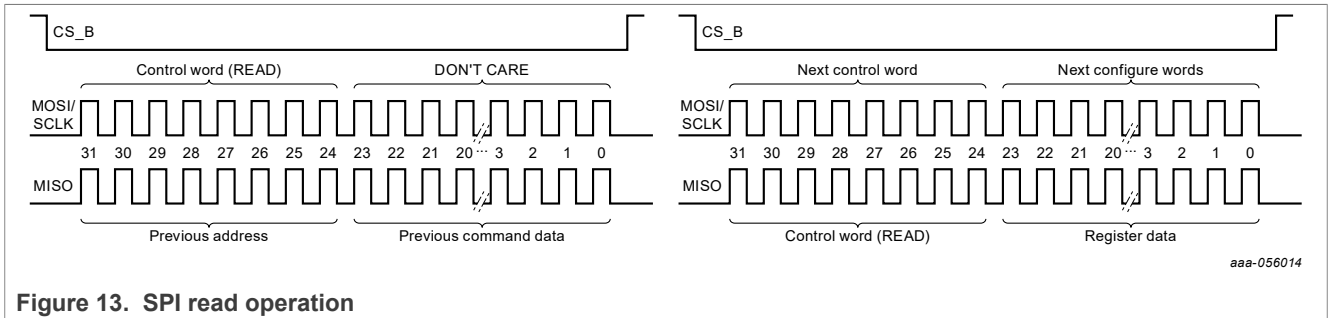
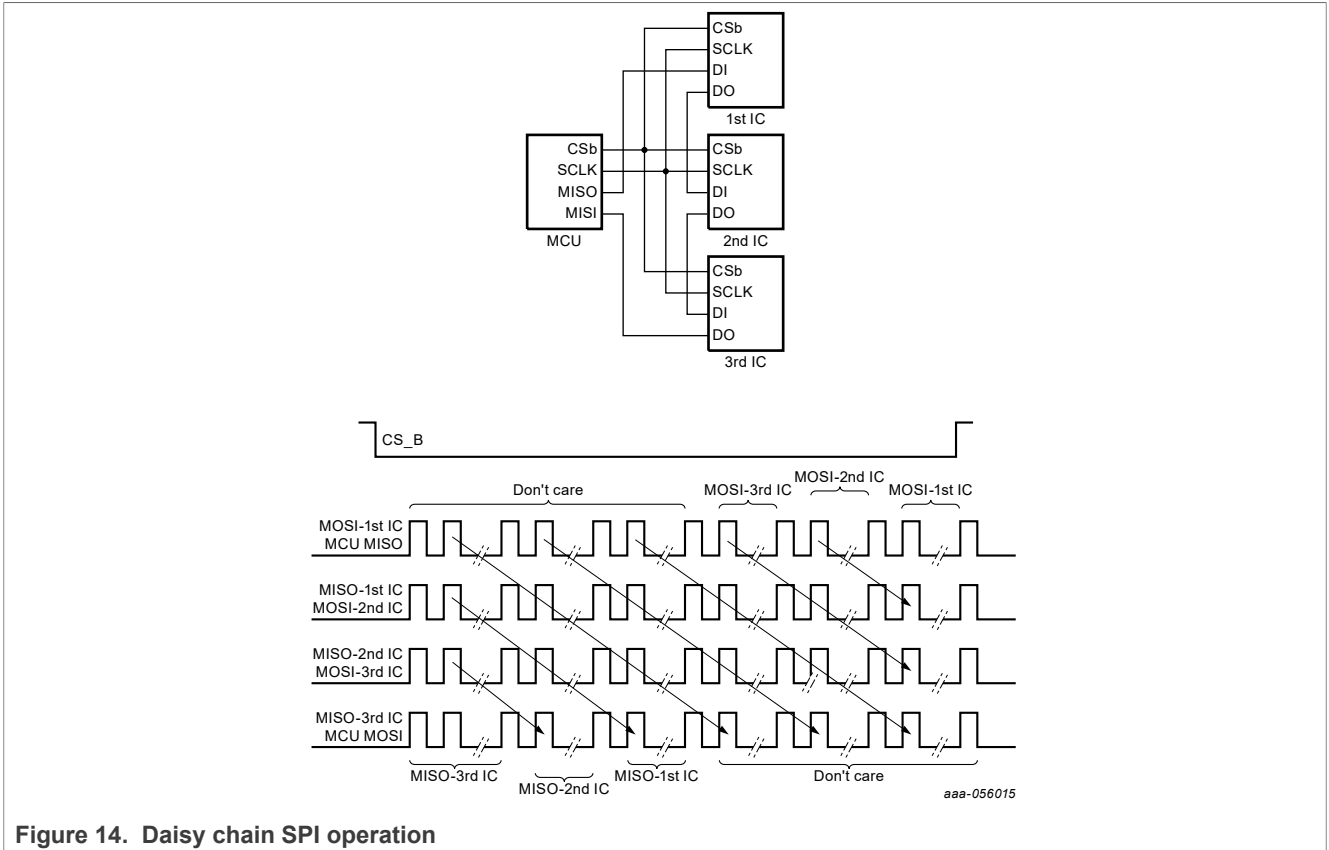


Figure 13. SPI read operation



8.10 SPI control register definition

A 32-bit SPI allows the system microprocessor to configure the CD1020 for each input as well as read out the status of each input. The SPI also allows the Fault Status and INTflg bits to be read via the SPI. The SPI MOSI bit definitions are given in [Table 8](#):

Table 3. MOSI input register bit definition

Register #	Register name	Address							R/W
0	SPI check	0	0	0	0	0	0	0	0
02/03	Device configuration register	0	0	0	0	0	0	1	0/1
04/05	Tri-state SP register	0	0	0	0	0	1	0	0/1
06/07	Tri-state SG register	0	0	0	0	0	1	1	0/1
08/09	Wetting current level SP register	0	0	0	0	1	0	0	0/1
0A/0B	Wetting current level SG register 0	0	0	0	0	1	0	1	0/1
0C/0D	Wetting current level SG register 1	0	0	0	0	1	1	0	0/1
16/17	Continuous wetting current SP register	0	0	0	1	0	1	1	0/1
18/19	Continuous Wetting Current SG Register	0	0	0	1	1	0	0	0/1
1A/1B	Interrupt enable SP register	0	0	0	1	1	0	1	0/1
1C/1D	Interrupt enable SG register	0	0	0	1	1	1	0	0/1
1E/1F	Low-power mode configuration	0	0	0	1	1	1	1	0/1
20/21	Wake-up enable register SP	0	0	1	0	0	0	0	0/1
22/23	Wake-up enable register SG	0	0	1	0	0	0	1	0/1
24/25	Comparator only SP	0	0	1	0	0	1	0	0/1
26/27	Comparator only SG	0	0	1	0	0	1	1	0/1
28/29	LPM voltage threshold SP configuration	0	0	1	0	1	0	0	0/1
2A/2B	LPM voltage threshold SG configuration	0	0	1	0	1	0	1	0/1
2C/2D	Polling current SP configuration	0	0	1	0	1	1	0	0/1
2E/2F	Polling current SG configuration	0	0	1	0	1	1	1	0/1
39	Enter low-power mode	0	0	1	1	1	0	0	1
3A/3B	AMUX control register	0	0	1	1	1	0	1	0/1

Table 3. MOSI input register bit definition...continued

Register #	Register name	Address								R/W
		0	0	1	1	1	1	1	1	
3E	Read switch status	0	0	1	1	1	1	1	1	0
42	Fault status register	0	1	0	0	0	0	0	1	0
47	Interrupt request	0	1	0	0	0	1	1	1	1
49	Reset register	0	1	0	0	1	0	0	0	1

The 32-bit SPI word consists of a command word (8-bit) and three configure words (24-bit). The 8-MSB bits are the command bits that select what type of configuration is to occur. The remaining 24-bits are used to select the inputs to be configured.

- Bit 31 – 24 = Command word: Use to select what configuration is to occur (example: setting wake-up enable command)
- Bit 23 – 0 = SGN input select word: Use these bits in conjunction with the command word to determine which input is set up.

Configuration registers may be read or written to. To read the contents of a configuration register, send the register address + '0' on the LSB of the command word; the contents of the corresponding register will be shifted out of the MISO buffer in the next SPI cycle. When a Read command is sent. The answer (in the next SPI transaction) includes the Register address in the upper byte (see [Figure 19](#)).

Read example:

- Send 0x0C00_0000 Receive: 8000_0000 (for example after a POR)
- Send 0x0000_0000 Receive: 0C00_0000 (address + register data)

The first response from the device after a POR event is a Read Status register (0x3Exxxxxx where x is the status of the inputs). This is the same for exiting the low-power mode (see [Figure 17](#)).

To write into a configuration register, send the register Address + '1' on the LSB of the command word and the configuration data on the next 24 bits. The new value of the register will be shifted out of the MISO buffer in the next SPI cycle, along with the register address.

[Table 9](#) provides a general overview of the functional SPI commands and configuration bits.

Table 4. Functional SPI register map

Commands	[31-25]	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Address	R/W																								
SPI check	0000000	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Device Configuration	0000001	0/1	FS	INT	X	X	X	X	X	X	X	X	SBPOLL TIME	VBATP OV Disable	WAKE_B Pull up	IntB_ Out	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Tri-State Enable SP	0000010	0/1	FS	INT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Tri-State Enable SG	0000011	0/1	FS	INT	X	X	X	X	X	X	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Wetting Current Level SP	0000100	0/1	SP7[2-0]			SP6[2-0]			SP5[2-0]			SP4[2-0]			SP3[2-0]			SP2[2-0]			SP1[2-0]			SP0[2-0]		
Wetting Current Level SG 0	0000101	0/1	SG7[2-0]			SG6[2-0]			SG5[2-0]			SG4[2-0]			SG3[2-0]			SG2[2-0]			SG1[2-0]			SG0[2-0]		

Table 4. Functional SPI register map...continued

Wetting Current Level SG 1	0000110	0/1	FS	INT	X	X	X	X	SG13[2-0]			SG12[2-0]			SG11[2-0]			SG10[2-0]			SG9[2-0]			SG8[2-0]		
Continuous Wetting Current Enable SP	0001011	0/1	FS	INT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Continuous Wetting Current Enable SG	0001100	0/1	FS	INT	X	X	X	X	X	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0	
Interrupt Enable SP	0001101	0/1	FS	INT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Interrupt Enable SG	0001110	0/1	FS	INT	X	X	X	X	X	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0	
Low-power mode configuration	0001111	0/1	FS	INT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	poll3	poll2	poll1	poll0	
Wake-Up Enable SP	0010000	0/1	FS	INT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
Wake-Up Enable SG	0010001	0/1	FS	INT	X	X	X	X	X	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0	
LPM Comparator Only SP	0010010	0/1	FS	INT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
LPM Comparator Only SG	0010011	0/1	FS	INT	X	X	X	X	X	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0	
LPM Voltage Threshold SP	0010100	0/1	FS	INT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
LPM Voltage Threshold SG	0010101	0/1	FS	INT	X	X	X	X	X	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0	
LPM Polling current config SP	0010110	0/1	FS	INT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
LPM Polling current config SG	0010111	0/1	FS	INT	X	X	X	X	X	X	X	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0	
Enter Low-power mode	0011100	1	FS	INT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
AMUX Channel Select SPI	0011101	0/1	FS	INT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	asett	asel5	asel4	asel3	asel2	asel1	asel0
Read Switch Status	0011111	0	FAULT STATUS	INTflg	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
Fault Status	0100001	0	X	INTflg	X	X	X	X	X	X	X	X	X	X	SPI Error	hash fault	X	UV	OV	Temp Flag	OT	INT_B wake	WAKE_B	SpiWake	POR	
Interrupt Pulse Request	0100011	1	FS	INT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	
Reset	0100100	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	

Notes
 24. FS = FAULT STATUS (available for reading on MISO return word)
 25. INT = INTflg (available for reading on MISO return word)

8.10.1 SPI check

The MCU may check the communication with the IC by using the SPI Check register. The MCU sends the command, and the response during the next SPI transaction will be 0x123456. The SPI Check command does not return Fault Status or INTflg bit, thus interrupts will not be cleared.

Table 5. SPI check command

Register address	R	SPI data bits [23 – 0]
[31–25]	[24]	bits [23 – 16]
0000_000	0	0000_0000
		bits [15 – 8]
		0000_0000
		bits [7 – 0]
		0000_0000
MISO return word		0x00123456

8.10.2 Device configuration register

The device has various configuration settings that are global in nature. The configuration settings are as follows:

- When the CD1020 is in the overvoltage region, a Logic [0] on the VBATP OV bit limits the wetting current on all input channels to 2 mA, and the CD1020 will not be able to enter into the low-power mode. A Logic [1] allows the device to operate normally even in the overvoltage region. The OV flag will be set when the device enters in the OV region, regardless of the value of the VBATP OV bit.
- WAKE_B can be used to enable an external power supply regulator to supply the VDDQ voltage rail. When the WAKE_B VDDQ check bit is a Logic [0], the WAKE_B pin is expected to be pulled up internally or externally to VDDQ and VDDQ is expected to go low, therefore, the CD1020 does not wake up on the falling edge of WAKE_B. A Logic [1], assumes the user is using an external pull-up to V_{BATP} or V_{DDQ} (when V_{DDQ} is not expected to be off) and the IC wakes up on a falling edge of WAKE_B.
- INT_B out is used to select how the INT_B pin operates when an interrupt occurs. The IC is able to pulse low [1] or latch low [0].
- Inputs SP0-7 may be programmable for switch-to-battery or switch-to-ground. These input types are defined using the settings command. To set a SPn input for switch-to-battery, a logic [1] for the appropriate bit must be set. To set a SPn input for switch-to-ground, a logic [0] for the appropriate bit must be set. The MCU may change or update the programmable switch register via software at any time in normal mode. Regardless of the setting, when the SPn input switch is closed a logic [1] is placed in the serial output response register.

Table 6. Device configuration register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0000_001	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused		SBPOLL TIME	VBATP OV disable	WAKE_B VDDQ Check	INT_B out	Unused	Unused
		0	0	0	0	1	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		1	1	1	1	1	1	1	1
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0000_001[R/W]		FAULT STATUS	INTflg	Register Data					

Table 7. Device configuration bits definition

Bit	Functions	Default value	Description
23–14	Unused	0	Unused
13	SBPOLLTIME	0	Select the polling time for SP channels configured as SB. • A logic [0] set the active polling timer to 1ms, • A logic [1] sets the active polling timer to 55 μ s.
12	VBATP OV Disable	0	VBATP Overvoltage protection • 0 – Enabled • 1 – Disable
11	WAKE_B VDDQ Check	1	Enable/Disable WAKE_B to wake-up the device on falling edge when V _{DDQ} is not present. • 0 – WAKE_B is pulled up to V _{DDQ} (internally and/or externally). WAKE_B is ignored while in LPM if V _{DDQ} is low. • 1 – WAKE_B is externally pulled up to V _{BATP} or V _{DDQ} and wakes upon a falling edge of the WAKE_B pin regardless of the V _{DDQ} status. (V _{DDQ} is not expected to go low)
10	Int_B_Out	0	Interrupt pin behavior • 0 – INT pin stays low when interrupt occurs • 1 – INT pin pulse low and return high
9–8	Unused	00	Unused
7–0	SP7 – SP0	1111_1111	Configure the SP pin as Switch to Battery (SB) or Switch to ground (SG) • 0 – Switch to Ground • 1 – Switch to Battery

8.10.3 Tri-state SP register

The tri-state command is use to set the input nodes as high-impedance ([Table 13](#)). By setting the tri-state register bit to logic [1], the input is high-impedance regardless of the Wetting current setting. The configurable comparator (4.0 V default) on each input remains active. The MCU may change or update the tri-state register via software at any time in normal mode. The tri-state register defaults to 1 (inputs are tri-stated). Any inputs in tristate are still polled in LPM, but the current source is not active during this time. The determination of change of state occurs at the end of the t_{ACTIVEPOLL} and the wake-up decision is made.

Table 8. Tri-state SP register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0000_010	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused							
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		1	1	1	1	1	1	1	1
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0000_010[R/W]		FAULT STATUS	INTflg	Register Data					

8.10.4 Tri-state SG register

The tri-state command is used to set the input nodes as high-impedance ([Table 14](#)). By setting the tri-state register bit to logic [1], the input is high-impedance regardless of the Wetting command setting. The configurable comparator (4.0 V default) on each input remains active. The MCU may change or update the tri-state register via software at any time in normal mode. The tri-state register defaults to 1 (inputs are tristated. Any inputs in tri-state are still polled in LPM but the current source is not active during this time. The determination of change of state occurs at the end of the t_{ACTIVEPOLL} and the wake-up decision is made.

Table 9. Tri-state SG register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0000_011	0/1	Unused							

Table 9. Tri-state SG register...continued

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused		SG13	SG12	SG11	SG10	SG9	SG8
		0	0	1	1	1	1	1	1
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
	1	1	1	1	1	1	1	1	
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0000_011[R/W]		FAULT STATUS	INTflg	Register Data					

8.10.5 Wetting current level SP register

The IC contains configurable wetting currents (Default = 16 mA). Three bits are used to control each individual input pin with the values set in Table 15. The MCU may change or update the wetting current register via software at any time in normal mode.

Table 10. Wetting current level SP register

Register address	R/W	SPI data bits [23 – 0]					
[31–25]	[24]	bit [23 – 21]		bit [20 – 18]		bit [17 – 16]	
0000_100	0/1	SP7 [2–0]		SP6[2–0]		SP5[2–1]	
Default on POR		110		110		11	
		bit [15]	bit [14 – 12]		bit [11 – 9]		bit [8]
		SP5[0]	SP4 [2–0]		SP3[2–0]		SP2[2]
		0	110		110		1
		bit [7 – 6]		bit [5 – 3]		bit [2 – 0]	
		SP2[1–0]		SP1[2–0]		SP0[2–0]	
		10		110		110	
MISO return word		bits [23 – 0]					
0000_100[R/W]		Register Data					

See Table 18 for the selectable Wetting Current level values for both SPx and SGx pins.

8.10.6 Wetting current level SG register 0

The IC contains configurable wetting currents (Default = 16 mA). Three bits are used to control each individual input pin with the values set in Table 16. The MCU may change or update the wetting current register via software at any time in normal mode.

Table 11. Wetting current level SG register 0

Register address	R/W	SPI data bits [23 – 0]					
[31–25]	[24]	bit [23 – 21]		bit [20 – 18]		bit [17 – 16]	
0000_101	0/1	SG7 [2–0]		SG6[2–0]		SG5[2–1]	
Default on POR		110		110		11	
		bit [15]	bit [14 – 12]		bit [11 – 9]		bit [8]
		SG5[0]	SG4 [2–0]		SG3[2–0]		SG2[2]
		0	110		110		1
		bit [7 – 6]		bit [5 – 3]		bit [2 – 0]	
		SG2[1–0]		SG1[2–0]		SG0[2–0]	
		10		110		110	
MISO return word		bits [23 – 0]					
0000_101[R/W]		Register Data					

See [Table 18](#) for the selectable Wetting Current level values for both SPx and SGx pins.

8.10.7 Wetting current level SG register 1

The IC contains configurable wetting currents (Default = 16 mA). Three bits are used to control each individual input pin with the values set in [Table 17](#). The MCU may change or update the wetting current register via software at any time in normal mode.

Table 12. Wetting current level SG register 1

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit [23 – 21]			bit [20 – 18]			bit [17 – 16]	
0000_110	0/1	Unused						SG13[2–1]	
		0						11	
Default on POR		bit [15]	bit [14 – 12]			bit [11 – 9]			bit [8]
		SG13[0]	SG12 [2–0]			SG11[2–0]			SG10[2]
		0	110			110			1
		bit [7 – 6]		bit [5 – 3]			bit [2 – 0]		
		SG10[1–0]		SG9[2–0]			SG8[2–0]		
		10		110			110		
MISO return word		bits [23 – 0]							
0000_110[R/W]		Register Data							

See [Table 18](#) for the selectable Wetting Current level values for both SPx and SGx pins.

Table 13. SPx/SGx selectable wetting current levels

SPx/SGx[2–1]			Wetting current level
bit 2	bit 1		
0	0		2.0 mA
0	1		8.0 mA
1	0		12 mA
1	1		16 mA
Notes			
26. bit 0 is 0			

8.10.8 Continuous wetting current SP register

Each switch input has a designated 20 ms timer. The timer starts when the specific switch input crosses the comparator threshold. When the 20 ms timer expires, the contact current is reduced from the configured wetting current (16 mA) to the Sustain current. The wetting current is defined to be an elevated level that reduces to the lower sustain current level after the timer has expired. With multiple wetting current timers disabled, power dissipation for the IC must be considered.

The MCU may change or update the continuous wetting current register via software at any time in normal mode. This allows the MCU to control the amount of time wetting current is applied to the switch contact. Programming the continuous wetting current bit to logic [0] operates normally with a higher wetting current followed by sustain current after 20 ms (pulsed Wetting current operation). Programming to logic [1] enables the continuous wetting current ([Table 19](#)) and results in a full time wetting current level. The continuous wetting current register defaults to 0 (pulse wetting current operation).

Table 14. Continuous wetting current SP register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0001_011	0/1	Unused							

Table 14. Continuous wetting current SP register...continued

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused							
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		0	0	0	0	0	0	0	0
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0001_011[R/W]		FAULT STATUS	INTflg	Register Data					

8.10.9 Continuous Wetting Current SG Register

Each switch input has a designated 20 ms timer. The timer starts when the specific switch input crosses the comparator threshold. When the 20 ms timer expires, the contact current is reduced from the configured wetting current (16 mA) to 2.0 mA. The wetting current is defined to be at an elevated level that reduces to the lower sustain current level after the timer has expired. With multiple wetting current timers disabled, power dissipation for the IC must be considered.

The MCU may change or update the continuous wetting current register via software at any time in normal mode. This allows the MCU to control the amount of time wetting current is applied to the switch contact. Programming the continuous wetting current bit to logic [0] operates normally with a higher wetting current followed by sustain current after 20 ms (Pulse wetting current operation). Programming to logic [1] enables the continuous wetting current (Table 20) and results in a full-time-wetting current level. The continuous wetting current register defaults to 0 (pulse wetting current operation).

Table 15. Continuous wetting current SG register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0001_100	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused		SG13	SG12	SG11	SG10	SG9	SG8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		0	0	0	0	0	0	0	0
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0001_100[R/W]		FAULT STATUS	INTflg	Register Data					

Register address	R/W	SPI data bits [23-0]							
[31-25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0001_100	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused		SG13	SG12	SG11	SG10	SG9	SG8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		0	0	0	0	0	0	0	0
MISO return word		bit [23]	bit [22]	bits [21-0]					
0001_100[R/W]		FAULT STATUS	INTflg	Register data					

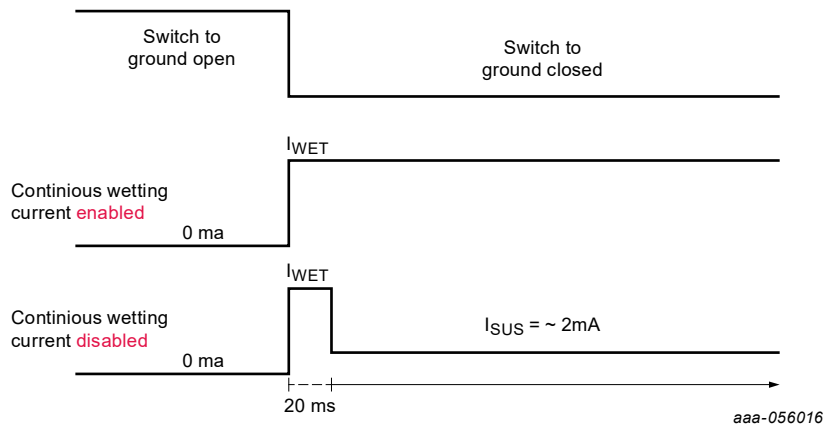


Figure 15. Pulsed/continuous wetting current configuration

8.10.10 Interrupt enable SP register

The interrupt register defines the inputs that are allowed to Interrupt the CD1020 normal mode. Programming the interrupt bit to logic [0] disables the specific input from generating an interrupt. Programming the interrupt bit to logic [1] enables the specific input to generate an interrupt with switch change of state. The MCU may change or update the interrupt register via software at any time in normal mode. The Interrupt register defaults to logic [1] (Interrupt enabled).

Table 16. Interrupt enable SP register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0001_101	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused							
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		1	1	1	1	1	1	1	1
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0001_101[R/W]		FAULT STATUS	INTflg	Register Data					

8.10.11 Interrupt enable SG register

The interrupt register defines the inputs that are allowed to Interrupt the CD1020 normal mode. Programming the interrupt bit to logic [0] disables the specific input from generating an interrupt. Programming the interrupt bit to logic [1] enables the specific input to generate an interrupt with switch change of state The MCU may change or update the interrupt register via software at any time in normal mode. The Interrupt register defaults to logic [1] (Interrupt enabled).

Table 17. Interrupt enable SG register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0001_110	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused		SG13	SG12	SG11	SG10	SG9	SG8
		0	0	1	1	1	1	1	1
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		1	1	1	1	1	1	1	1
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0001_110[R/W]		FAULT STATUS	INTflg	Register Data					

8.10.12 Low-power mode configuration

The device has poll[3-0] to set the normal polling rate for the IC. The polling rate is the time between polling events. The current sources become active at this time for a time of t_{ACTIVESGPOLLING} or t_{ACTIVESBPOLLING} for SG or SB channels respectively.

Table 18. Low-power mode configuration register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0001_111	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused							
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		Unused				poll3	poll2	poll1	poll0
		0	0	0	0	1	1	1	1
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0001_111[R/W]		FAULT STATUS	INTflg	Register Data					

Table 19. Low-power mode configuration bits definition

Bit	Functions	Default value	Description
23 – 4	Unused	0	Unused
3 – 0	poll[3–0]	1111	Set the polling rate for switch detection <ul style="list-style-type: none"> • 0000 – 3.0 ms • 0001 – 6.0 ms • 0010 – 12 ms • 0011 – 24 ms • 0100 – 48 ms • 0101 – 68 ms • 0110 – 76 ms • 0111 – 128 ms • 1000 – 32 ms • 1001 – 36 ms • 1010 – 40 ms • 1011 – 44 ms • 1100 – 52 ms • 1101 – 56 ms • 1110 – 60 ms • 1111 – 64 ms (default)

8.10.13 Wake-up enable register SP

The wake-up register defines the inputs that are allowed to wake the CD1020 from low-power mode. Programming the wake-up bit to logic [0] disables the specific input from waking the IC (Table 25). Programming the wake-up bit to logic [1] enables the specific input to wake-up with switch change of state The MCU may change or update the wake-up register via software at any time in normal mode. The Wake-up register defaults to logic [1] (wake-up enabled). If all channels (SG and SB) have the Wake-up bit disabled, the device disables the polling timer to reduce the current consumption during low-power mode.

Table 20. Wake-up enable SP register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_000	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused							
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		1	1	1	1	1	1	1	1
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0010_000[R/W]		FAULT STATUS	INTflg	Register Data					

8.10.14 Wake-up enable register SG

The wake-up register defines the inputs that are allowed to wake the CD1020 from low-power mode. Programming the wake-up bit to logic [0] disables the specific input from waking the IC (Table 26). Programming the wake-up bit to logic [1] enables the specific input to wake-up with any switch change of state The MCU may change or update the wake-up register via software at any time in normal mode. The Wake-up register defaults to logic [1] (wake-up enabled). If all channels (SG and SB) have the Wake-up bit disabled, the device disables the polling timer to reduce the current consumption during low-power mode.

Table 21. Wake-up enable SG register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_001	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused		SG13	SG12	SG11	SG10	SG9	SG8
		0	0	1	1	1	1	1	1
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		1	1	1	1	1	1	1	1
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0010_001[R/W]		FAULT STATUS	INTflg	Register Data					

8.10.15 Comparator only SP

The comparator only register allows the input comparators to be active during LPM with no polling current. In this case, the inputs can receive a digital signal on the order of the LPM clock cycle and wake-up on a change of state. This register is intended to be used for signals that are driven by an external chip and drive to 5.0 V.

Table 22. Comparator only SP Register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_010	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused							
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		0	0	0	0	0	0	0	0
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0010_010[R/W]		FAULT STATUS	INTflg	Register Data					

8.10.16 Comparator only SG

The comparator only register allows the input comparators to be active during LPM with no polling current. In this case, the inputs can receive a digital signal on the order of the LPM clock cycle and wake-up on a change of state. This register is intended to be used for signals that are driven by an external chip and drive to 5.0 V.

Table 23. Comparator only SG register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_011	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused		SG13	SG12	SG11	SG10	SG9	SG8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		0	0	0	0	0	0	0	0
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0010_011[R/W]		FAULT STATUS	INTflg	Register Data					

8.10.17 LPM voltage threshold SP configuration

The CD1020 is able to use different voltage thresholds to wake-up from LPM. When configured as SG, a Logic [0] means the input will use the LPM delta voltage threshold to determine the state of the switch. A Logic [1] means the input uses the Normal threshold (VICTHR) to determine the state of the switch. When configured as an SB, it only uses the 4.0 V threshold regardless of the status of the LPM voltage threshold bit. The user must ensure that the correct current level is set to allow the crossing of the normal mode threshold (typically 4.0 V).

Table 24. LPM voltage threshold configuration SP register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_100	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused							
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
		0	0	0	0	0	0	0	0
MISO return word		bit [23]	bit [22]	bits [21 – 0]					

Table 24. LPM voltage threshold configuration SP register...continued

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_100[R/W]		FAULT STATUS	INTflg	Register Data					

8.10.18 LPM voltage threshold SG configuration

This means the input uses the LPM delta voltage threshold to determine the state of the switch. A Logic [1] means the input uses the Normal threshold to determine the state of the switch. The user must ensure that the correct current level is set to allow the crossing of the normal mode threshold (typically 4.0 V)

Table 25. LPM voltage threshold configuration SG register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_101	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused		SG13	SG12	SG11	SG10	SG9	SG8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
	0	0	0	0	0	0	0	0	
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0010_101[R/W]		FAULT STATUS	INTflg	Register Data					

8.10.19 Polling current SP configuration

The normal polling current for LPM is 2.2 mA for SB channels and 1.0 mA for SG channels, A logic [0] selects the normal polling current for each individual channel. The user may choose to select the I_{WET} current value as defined in the wetting current level registers by writing a Logic [1] on this bit; this will result in higher LPM currents but may be used in cases when a higher polling current is needed.

Table 26. Polling current configuration SP register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_110	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused							
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
	0	0	0	0	0	0	0	0	
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0010_110[R/W]		FAULT STATUS	INTflg	Register Data					

8.10.20 Polling current SG configuration

A Logic [0] selects the normal polling current for LPM =1.0 mA. The user may choose to select the I_{WET} current value as defined in the wetting current registers for LPM by writing a Logic [1] in this bit; this results in higher LPM currents but may be used in cases when a higher polling current is needed.

Table 27. Polling current configuration SG register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0010_111	0/1	Unused							
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused		SG13	SG12	SG11	SG10	SG9	SG8
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
		0	0	0	0	0	0	0	0
MISO return word		bit [23]	bit [22]	bits [21 – 0]					
0010_111[R/W]		FAULT STATUS	INTflg	Register Data					

8.10.21 Enter low-power mode

Low-power mode (LPM) is used to reduce system quiescent currents. Low-power mode may be entered only by sending the low-power command. When returning to normal mode, all register settings is maintained.

The Enter Low-power mode register is write only and has the effect of going to LPM and beginning operation as selected (polling, interrupt timer). When returning form low-power mode, the first SPI transaction will return the Fault Status and the intflg bit set to high, as well as the actual status of the Input pins.

Table 28. Enter low-power mode command

Register address	W	SPI data bits [23 – 0]							
[31–25]	[24]	bits [23 – 16]							
0011_100	1	0000_0000							
		bits [15 – 8]							
		0000_0000							
		bits [7 – 0]							
		0000_0000							
MISO return word		—							

8.10.22 AMUX control register

The analog voltage on switch inputs may be read by the MCU using the analog command (Table 34). Internal to the CD1020 is a 22---to-1 analog multiplexer. The voltage present on the selected input pin is buffered and made available on the AMUX output pin. The AMUX output pin is clamped to a maximum of V_{DDQ} volts regardless of the higher voltages present on the input pin. After an input has been selected as the analog, the corresponding bit in the next MISO data stream is logic [0].

Setting the current to wetting current (configurable) may be useful for reading sensor inputs. The MCU may change or update the analog select register via software at any time in normal mode. The analog select defaults to no input.

Table 29. Slow polling SG register

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0011_101	0/1	Unused							

Table 29. Slow polling SG register...continued

Register address	R/W	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
Default on POR		0	0	0	0	0	0	0	0
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8
		Unused							
		0	0	0	0	0	0	0	0
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
		Unused	asett0	asel[5–0]					
MISO return word		0	0	0	0	0	0	0	0
		bit [23]	bit [22]	bits [21 – 0]					
0011_101[R/W]		FAULT STATUS	INTflg	Register Data					

Table 30. AMUX current select

asett[0]	Zsource
0	hi Z (default)
1	lwET

Table 31. AMUX channel select

asel 5	asel 4	asel3	asel 2	asel 1	asel 0	Analog channel select
0	0	0	0	0	0	No Input Selected
0	0	0	0	0	1	SG0
0	0	0	0	1	0	SG1
0	0	0	0	1	1	SG2
0	0	0	1	0	0	SG3
0	0	0	1	0	1	SG4
0	0	0	1	1	0	SG5
0	0	0	1	1	1	SG6
0	0	1	0	0	0	SG7
0	0	1	0	0	1	SG8
0	0	1	0	1	0	SG9
0	0	1	0	1	1	SG10
0	0	1	1	0	0	SG11
0	0	1	1	0	1	SG12
0	0	1	1	1	0	SG13
0	0	1	1	1	1	SP0
0	1	0	0	0	0	SP1
0	1	0	0	0	1	SP2
0	1	0	0	1	0	SP3
0	1	0	0	1	1	SP4
0	1	0	1	0	0	SP5
0	1	0	1	0	1	SP6
0	1	0	1	1	0	SP7

8.10.23 Read switch status

The Read switch status register is used to determine the state of each of the inputs and is read only. All of the inputs (SGn and SPn) are returned after the next command is sent. A Logic [1] means the switch is closed while a Logic [0] is an open switch.

Included in the status register are two more bits, the Fault Status bit and intflg bit. The Fault Status bit is a combination of the extended status bits and the wetting current fault bits. If any of these bits are set, the Fault Status bit is set. The intflg bit is set when an interrupt occurs on this device.

After POR, both the Fault Status bit and the intflg bit are set high to indicate an interrupt due to a POR occurring. The intflg bit will be cleared upon reading the Read Switch Status register, and the Fault Status bit will remain high until the Fault status register is read and thus the POR fault bit and all other fault flags are cleared.

The Fault Status and Intflg bits are semi-global flags, if a fault or an interrupt occurs, these bit will be returned after writing or reading any command, except for the SPICheck and the Wetting Current configuration registers, which use those bits to set/display the device configuration.

Table 32. Read switch status command

Register address	R	SPI data bits [23 – 0]							
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16
0011_111	0	FAULT STATUS	INTflg	SP7	SP6	SP5	SP4	SP3	SP2
Default After POR	1	1	X	X	X	X	X	X	X
	bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	
	SP1	SP0	SG13	SG12	SG11	SG10	SG9	SG8	
	X	X	X	X	X	X	X	X	X
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	
	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0	
	X	X	X	X	X	X	X	X	X
MISO return word		bit [23]	bit [22]	bits [21–14]			bits [13–0]		
0011_1110		FAULT STATUS	INTflg	SP7 – SP0 Switch Status			SG13 – SG0 Switch Status		

The fault/status diagnostic capability consists of one internal 24-bit register. The content of the fault/status register is shown in [Table 38](#). Bits 0 – 21 show the status of each input where logic [1] is a closed switch and logic [0] is an open switch. In addition to input status information, fault status such as die over-temp, Hash fault, SPI errors, as well as interrupts are reported.

A SPI read cycle is initiated by a CS_B logic ‘1’ to ‘0’ transition, followed by 32 SCLK cycles to shift the fault/status registers out the MISO pin. The INT_B pin is cleared 1.0 ms after the falling edge of CS_B. The fault is immediately set again if the fault condition is still present. The Fault Status bit sets any time a Fault occurs, and the Fault register ([Table 39](#)) must be read in order to clear the Fault status flag.

The intflg bit sets anytime an interrupt event occurs (change of state on switch, any fault status bit gets set). Any SPI message that will return intflg bit will clear this flag, even if the event is still occurring. For example an overtemp, will cause an interrupt. The interrupt can be cleared but the chip will not interrupt again, based on the overtemp until that fault has gone away.

Table 33. MISO output register definition

MISO Response Sends	Fault Status	INTflg	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	SG13	SG12	SG11	SG10	SG9	SG8	SG7	SG6	SG5	SG4	SG3	SG2	SG1	SG0
---------------------	--------------	--------	-----	-----	-----	-----	-----	-----	-----	-----	------	------	------	------	-----	-----	-----	-----	-----	-----	-----	-----	-----	-----

Bit 23 : Fault Status:

- 0 = No Fault
- 1 = Indicates a fault has occurred and should be viewed in the fault status register.

Bit 22 : Intflg:

- 0 = No Change of state
- 1 = Change of state detected.

Bit 21 – 0 : SPx /SGx input status:

- 0 = Open switch
- 1 = Closed switch

8.10.24 Fault status register

To read the fault status bits, the user should first send a message to the IC with the fault status register address followed by any given second command. The MISO response from the second command will contain the fault flags information.

Table 34. Fault status register

Register address	R	SPI data bits [23 – 0]									
[31–25]	[24]	bit 23	bit 22	bit 21	bit 20	bit 19	bit 18	bit 17	bit 16		
0100_001	0	Unused	INTflg	Unused							
Default After POR		0	1	0	0	0	0	0	0		
		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8		
		Unused					SPI error	Hash Fault	Unused		
		0	0	0	0	0	X	X	0		
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0		
		UV	OV	TempFlag	OT	INT_B Wake	WAKE_B Wake	SPI Wake	POR		
	X	X	X	X	X	X	X	X			
MISO return word		bit [23]	bit [22]	bits [21–0]							
0100_0010		FAULT STATUS	INTflg	FAULT/FLAG BITS							

Table 35. MISO response for fault status command

Bit	Functions	Default value	Description
23	Unused	0	Unused
22	INTflg	X	Reports that an Interrupt has occurred, user should read the status register to determine cause. • Set: Various (SGx change of state, SPx change of state, Extended status bits). • Reset: Clear of fault or read of Status register
21–11	Unused	0	Unused
10	SPI error	X	Any SPI error generates a bit (Wrong address, incorrect modulo). • Set: SPI message error. • Reset: Read fault status register and no SPI errors.
9	Hash Fault	X	SPI register and hash mismatch. • Set: Mismatch between SPI registers and hash. • Reset: No mismatch and SPI flag read.
8	Unused	0	Unused
7	UV	X	Reports that low V _{BATP} voltage was in undervoltage range • Set: Voltage drops below UV level. • Reset: VBATP rises above UV level and flag read (SPI)
6	OV	X	Report that the voltage on VBATP was higher than OV threshold • Set: Voltage at VBATP rises above overvoltage threshold. • Reset: Overvoltage condition is over and flag read (SPI)
5	Temp Flag	X	Temperature warning to note elevated IC temperature • Set: tLIM warning threshold is passed. • Reset: Temperature drops below thermal warning threshold + hysteresis and flag read (SPI)
4	OT	X	Tlim event occurred on the IC • Set: Tlim warning threshold is passed. • Reset: Temperature drops below thermal warning threshold + hysteresis and flag read (SPI)
3	INT_B Wake	X	Part awakens via an external INT_B falling edge • Set: INT_B Wakes the part from LPM (external falling edge) • Reset: flag read (SPI).
2	WAKE_B Wake	X	Part awakens via an external WAKE_B falling edge • Set: External WAKE_B falling edge seen • Reset: flag read (SPI).
1	SPI Wake	X	Part awaken via a SPI message • Set: SPI message wakes the IC from LPM • Reset: flag read (SPI).
0	POR	X	Reports a POR event occurred. • Set: Voltage at VBATP pin dropped below VBATP(POR) voltage • Reset: flag read (SPI)

8.10.25 Interrupt request

The MCU may request an Interrupt pulse of duration 100 μs by sending the Interrupt request command. After an Interrupt request command, the CD1020 returns the Interrupt request command word, as well as the Fault status and INTflg bits set if a fault/interrupt event occurred. Sending an interrupt request command does not set the INTflg bit itself.

Table 36. Interrupt request command

Register address	W	SPI data bits [23 – 0]	
[31–25]	[24]	bits [23 – 16]	
0100_011	1	0000_0000	
		bits [15 – 8]	
		0000_0000	
		bits [7 – 0]	
		0000_0000	
MISO return word	bit [23]	bit [22]	bits [21–0]
0100_0111	FAULT STATUS	INTflg	0

8.10.26 Reset register

Writing to this register causes all of the SPI registers to reset.

Table 37. Reset command

Register address	W	SPI data bits [23 – 0]	
[31–25]	[24]	bits [23 – 16]	
0100_100	1	0000_0000	
		bits [15 – 8]	
		0000_0000	
		bits [7 – 0]	
		0000_0000	
MISO return word	bit [23]	bit [22]	bits [21–0]
0011_1110	FAULT STATUS	INTflg	Switch Status

9 General product characteristics

9.1 Maximum ratings

Table 38. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit	Notes
Electrical ratings					
VBATP	Battery voltage	-0.3	40	V	
VDDQ	Supply voltage	-0.3	7.0	V	
CS_B, MOSI, MISO, SCLK	SPI inputs/outputs	-0.3	7.0	V	
SGx, SPx	Switch input range	-14 ⁽²⁾	38	V	
AMUX	AMUX	-0.3	7.0	V	
INT_B	INT_B	-0.3	7.0	V	
WAKE_B	WAKE_B	-0.3	40	V	
V _{ESD1-2} V _{ESD1-3} V _{ESD3-1} V _{ESD2-1} V _{ESD2-2}	ESD voltage • Human Body Model (HBM) (VBATP versus GND) CD1020 • Human Body Model (HBM) (All other pins) • Machine Model (MM) • Charge Device Model (CDM) (Corners pins) • Charge Device Model (CDM) (All other pins)		±2000 ±2000 ±200 ±750 ±500	V	(3)
V _{ESD5-3} V _{ESD5-4} V _{ESD6-2}	Contact discharge • VBATP ⁽⁵⁾ • WAKE_B (series resistor 10 kΩ) • SGx and SPx pins with 100 nF capacitor (50 Ω series R)		±8000 ±8000 ±8000	V	(4)

Notes

- Minimum value of -18 V is guaranteed by design for switch input voltage range (SGx, SPx).
- ESD testing is performed in accordance AEC Q100, with the Human Body Model (HBM) (C_{ZAP} = 100 pF, R_{ZAP} = 1500 Ω), the Machine Model (MM) (C_{ZAP} = 200 pF, R_{ZAP} = 0 Ω), and the Charge Device Model (CDM).
- C_{ZAP} = 330 pF, R_{ZAP} = 2.0 kΩ (powered and unpowered) / C_{ZAP} = 150 pF, R_{ZAP} = 330 Ω (unpowered)
- External component requirements at system level:
C_{bulk} = 100 μF aluminum electrolytic capacitor
C_{bypass} = 100 nF ±37 % ceramic capacitor
Reverse blocking diode from Battery to VBATP (0.6 V < V_F < 1 V). See [Figure 22. Typical application diagram](#).

9.2 Thermal characteristics

Table 39. Thermal ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Description (rating)	Min	Max	Unit	Notes
Thermal ratings					
T_A T_J	Operating Temperature • Ambient • Junction	-40 -40	125 150	°C	
T_{STG}	Storage Temperature	-65	150	°C	
T_{PPRT}	Peak Package Reflow Temperature During Reflow	-	-	°C	
Thermal resistance					
$R_{\theta JA}$	Junction-to-Ambient, Natural Convection, Single-Layer Board • 32 QFN	—	94	°C/W	(6) (7)
$R_{\theta JB}$	Junction-to-Board • 32 QFN	—	12	°C/W	(8)
$R_{\theta JC}$	Junction-to-Case (Bottom) • 32 QFN	—	2.0	°C/W	(9)
Ψ_{JT}	Junction-to-Package (Top), Natural convection • 32 QFN	—	2.0	°C/W	(10)
Package dissipation ratings					
T_{SD}	Thermal shutdown • 32 QFN	155	185	°C	
T_{SDH}	Thermal shutdown hysteresis • 32 QFN	3.0	15	°C	

Notes

- 6. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
- 7. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
- 8. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
- 9. Thermal resistance between the die and the solder pad on the bottom of the package based on simulation without any interface resistance.
- 10. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

9.3 Operating conditions

This section describes the operating conditions of the device. Conditions apply to the following data, unless otherwise noted.

Table 40. Operating conditions

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Ratings	Min	Max	Unit	Notes
VBATP	Battery voltage	6.0	36	V	
VDDQ	Supply voltage	3.0	5.25	V	
CS_B, MOSI, MISO, SCLK	SPI inputs / outputs	3.0	5.25	V	
SGx, SPx	Switch input range	-1.0	36	V	
AMUX, INT_B	AMUX, INT_B	0.0	5.25	V	
WAKE_B	WAKE_B	0.0	36	V	

9.4 Electrical characteristics

9.4.1 Static electrical characteristics

Table 41. Static electrical characteristics

T_A = -40 °C to +125 °C, VDDQ = 3.1 V to 5.25 V, VBATP = 6.0 V to 28.0 V, unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Units	Notes
Power input						
V _{BATP(POR)}	VBATP supply voltage POR • VBATP supply Power-On-Reset voltage.	2.7	3.3	3.8	V	
V _{BATPUV}	VBATP undervoltage rising threshold	—	4.3	4.5	V	
V _{BATPUVHYS}	VBATP undervoltage hysteresis	250	—	500	mV	
V _{BATPOV}	VBATP overvoltage rising threshold	32	—	37	V	
V _{BATPOVHYS}	VBATP overvoltage hysteresis	1.5	—	3.0	V	
I _{BAT(ON)}	VBATP supply current • All switches open, normal mode, tri-state disabled (all channels)	—	7.0	12	mA	
I _{BATP,IQ,LPM,P}	VBATP low-power mode supply current (polling disabled) • Parametric V _{BATP} , 6.0 V < V _{BATP} < 28 V	—	—	40	µA	
I _{POLLING,IQ}	VBATP polling current • Polling 64 ms, 11 inputs of wake enabled	—	—	20	µA	(11)
I _{VDDQ,NORMAL}	Normal mode (I _{VDDQ}) • SCLK, MOSI, WakeB = 0 V, CS_B, INT_B = V _{DDQ} , no SPI communication, AMUX selected no input	—	—	500	µA	
I _{VDDQ,LPM}	Logic low-power mode supply current • SCLK, MOSI = 0 V, CS_B, INT_B, WAKE_B = V _{DDQ} , no SPI communication	—	—	10	µA	
V _{GNDOFFSET}	Ground Offset • Ground offset of Global pins to IC ground	-1.0	—	1.0	V	(20)
V _{VDDQUV}	VDDQ undervoltage falling threshold	2.2	—	2.8	V	
V _{VDDQUVHYS}	VDDQ undervoltage hysteresis	150	—	350	mV	
Switch input						
I _{LEAKSG_GND}	Leakage (SGx/SPx pins) to GND • Inputs tristated, analog mux selected for each input, voltage at SGx = VBATP	—	—	2.0	µA	
I _{LEAKSG_BAT}	Leakage (SGx/SPx pins) to battery • Inputs tristated, analog mux selected for each input, voltage at SGx = GND	—	—	2.0	µA	
I _{SUSSG}	SG sustain current / mode 0 wetting current • VBATP 6.0 to 28 V	1.6	2.0	2.4	mA	
I _{SUSSB}	SB sustain current / mode 0 wetting current	1.75	2.2	2.85	mA	
I _{WET}	Wetting current level (SG and SB) • Mode 1 = 8 mA • Mode 2 = 12 mA • Mode 3 = 16 mA	—	8 12 16	—	mA	

Table 41. Static electrical characteristics...continued

$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{DDQ} = 3.1\text{ V}$ to 5.25 V , $V_{BATP} = 6.0\text{ V}$ to 28.0 V , unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Units	Notes
I_{WETSG}	SG wetting current tolerance • Mode 1 to 3	—	20	—	%	
I_{WETSB}	SB wetting current tolerance • Mode 1 to 3	—	20	—	%	
V_{ICTHR}	Switch detection threshold	3.7	4.0	4.3	V	(17)
$V_{ICTHRLPM}$	Switch detection threshold low-power mode (SG only)	100	—	300	mV	(18)
V_{ICTHRH}	Switch detection threshold hysteresis (4.0 V threshold)	80	—	300	mV	
$V_{ICTH2P5}$	Input threshold 2.5 V, • Used for Comp Only	2.0	2.5	3.0	V	
$I_{ACTIVEPOLLSG}$	Low-power mode polling current SG • $V_{BATP} = 6.0\text{ V}$ to 28 V	0.7	1.0	1.44	mA	
$I_{ACTIVEPOLLSB}$	Low-power mode polling current SB	1.75	2.2	2.85	mA	
Digital interface						
I_{HZ}	Tri-state leakage current (MISO) • $V_{DDQ} = 0.0$ to V_{DDQ}	-2.0	—	2.0	μA	
$V_{INLOGIC}$	Input logic voltage thresholds • SI, SCLK, CS_B, INT_B	$V_{DDQ} * 0.25$	—	$V_{DDQ} * 0.7$	V	
$V_{INLOGICHYS}$	Input logic hysteresis • SI, SCLK, CS_B, INT_B	300	—	—	mV	
$V_{INLOGICWAKE}$	Input logic voltage threshold WAKE_B	0.8	1.25	1.7	V	
$V_{INWAKEBHYS}$	Input logic voltage hysteresis WAKE_B	200	—	800	mV	
I_{SCLK}, I_{MOSI}	SCLK / MOSI input current • SCLK / MOSI = 0 V	-3.0	—	3.0	μA	
I_{SCLK}, I_{MOSI}	SCLK / MOSI pulldown current • SCLK / MOSI = V_{DDQ}	30	—	100	μA	
I_{CS_BH}	CS_B input current • CS_B = V_{DDQ}	-10	—	10	μA	
R_{CS_BL}	CS_B pull-up resistor to V_{DDQ} • CS_B = 0.0 V	40	125	270	k Ω	
V_{OHMISO}	MISO high-side output voltage • $I_{OHMISO} = -1.0\text{ mA}$	$V_{DDQ} - 0.8$	—	V_{DDQ}	V	
V_{OLMISO}	MISO low-side output voltage • $I_{OLMISO} = 1.0\text{ mA}$	—	—	0.4	V	
C_{IN}	Input Capacitance on SCLK, MOSI, Tri-state MISO (GBD)	—	—	20	pF	
Analog MUX output						
V_{OFFSET}	Input offset voltage when selected as analog • ES suffix (QFN at $T_A = -40\text{ }^\circ\text{C}$ to $25\text{ }^\circ\text{C}$)	-15	—	15	mV	(19), (20)
V_{OLAMUX}	Analog operational amplifier output voltage • Sink 1.0 mA	—	—	50	mV	
V_{OHAMUX}	Analog operational amplifier output voltage • Source 1.0 mA	$V_{DDQ} - 0.1$	—	—	V	
INT_B						
V_{OLINT}	INT_B output low voltage • $I_{OUT} = 1.0\text{ mA}$	—	0.2	0.5	V	
V_{OHINT}	INT_B output high voltage • INT_B = Open-circuit	$V_{DDQ} - 0.5$	—	V_{DDQ}	V	
R_{PU}	Pull-up resistor to V_{DDQ}	40	125	270	k Ω	
$I_{LEAKINT_B}$	Leakage current INT_B • INT_B pulled up to V_{DDQ}	—	—	1.0	μA	
Temperature limit						
t_{FLAG}	Temperature warning • First flag to trip	105	120	135	$^\circ\text{C}$	
t_{LIM}	Temperature monitor	155	—	185	$^\circ\text{C}$	(19)
$t_{LIM(HYS)}$	Temperature monitor hysteresis	5.0	—	15	$^\circ\text{C}$	(19)

Table 41. Static electrical characteristics...continued

$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{DDQ} = 3.1\text{ V}$ to 5.25 V , $V_{BATP} = 6.0\text{ V}$ to 28.0 V , unless otherwise noted.

Symbol	Characteristic	Min	Typ	Max	Units	Notes
WAKE_B						
$R_{WAKE_B(RPU)}$	WAKE_B internal pull-up resistor to VDDQ	40	125	270	kΩ	
$V_{WAKE_B(VOH)}$	WAKE_B voltage high • WAKE_B = Open-circuit	$V_{DDQ} - 1.0$	—	V_{DDQ}	V	
$V_{WAKE_B(VOL)}$	WAKE_B voltage low • WAKE_B = 1.0 mA (R_{PU} to $V_{BATP} = 16\text{ V}$)	—	—	0.4	V	
I_{WAKE_BLEAK}	WAKE_B leakage • WAKE_B pulled up to $V_{BATP} = 16\text{ V}$ through 10 kΩ	—	—	1.0	μA	
Notes 11. Guaranteed by design 12. During low voltage range operation SG wetting current may be limited when there is not enough headroom between V_{BATP} and SG pin voltage. 13. $(I_{SUS(MAX)} - I_{SUS(MIN)}) \times 100 / I_{SUS(MIN)}$ 14. Sustain current source (SGs only) 15. $(I_{WET(MAX)} - I_{WET(MIN)}) \times 100 / I_{WET(MIN)}$ 16. Wetting current source (SGs only) 17. The input comparator threshold decreases when $V_{BATP} \leq 6.0\text{ V}$. 18. SP (as SB) only use the 4.0 V V_{ICTHR} for LPM wake-up detection. 19. Guaranteed by characterization in the Development Phase, parameter not tested. 20. AMUX output voltage deviates when there are negative inputs on other SGx/SPx pins.						

9.4.2 Dynamic electrical characteristics

Table 42. Dynamic electrical characteristics

$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$, $V_{DDQ} = 3.1\text{ V}$ to 5.25 V , $V_{BATP} = 6.0\text{ V}$ to 28 V , unless otherwise specified. All SPI timing is performed with a 100 pF load on MISO, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Units	Notes
General						
t_{ACTIVE}	POR to active time • Undervoltage to normal mode	250	340	450	μs	
Switch input						
$t_{PULSE(ON)}$	Pulse wetting current timer • Normal mode	17	20	23	ms	
$t_{INT-DLY}$	Interrupt delay time • Normal mode	—	—	18.5	μs	
$t_{POLLING_TIMER}$	Polling timer accuracy • Low-power mode	—	—	15	%	
$t_{ACTIVEPOLLSGTIME}$	Tactivepoll timer SG	49.5	58	66.5	μs	
$t_{ACTIVEPOLLSBTIME}$	Tactivepoll timer SB • SBPOLLTIME = 0 • SBPOLLTIME = 1	1.0 49.5	1.2 58	1.4 66.5	ms μs	
$t_{GLITCHTIMER}$	Input glitch filter timer • Normal mode	5.0	—	18	μs	
AMUX output						
$AMUX_{VALID}$	AMUX access time (selected output to selected output) • $C_{MUX} = 1.0\text{ nF}$, Rising edge of CS_B to selected	—	(22)	—	μs	
$AMUX_{VALIDTS}$	AMUX access time (tri-state to ON) • $C_{MUX} = 1.0\text{ nF}$, rising edge of CS_B to selected	—	—	20	μs	
Oscillator						
OSC_{TOLLPM}	Oscillator tolerance at 192 kHz in low-power mode	-15	—	15	%	
OSC_{TOLNOR}	Oscillator tolerance normal mode at 4.0 MHz	-15	—	15	%	
Interrupt						
INT_{PULSE}	INT pulse duration • Interrupt occurs or INT_B request	90	100	110	μs	

Table 42. Dynamic electrical characteristics...continued

$T_A = -40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$, $V_{DDQ} = 3.1\text{ V}$ to 5.25 V , $V_{BATP} = 6.0\text{ V}$ to 28 V , unless otherwise specified. All SPI timing is performed with a 100 pF load on MISO, unless otherwise noted.

Symbol	Parameter	Min	Typ	Max	Units	Notes
SPI interface						
f_{OP}	Transfer frequency	—	—	8.0	MHz	
t_{SCK}	SCLK period • Figure 6 - 1	160	—	—	ns	
t_{LEAD}	Enable lead time • Figure 6 - 2	140	—	—	ns	
t_{LAG}	Enable lag time • Figure 6 - 3	50	—	—	ns	
t_{SCKHS}	SCLK high time • Figure 6 - 4	56	—	—	ns	
t_{SCKLS}	SCLK low time • Figure 6 - 5	56	—	—	ns	
t_{SUS}	MOSI input setup time • Figure 6 - 6	16	—	—	ns	
t_{HS}	MOSI input hold time • Figure 6 - 7	20	—	—	ns	
t_A	MISO access time • Figure 6 - 8	—	—	116	ns	
t_{DIS}	MISO disable time ⁽²¹⁾ • Figure 6 - 9	—	—	100	ns	
t_{VS}	MISO output valid time • Figure 6 - 10	—	—	116	ns	
t_{HO}	MISO output hold time (no cap on MISO) • Figure 6 - 11	20	—	—	ns	
t_{RO}	Rise time • Figure 6 - 12	—	—	30	ns	(21)
t_{FO}	Fall time • Figure 6 - 13	—	—	30	ns	(21)
t_{CSN}	CS_B negated time • Figure 6 - 14	500	—	—	ns	
WAKE-UP						
t_{CSB_WAKEUP}	LPM mode wake-up time triggered by edge of CS_B	—	755	1000	μs	(23)

Notes
 21. Guaranteed by characterization.
 22. AMUX settling time to be within the 10 mV offset specification. $AMUX_{VALID}$ is dependent on the voltage step applied on the input SGx/SPx pin or the difference between the first and second channel selected as the multiplexed analog output. See Figure 8 for a typical AMUX access time VS voltage step waveform.
 23. The parameter is guaranteed at $V_{BATP} = 6.0\text{ V}$ to 28 V .

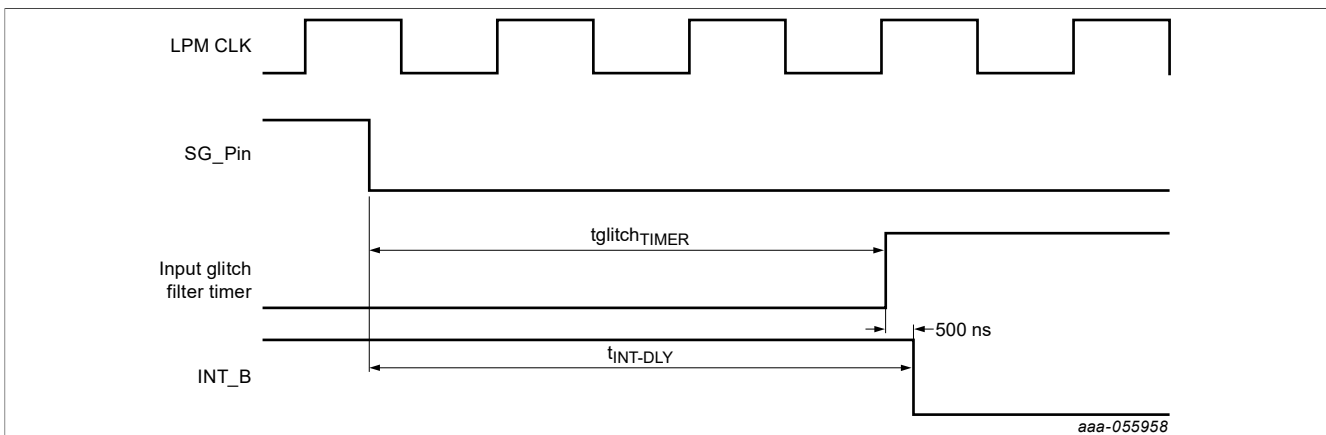
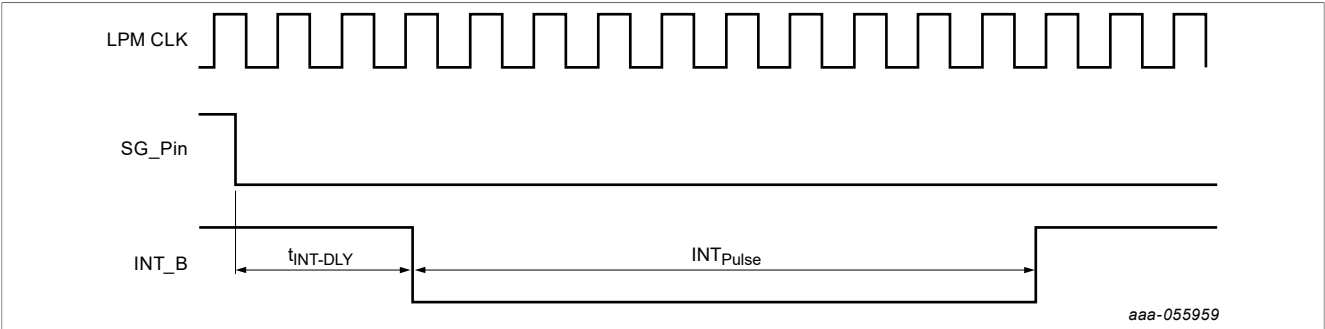
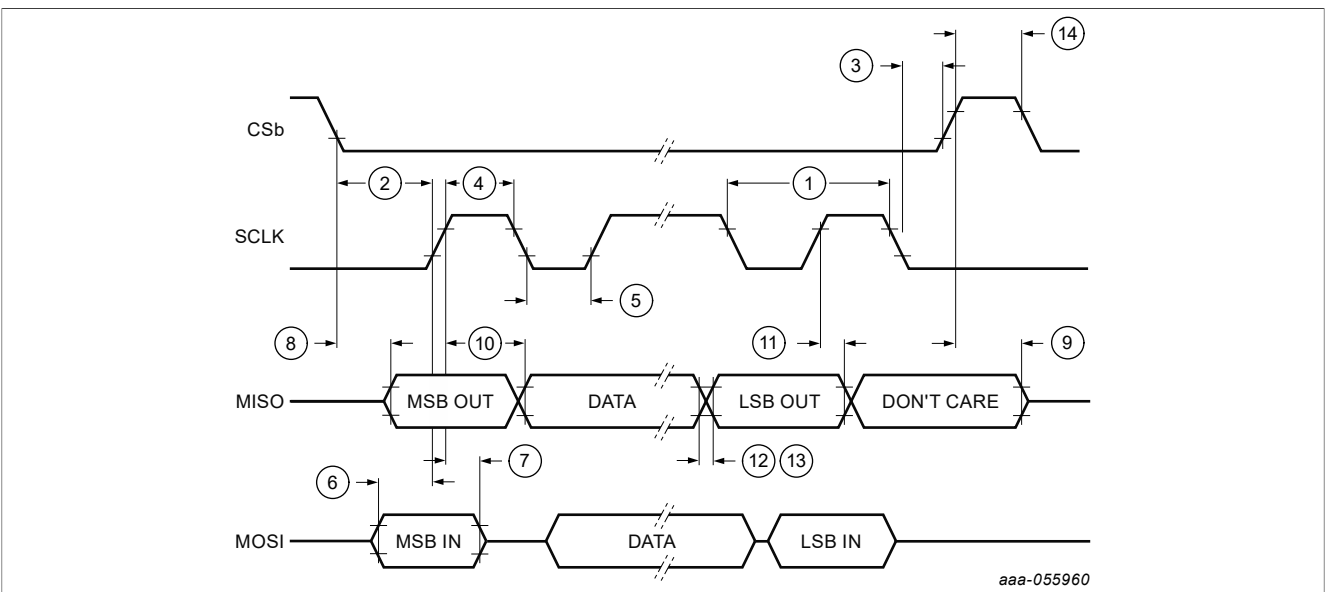


Figure 16. Glitch filter and interrupt delay timers



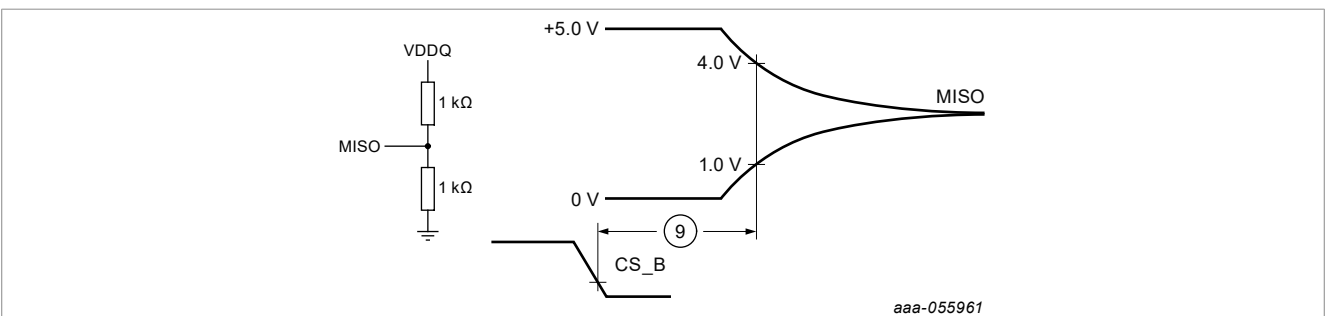
aaa-055959

Figure 17. Interrupt pulse timer



aaa-055960

Figure 18. SPI timing diagram



aaa-055961

Figure 19. MISO loading for disable time measurement

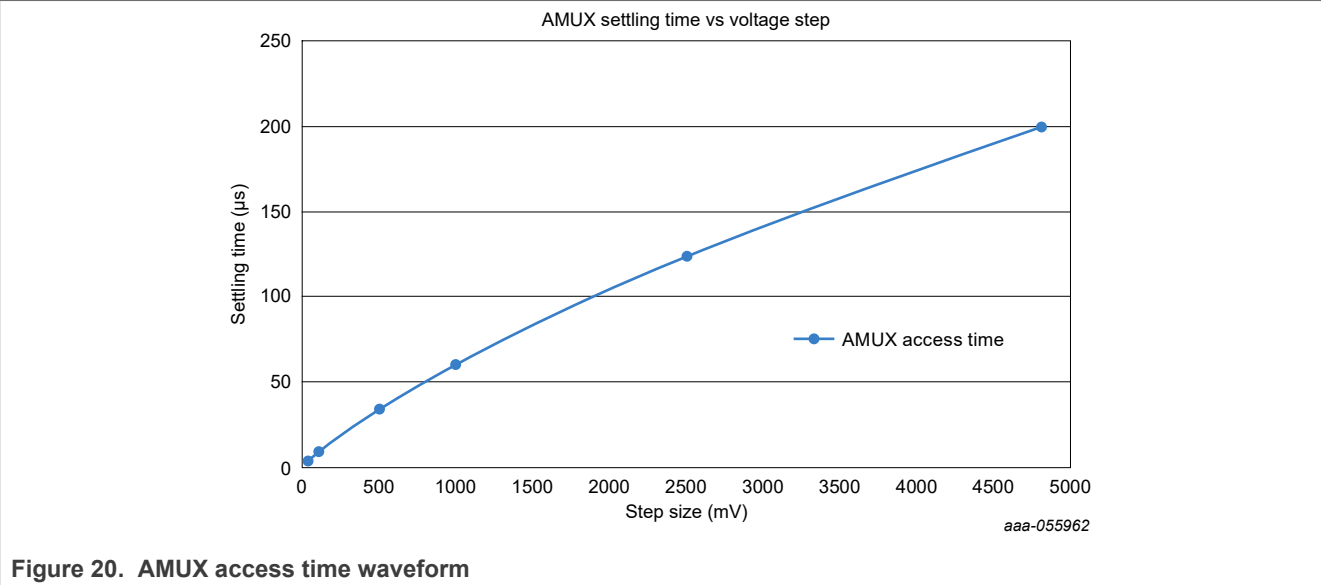


Figure 20. AMUX access time waveform

10 Typical applications

10.1 Simplified application diagram

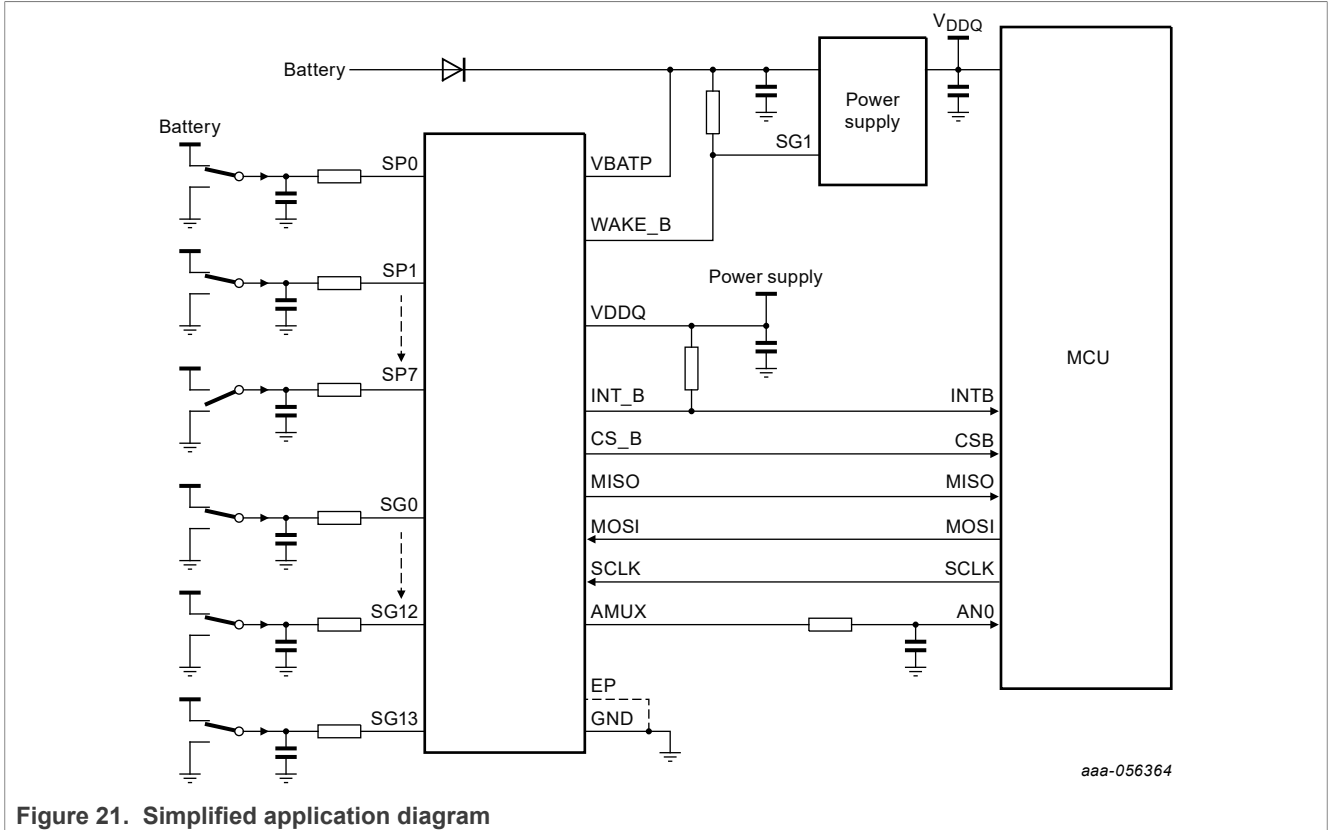


Figure 21. Simplified application diagram

10.2 Application diagram

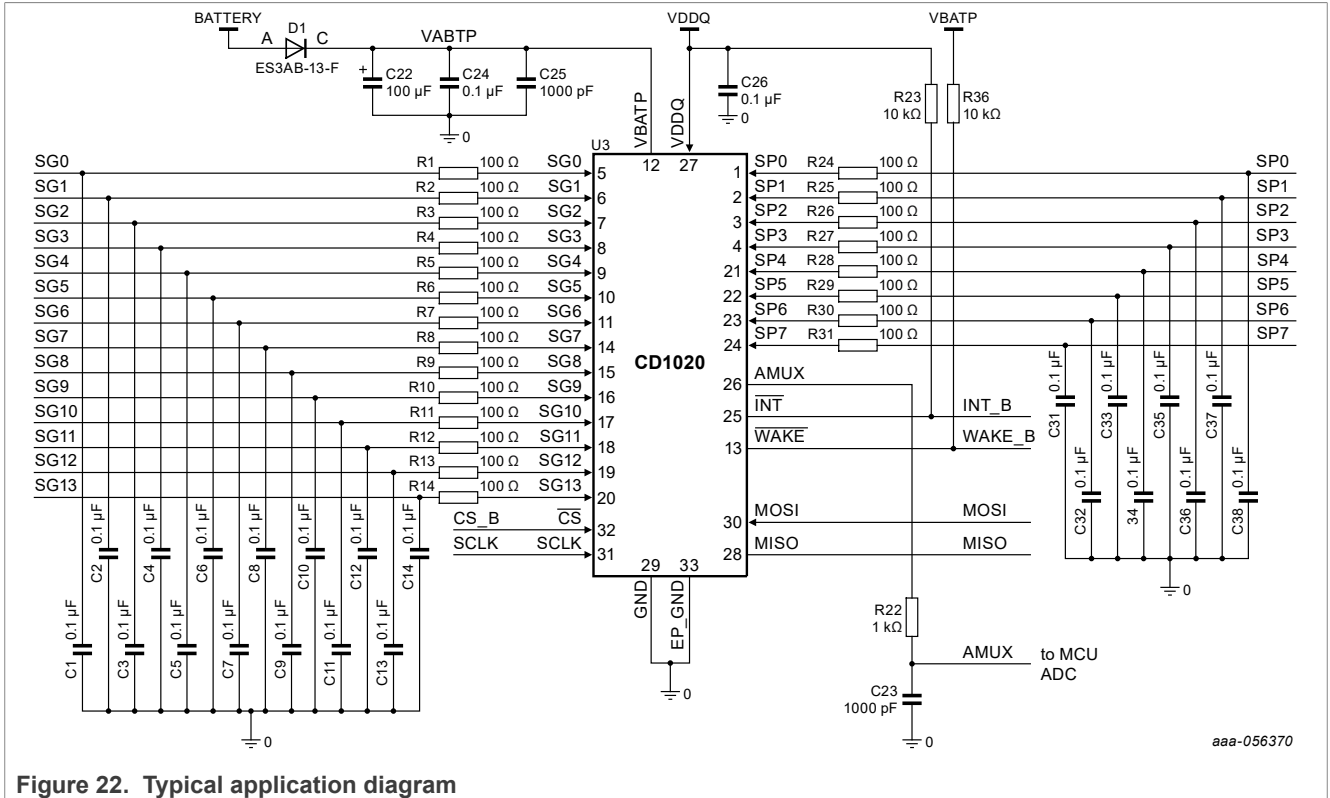


Figure 22. Typical application diagram

10.3 Bill of materials

Table 43. Bill of materials

Item	Quantity	Reference	Value	Description
1	24	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C24, C26, C31, C32, C33, C34, C35, C36, C37, C38	0.1 μ F	CAP CER 0.1 μ F 100 V X7R 10 % 0603
2	2	C23, C25	1.0 nF	CAP CER 1000 pF 100 V 10 % X7R 0603
3	1	C22	100 μ F	CAP ALEL 100 μ F 50 V 20 % – SMD
4	1	D1	—	DIODE RECT 3.0 A 50 V AEC-Q101 SMB
5	22	R1, R2, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, R24, R25, R26, R27, R28, R29, R30, R31	100 Ω	RES MF 100 Ω 0.5 W 1% 0805
6	1	R23	10 k Ω	RES MF 10 k Ω 0.5 W 5 % 0805 (optional)
7	1	R36	10 k Ω	RES MF 10 k Ω 0.5 W 5 % 0805
8	1	R22	1.0 k Ω	RES MF 1 k Ω 0.5 W 5 % 0805
9	1	U3	CD1020	IC MULTIPLE DETECTION SWITCH INTERFACE QFN 32-pin

10.4 Abnormal operation

The CD1020 could be subject to various conditions considered abnormal as defined within this section.

10.4.1 Reverse battery

This device with applicable external components will not be damaged by exposure to reverse battery conditions of -14 V. This test is performed for a period of one minute at 25 °C. In addition, this negative voltage condition does not force any of the logic level I/O pins to a negative voltage less than -0.6 V at 10 mA or to a positive voltage greater than 5.0 V. This ensures protection of the digital device interfacing with this device.

10.4.2 Ground offset

The applicable driver outputs and/or current sense inputs are capable of operation with a ground offset of ± 1.0 V. The device will not be damaged by exposure to this condition and will maintain specified functionality. AMUX output voltage deviates when there are negative ground offsets on other SGx/SPx pins.

10.4.3 Shorts to ground

All I/Os of the device that are available at the module connector are protected against shorts to ground with maximum ground offset considered, i.e. -1.0 V referenced to device ground or other application specific value. The device will not be damaged by this condition.

10.4.4 Shorts to battery

All I/Os of the device that are available at the module connector are protected against a short to battery (voltage value is application dependent, there may be cases where short to jump start or load dump voltage values are required). The device will not be damaged by this condition.

10.4.5 Unpowered shorts to battery

All I/Os of the device that are available at the module connector are protected against unpowered (battery to the module is open) shorts to battery per application specifics. The device will not be damaged by this condition, will not enable any outputs nor backfeed onto the power rails (VBATP, VDDQ) or the digital I/O pins.

10.4.6 Loss of module ground

The definition of a loss of ground condition at the device level is that all pins of the IC detects very low impedance-to-battery. The nomenclature is suited to a test environment. In the application, a loss of ground condition results in all I/O pins floating to battery voltage, while all externally referenced I/O pins are, at worst case, pulled to ground. All applicable driver outputs and current sense inputs are protected against excessive leakage current due to loads that are referenced to an external ground (high-side drivers).

10.4.7 Loss of module battery

The loss of battery condition at the parts level is that the power input pins of the IC see infinite impedance to the battery supply voltage (depending upon the application) but there is some undefined impedance looking from these pins to ground. All applicable driver outputs and current sense inputs are protected against excessive leakage current due to loads that are referenced to an external battery connection (low-side drivers).

11 Packaging

11.1 Package mechanical dimensions

Package dimensions are provided in package drawings. To find the most current package outline drawing, go to www.nxp.com and perform a keyword search for the drawing's document number.

Table 44. Packaging information

Package	Suffix	Package outline drawing number
32-pin QFN (WF-type)	ES	98ASA00656D

11.2 Package drawing

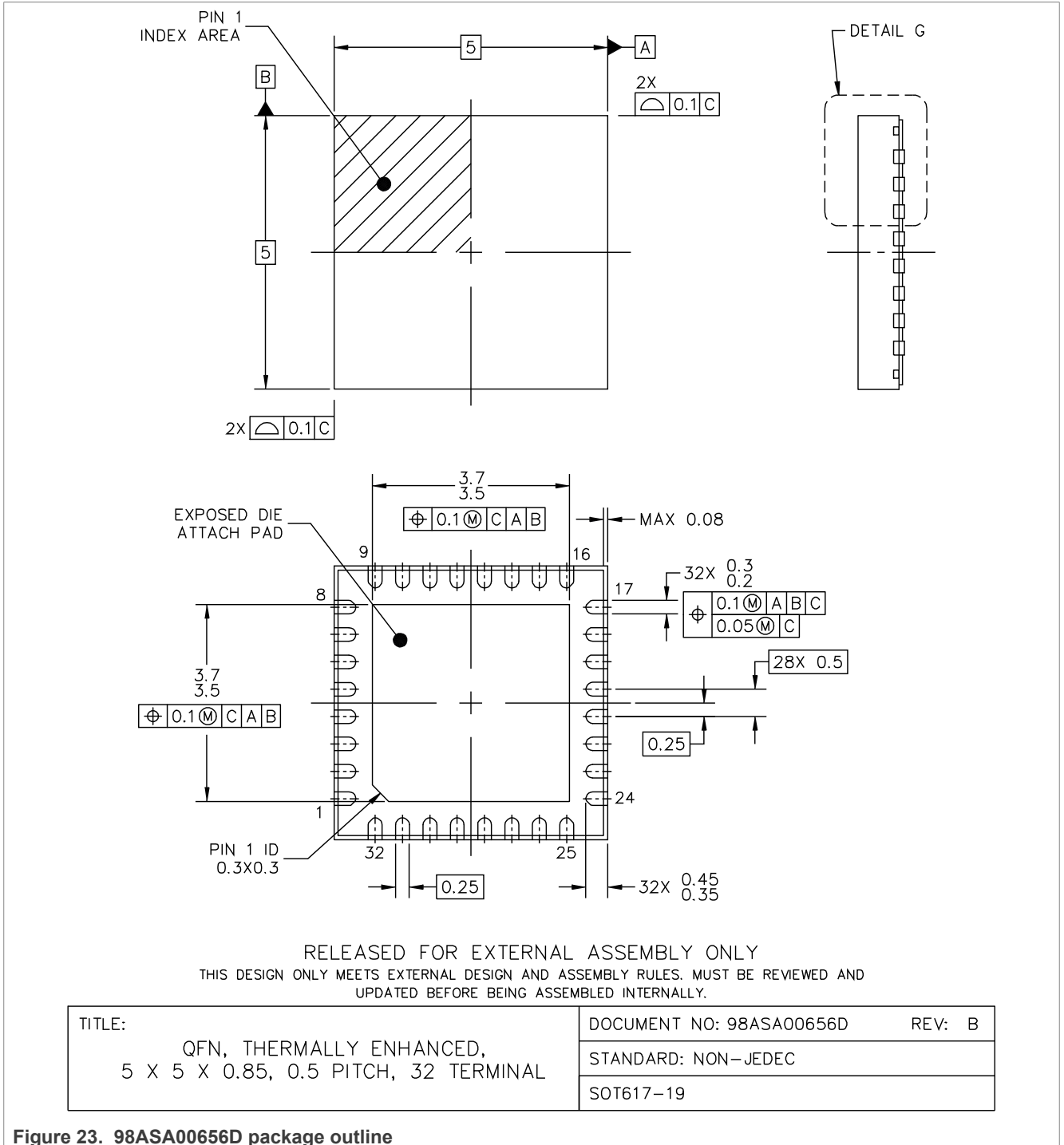
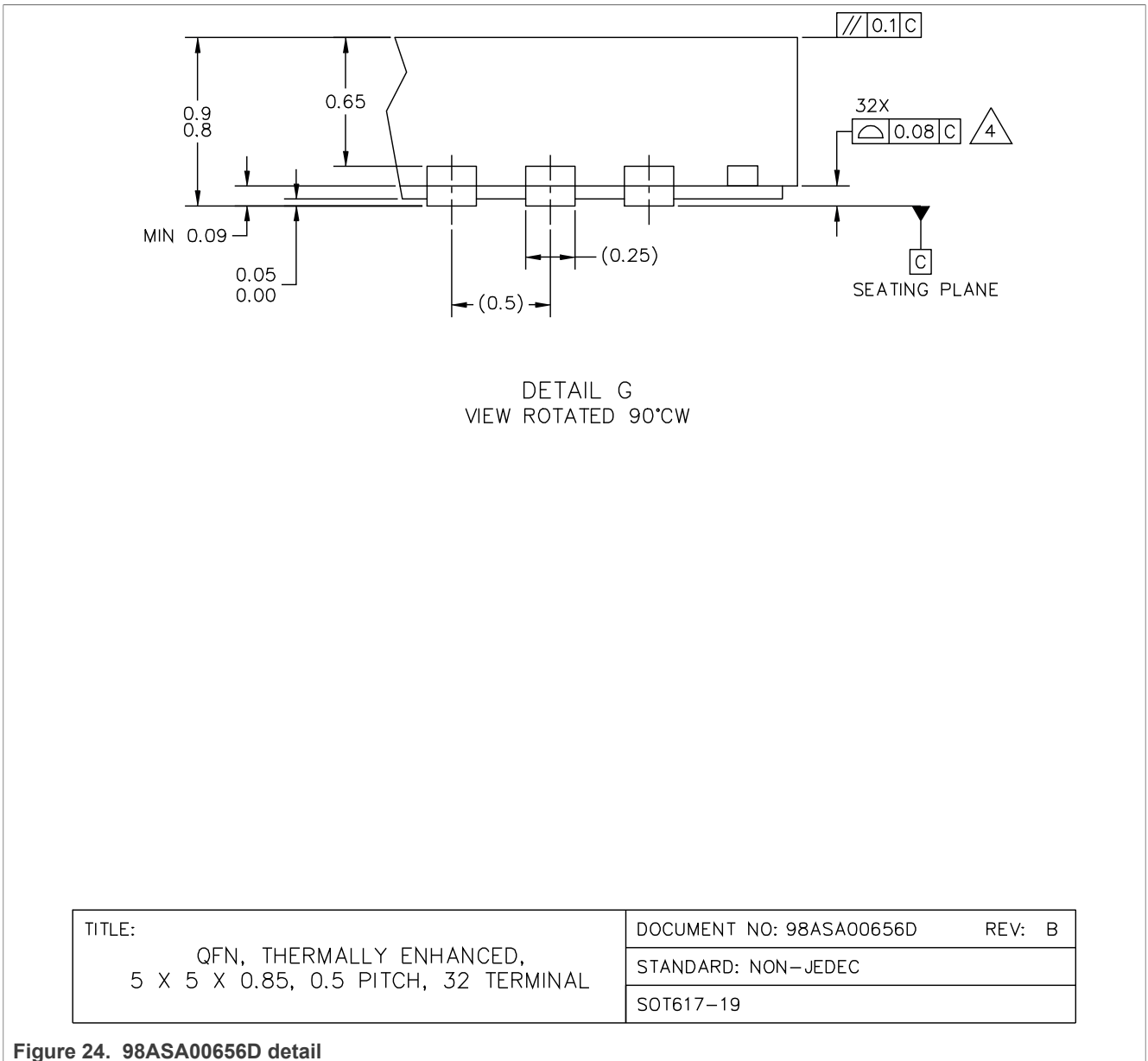



Figure 23. 98ASA00656D package outline



NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. THIS IS A NON-JEDEC REGISTERED PACKAGE.
4.  COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.
5. MIN. METAL GAP SHOULD BE 0.2 MM.

TITLE: QFN, THERMALLY ENHANCED, 5 X 5 X 0.85, 0.5 PITCH, 32 TERMINAL	DOCUMENT NO: 98ASA00656D	REV: B
	STANDARD: NON-JEDEC	
	SOT617-19	

Figure 25. 98ASA00656D notes

12 Reference section

Table 45. CD1020 reference documents

Reference	Description
CDF-AEC-Q100	Stress Test Qualification For Automotive Grade Integrated Circuits
Q-1000	Qualification Specification for Integrated Circuits
SQ-1001	Specification Conformance
ISO 7637	Electrical Disturbances from Conduction and Coupling
ISO 61000	Electromagnetic Compatibility

13 Revision history

Revision	Date	Description of changes
5.0	20 August 2024	<ul style="list-style-type: none"> • CIN 202407012I • Changed organization and format to conform to current data sheet template • Corrected Section 1 to mention polling mode • Replaced <i>slave</i> with <i>secondary</i> or <i>secondary device</i> <ul style="list-style-type: none"> – Section 6.2 (two instances) – Section 8.9 (one instance) • Replaced <i>master</i> with <i>primary</i> or <i>primary device</i> <ul style="list-style-type: none"> – Section 8.9.2 (two instances) – Section 8.9.4 (one instance) • Updated package drawing in Section 11.2 to Rev B • Updated legal information
4.0	July 2019	<ul style="list-style-type: none"> • Updated Figure 22 and Table 43, Bill of materials as per CIN 201907004I
3.0	July 2018	<ul style="list-style-type: none"> • Changed document status from Advance Information to Technical Data • Added t_{CSB_WAKEUP} parameter to Table 7
2.0	February 2018	<ul style="list-style-type: none"> • Changed document specification state from Product Preview to Advance Information • Table 3, Maximum ratings <ul style="list-style-type: none"> – Deleted V_{ESD6-1}, description, parameter, and footnote 5 • Table 6, Static electrical characteristics <ul style="list-style-type: none"> – Added footnote ‘AMUX output voltage deviates when there are negative inputs on other SGx/SPx pins.’ to $V_{GNDOFFSET}$ and V_{OFFSET} • Table 7, Dynamic electrical characteristics <ul style="list-style-type: none"> – Deleted $i_{INT-TIMER}$ row • Section 7.8, deleted last sentence of section, ‘Since the device is required...’ • Table 11, Device configuration register <ul style="list-style-type: none"> – Changed bit 9 from Aconfig1 to Unused – Changed bit 8 from Aconfig0 to Unused • Section 7.10.22, AMUX control register <ul style="list-style-type: none"> – Changed ‘Internal to the CD1020 is a 24-to-1...’ to ‘Internal to the CD1020 is a 22-to-1...’ • Section 8.2, Bill of materials <ul style="list-style-type: none"> – Changed item 9 from ‘...SWITCH INTERFACE SOIC32’ to ‘...SWITCH INTERFACE QFN 32 pin’
1.0	June 2017	<ul style="list-style-type: none"> • Initial release

Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <https://www.nxp.com>.

Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <https://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as “Critical Applications”), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys’ fees) that NXP may incur related to customer’s incorporation of any product in a Critical Application.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

HTML publications — An HTML version, if available, of this document is provided as a courtesy. Definitive information is contained in the applicable document in PDF format. If there is a discrepancy between the HTML document and the PDF document, the PDF document has priority.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer’s applications and products. Customer’s responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer’s applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Tab. 1.	Orderable part variations	3	Tab. 24.	LPM voltage threshold configuration SP register	32
Tab. 2.	CD1020 pin definitions	6	Tab. 25.	LPM voltage threshold configuration SG register	33
Tab. 3.	MOSI input register bit definition	21	Tab. 26.	Polling current configuration SP register	33
Tab. 4.	Functional SPI register map	22	Tab. 27.	Polling current configuration SG register	34
Tab. 5.	SPI check command	24	Tab. 28.	Enter low-power mode command	34
Tab. 6.	Device configuration register	24	Tab. 29.	Slow polling SG register	34
Tab. 7.	Device configuration bits definition	25	Tab. 30.	AMUX current select	35
Tab. 8.	Tri-state SP register	25	Tab. 31.	AMUX channel select	35
Tab. 9.	Tri-state SG register	25	Tab. 32.	Read switch status command	36
Tab. 10.	Wetting current level SP register	26	Tab. 33.	MISO output register definition	37
Tab. 11.	Wetting current level SG register 0	26	Tab. 34.	Fault status register	38
Tab. 12.	Wetting current level SG register 1	27	Tab. 35.	MISO response for fault status command	38
Tab. 13.	SPx/SGx selectable wetting current levels	27	Tab. 36.	Interrupt request command	39
Tab. 14.	Continuous wetting current SP register	27	Tab. 37.	Reset command	39
Tab. 15.	Continuous wetting current SG register	28	Tab. 38.	Maximum ratings	40
Tab. 16.	Interrupt enable SP register	29	Tab. 39.	Thermal ratings	41
Tab. 17.	Interrupt enable SG register	30	Tab. 40.	Operating conditions	42
Tab. 18.	Low-power mode configuration register	30	Tab. 41.	Static electrical characteristics	42
Tab. 19.	Low-power mode configuration bits definition	30	Tab. 42.	Dynamic electrical characteristics	44
Tab. 20.	Wake-up enable SP register	31	Tab. 43.	Bill of materials	49
Tab. 21.	Wake-up enable SG register	31	Tab. 44.	Packaging information	51
Tab. 22.	Comparator only SP Register	32	Tab. 45.	CD1020 reference documents	55
Tab. 23.	Comparator only SG register	32			

Figures

Fig. 1.	Functional block diagram	4	Fig. 14.	Daisy chain SPI operation	20
Fig. 2.	CD1020 internal block diagram	5	Fig. 15.	Pulsed/continuous wetting current configuration	29
Fig. 3.	QFN (WF-Type) pinouts	6	Fig. 16.	Glitch filter and interrupt delay timers	45
Fig. 4.	Battery voltage range	9	Fig. 17.	Interrupt pulse timer	46
Fig. 5.	CD1020 state diagram	11	Fig. 18.	SPI timing diagram	46
Fig. 6.	Low-power mode polling check	13	Fig. 19.	MISO loading for disable time measurement	46
Fig. 7.	Low-power mode typical timing	14	Fig. 20.	AMUX access time waveform	47
Fig. 8.	Low-power mode to normal mode operation	14	Fig. 21.	Simplified application diagram	48
Fig. 9.	SG block diagram	15	Fig. 22.	Typical application diagram	49
Fig. 10.	SP block diagram	16	Fig. 23.	98ASA00656D package outline	52
Fig. 11.	First SPI operation (after POR)	19	Fig. 24.	98ASA00656D detail	53
Fig. 12.	SPI write operation	19	Fig. 25.	98ASA00656D notes	54
Fig. 13.	SPI read operation	19			

Contents

1	General description	1	8.10.11	Interrupt enable SG register	30
2	Features and benefits	2	8.10.12	Low-power mode configuration	30
3	Ordering information	3	8.10.13	Wake-up enable register SP	31
4	Functional block diagram	4	8.10.14	Wake-up enable register SG	31
5	Internal block diagram	5	8.10.15	Comparator only SP	31
6	Pinning information	6	8.10.16	Comparator only SG	32
6.1	Pinout	6	8.10.17	LPM voltage threshold SP configuration	32
6.2	Pin definitions	6	8.10.18	LPM voltage threshold SG configuration	33
7	General IC functional description	8	8.10.19	Polling current SP configuration	33
7.1	Battery voltage ranges	8	8.10.20	Polling current SG configuration	33
7.1.1	Load dump (overvoltage)	8	8.10.21	Enter low-power mode	34
7.1.2	Jump start (double battery)	8	8.10.22	AMUX control register	34
7.1.3	Normal battery range	8	8.10.23	Read switch status	36
7.1.4	Undervoltage	8	8.10.24	Fault status register	38
7.1.5	Undervoltage lockout	8	8.10.25	Interrupt request	39
7.1.6	Power-On-Reset (POR) activated	8	8.10.26	Reset register	39
7.1.7	No operation	9	9	General product characteristics	40
7.2	Power sequencing conditions	9	9.1	Maximum ratings	40
7.2.1	VBATP before VDDQ	9	9.2	Thermal characteristics	41
7.2.2	VDDQ before VBATP	9	9.3	Operating conditions	41
7.2.3	VBATP okay, VDDQ lost	10	9.4	Electrical characteristics	42
7.2.4	VDDQ okay, VBATP lost	10	9.4.1	Static electrical characteristics	42
8	Functional block description	11	9.4.2	Dynamic electrical characteristics	44
8.1	State diagram	11	10	Typical applications	48
8.1.1	State machine	11	10.1	Simplified application diagram	48
8.1.2	UV: undervoltage lockout	11	10.2	Application diagram	49
8.1.3	Normal mode	12	10.3	Bill of materials	49
8.1.4	Low-power mode	12	10.4	Abnormal operation	50
8.1.5	Polling mode	12	10.4.1	Reverse battery	50
8.2	Low-power mode operation	12	10.4.2	Ground offset	50
8.3	Input functional block	15	10.4.3	Shorts to ground	50
8.4	Oscillator and timer control functional block	16	10.4.4	Shorts to battery	50
8.5	Temperature monitor and control functional block	16	10.4.5	Unpowered shorts to battery	50
8.6	WAKE_B control functional block	16	10.4.6	Loss of module ground	50
8.7	INT_B functional block	17	10.4.7	Loss of module battery	50
8.8	AMUX functional block	17	11	Packaging	51
8.9	Serial peripheral interface (SPI)	17	11.1	Package mechanical dimensions	51
8.9.1	Chip select low (CS_B)	18	11.2	Package drawing	52
8.9.2	Serial clock (SCLK)	18	12	Reference section	55
8.9.3	Serial data output (MISO)	18	13	Revision history	56
8.9.4	Serial data input (MOSI)	18		Legal information	57
8.10	SPI control register definition	21			
8.10.1	SPI check	24			
8.10.2	Device configuration register	24			
8.10.3	Tri-state SP register	25			
8.10.4	Tri-state SG register	25			
8.10.5	Wetting current level SP register	26			
8.10.6	Wetting current level SG register 0	26			
8.10.7	Wetting current level SG register 1	27			
8.10.8	Continuous wetting current SP register	27			
8.10.9	Continuous Wetting Current SG Register	28			
8.10.10	Interrupt enable SP register	29			

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.