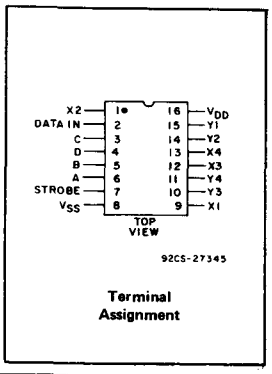
CMOS 4 x 4 Crosspoint Switch with Control Memory

High-Voltage Types (20-Volt Rating)

The RCA-CD22100 combines a 4 x 4 array of crosspoints (transmission gates) with a 4-line-to-16-line decoder and 16 latch circuits. Any one of the sixteen transmission gates (crosspoints) can be selected by applying the appropriate four line address. The selected transmission gate can be turned on or off by applying a logical one or zero, respectively, to the data input and strobing the strobe input to a logical one. Any number of the transmission gates can be ON simultaneously. When the required operating power is applied to the CD22100, the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high and data-in low, and then addressing all switches in succession.

Features:

- **Low ON resistance — 75 Ω typ. at V_{DD} = 12 V**
- **"Built-in" control latches**
- **Large analog signal capability — ± $V_{DD}/2$**
- **10-MHz switch bandwidth**
- **Matched switch characteristics ΔR_{ON} = 18Ω typ. at V_{DD} = 12 V**
- **High linearity — 0.5% distortion (typ.) at f = 1 kHz, V_{IN} = 5 V_{p-p}, V_{DD} = 10 V, and R_L = 1 kΩ**
- **Standard CMOS noise immunity**
- **100% tested for maximum quiescent current at 20 V**



Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT*	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER TRANSMISSION GATE	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

* Maximum current through transmission gates (switches) = 25 mA.

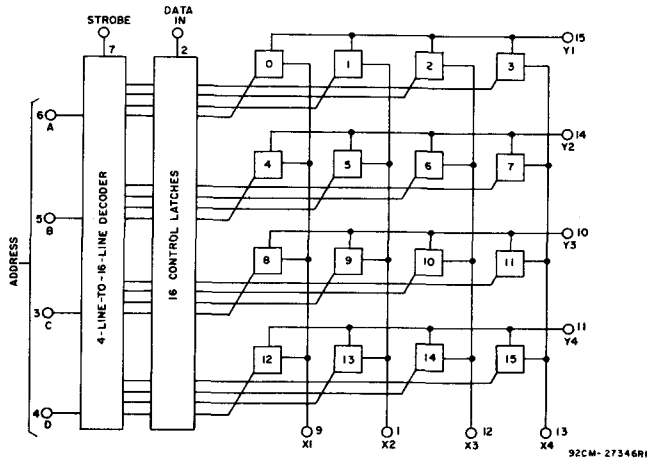


Fig. 1 — Functional diagram.

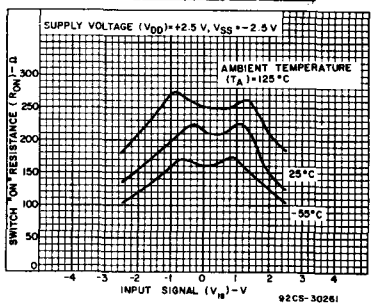


Fig. 2— Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS}$ = 2.5 V.

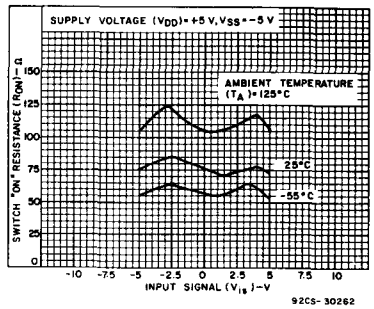


Fig. 3— Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS}$ = 5 V.

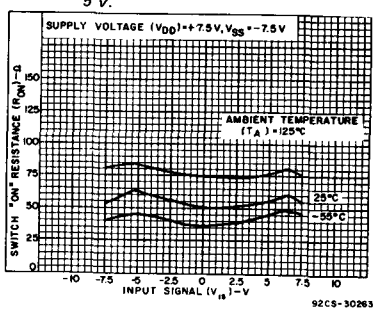


Fig. 4 — Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS}$ = 7.5 V.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

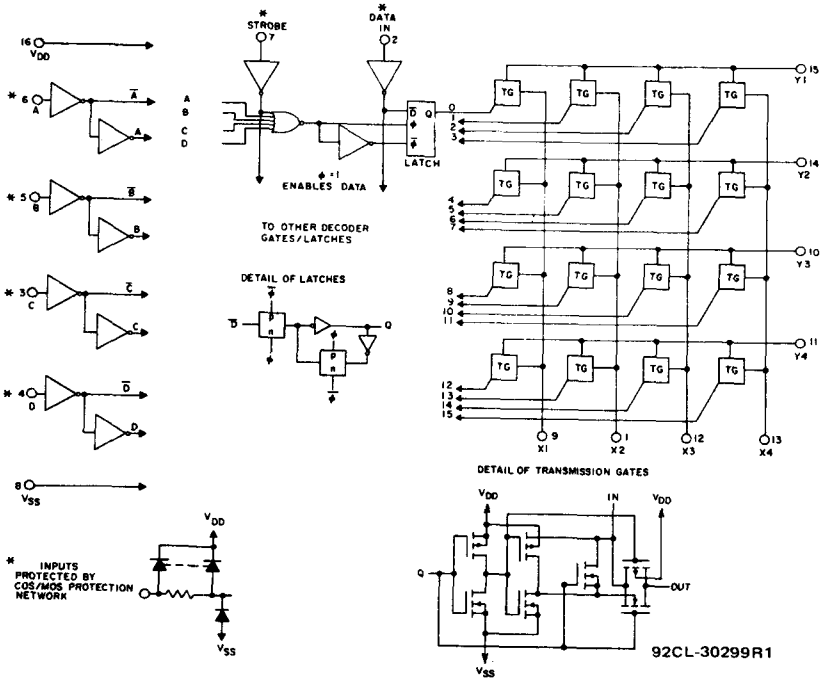


Fig. 6— Schematic diagram.

TRUTH TABLE								
Address				Select	Address				Select
A	B	C	D		A	B	C	D	
0	0	0	0	X1Y1	0	0	0	1	X1Y3
1	0	0	0	X2Y1	1	0	0	1	X2Y3
0	1	0	0	X3Y1	0	1	0	1	X3Y3
1	1	0	0	X4Y1	1	1	0	1	X4Y3
0	0	1	0	X1Y2	0	0	1	1	X1Y4
1	0	1	0	X2Y2	1	0	1	1	X2Y4
0	1	1	0	X3Y2	0	1	1	1	X3Y4
1	1	1	0	X4Y2	1	1	1	1	X4Y4

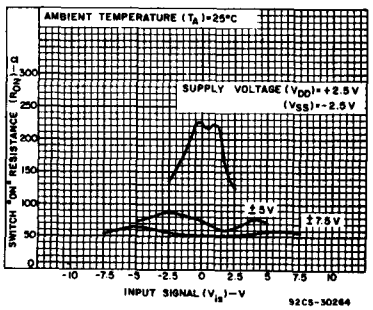


Fig. 5— Typical ON resistance as a function of input signal voltage at T_A = 25°C.

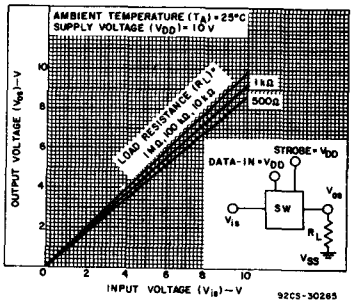


Fig. 7 — Typical switch ON transfer characteristics (1 of 16 switches).

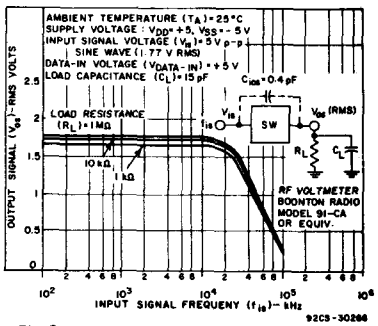


Fig. 8 — Typical switch ON frequency response characteristics.

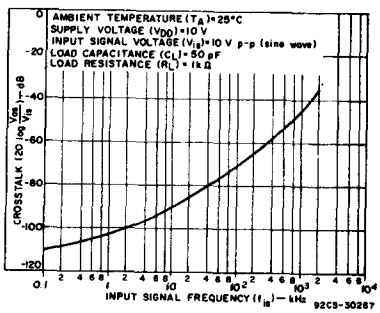


Fig. 9 — Typical crosstalk between switches as a function of signal frequency.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at −55,+25,+125,apply to D,F,H pkg Values at −40,+25,+85,apply to E pkg							Units
		V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
CROSSPOINTS											
Quiescent Device Current, I_{DD} Max.		–	5	5	5	150	150	–	0.04	5	μA
		–	10	10	10	300	300	–	0.04	10	
		–	15	20	20	600	600	–	0.04	20	
		–	20	100	100	3000	3000	–	0.08	100	
ON Resistance R_{ON} Max.	Any Switch V_{IS} = 0 to V_{DD}	–	5	475	500	725	800	–	225	600	Ω
		–	10	135	145	205	230	–	85	180	
		–	12	100	110	155	175	–	75	135	
		–	15	70	75	110	125	–	65	95	
ΔON Resistance, ΔR_{ON}	Between any two switches	–	5	–	–	–	–	–	25	–	Ω
		–	10	–	–	–	–	–	10	–	
		–	12	–	–	–	–	–	8	–	
		–	15	–	–	–	–	–	5	–	
OFF Switch Leakage Current I_L Max.	All switches OFF	0,18	18	±100		±1000		–	±1	±100*	nA
CONTROLS											
Input Low Voltage V_{IL} Max.	OFF switch I_L <0.2 μA	–	5	1.5				–	–	1.5	V
		–	10	3				–	–	3	
		–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	ON switch see R_{ON} characteristic	–	5	3.5				3.5	–	–	
		–	10	7				7	–	–	
		–	15	11				11	–	–	
Input Current, I_{IN} Max.	Any control	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

* Determined by minimum feasible leakage measurement for automatic testing.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	CONDITIONS				LIMITS			UNITS
	f_{is} kHz	R_L kΩ	V_{is}* (V)	V_{DD} (V)	Min.	Typ.	Max.	
CROSSPOINTS								
Propagation Delay Time, (Switch ON) Signal Input to Output, t_{PHL}, t_{PLH}	–	10	5	5	–	30	60	ns
			10	10	–	15	30	
			15	15	–	10	20	
	C_L = 50 pF; t_r, t_f = 20 ns							
Frequency Response, (Any Switch ON)	1	1	5	10	–	40	–	MHz
	Sine wave input, $20 \log \frac{V_{os}}{V_{is}} = -3$ dB							
Sine Wave Response, (Distortion)	1	1	5	10	–	0.5	–	%
Feedthrough (All Switches OFF)	1.6	1	5	10	–	−80	–	dB
	Sine wave input							

*Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$

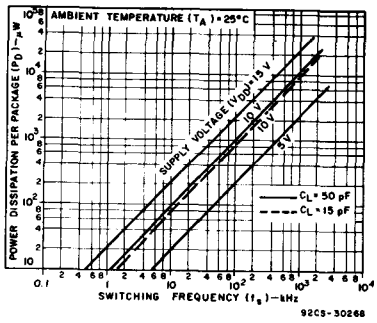


Fig. 10 – Typical dynamic power dissipation as a function of switching frequency.

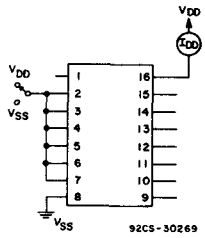


Fig. 11 – Quiescent current test circuit.

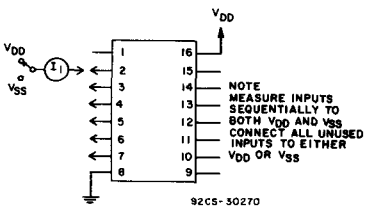


Fig. 12 – Input current test circuit.

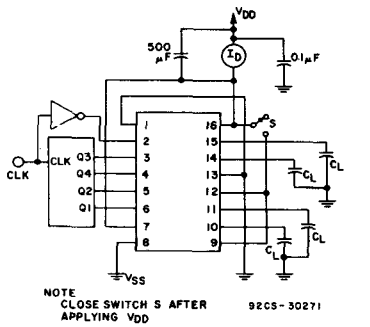


Fig. 13 – Dynamic power dissipation test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	CONDITIONS				LIMITS			UNITS
	f_{is} kHz	R_L kΩ	V_{is}● (V)	V_{DD} (V)	Min.	Typ.	Max.	
CROSSPOINTS (CONT'D)								
Frequency for Signal Crosstalk Attenuation of 40 dB	–	1	10	10	–	1.5	–	MHz
Attenuation of 110 dB	Sine wave input					0.1		kHz
Capacitance, X_n to Ground		–	–	5-15	–	18	–	pF
Y_n to Ground		–	–	5-15	–	30	–	
Feedthrough		–	–	–	–	0.4	–	
CONTROLS			See Fig.					
Propagation Delay Time: Strobe to Output, t_{PZH} (Switch Turn-ON to High Level)	R_L=1kΩ, C_L=50pF, t_r,t_f = 20 ns		18	5	–	300	600	ns
				10	–	125	250	
				15	–	80	160	
Data-In to Output, t_{PZH} (Turn-On to High Level)			19	5	–	110	220	
				10	–	40	80	
				15	–	25	50	
Address to Output, t_{PZH} (Turn-ON to High Level)			20	5	–	350	700	
				10	–	135	270	
				15	–	90	180	
Propagation Delay Time: Strobe to Output, t_{PHZ} (Switch Turn-OFF)			18	5	–	165	330	
				10	–	85	170	
				15	–	70	140	
Data-In to Output, t_{PZL} (Turn-ON to Low Level)			19	5	–	210	420	
				10	–	110	220	
				15	–	100	200	
Address to Output, t_{PHZ} (Turn-OFF)			20	5	–	435	870	
				10	–	210	420	
				15	–	160	320	
Minimum Setup Time, Data-In to Strobe, Address, t_{SU}				5	–	95	190	ns
				10	–	25	50	
				15	–	15	30	
Minimum Hold Time, Data-In to Strobe, Address, t_H				5	–	180	360	ns
				10	–	110	220	
				15	–	35	70	
Maximum Switching Frequency, f_ϕ	R_L=1kΩ, C_L=50 pF t_r, t_f = 20 ns			5	0.6	1.2	–	MHz
				10	1.6	3.2	–	
				15	2.5	5	–	
Minimum Strobe Pulse Width, t_W				5	–	300	600	ns
				10	–	120	240	
				15	–	90	180	
Control Crosstalk, Data-In, Address, or Strobe to Output	–	10	10	10	–	75	–	mV (peak)
	Square wave input t_r, t_f = 20 ns							
Input Capacitance, C_{IN}	Any Control Input			–	–	5	7.5	pF

● Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$

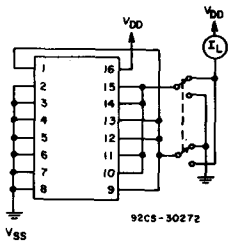


Fig. 14 – OFF switch input or output leakage current test circuit.

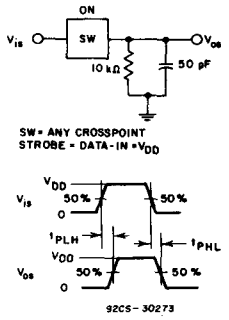


Fig. 15 – Propagation delay time test circuit and waveforms (signal input to signal output, switch ON).

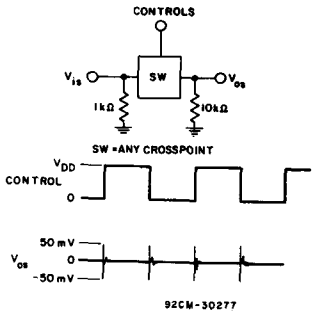


Fig. 16– Test circuit and waveforms for crosstalk (control input to signal output).

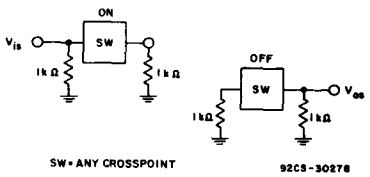


Fig. 17 – Test circuit for crosstalk between switch circuits in the same package.

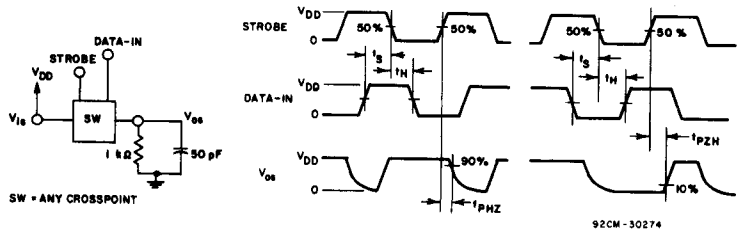


Fig. 18 — Propagation delay time test circuit and waveforms (strobe to signal output, switch Turn-ON or Turn-OFF).

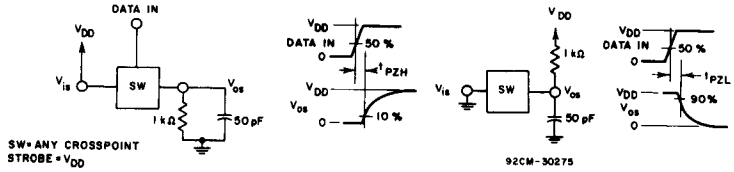


Fig. 19 — Propagation delay time test circuit and waveforms (data-in to signal output, switch Turn-ON to high or low level).

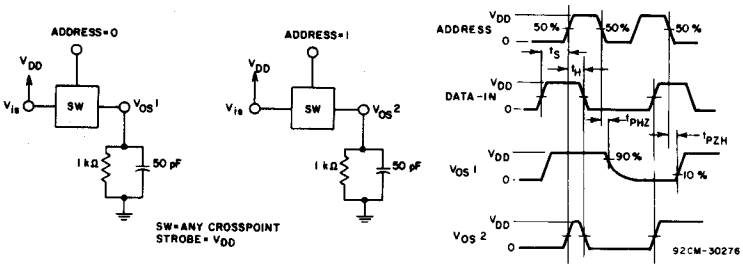
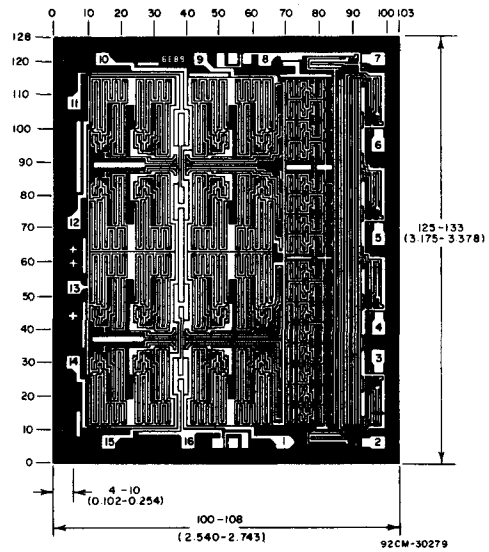


Fig. 20 — Propagation delay time test circuit and waveforms (address to signal output, switch Turn-On or Turn-OFF).



Dimensions and pad layout for CD22100H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.