CMOS 4 x 4 x 2 Crosspoint Switches With Control Memory

The RCA-CD22101 and CD22102 crosspoint switches consist of 4 x 4 x 2 arrays of crosspoints (transmission gates), 4-line to 16-line decoders, and 16 latch circuits. Any one of the sixteen crosspoint pairs can be selected by applying the appropriate four-line address, and any number of crosspoints can be *ON simultaneously*. *Corresponding* crosspoints in each array are turned on and off simultaneously, also.

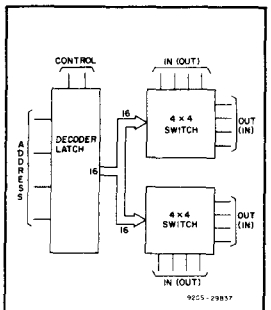
In the CD22101, the selected crosspoint pair can be turned on or off by applying a logical ONE or ZERO, respectively, to the data input, and applying a ONE to the strobe input. When the device is "powered up", the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high, data-in low, and then addressing all switches in succession.

The selected pair of crosspoints in the CD22102 is turned on by applying a logical ONE to the K_a (set) input while a logical ZERO is on the K_b input, and turned off by applying a logical ONE to the K_b (reset) input while a logical ZERO is on the K_a input. In this respect, the control latches of the CD22102 are similar to SET/RESET flip-flops. They differ, however, in that the simultaneous application of ONEs to the K_a and K_b inputs turns off (resets) all crosspoints. All crosspoints in both devices must be turned off as V_{DD} is applied.

The CD22101 and CD22102 types are supplied in 24-lead hermetic dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

- **Low ON resistance — 75 Ω typ. at V_{DD} = 12 V**
- **"Built-in" latched inputs**
- **Large analog signal capability — ± V_{DD}/2**
- **10 MHz switch bandwidth**
- **Matched switch characteristics ΔR_{ON} = 8 Ω typ. at V_{DD} = 12 V**
- **High linearity — 0.25% distortion (typ.) at f = 1 kHz, V_{IN} = 5 V_{p-p}, $V_{DD} - V_{SS}$ = 10 V, and R_l = 1 kΩ**
- **Standard CMOS noise immunity**



CD22101, CD22102
Functional Diagram

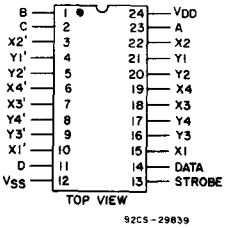
Applications:

- **Telephone systems**
- **PBX**
- **Studio audio switching**
- **Multisystem bus interconnect**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) . . . . . −0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT*. . . . . ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F) . . . . . 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) . . . . . 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

* Maximum current through transmission gates (switches) = 25 mA.

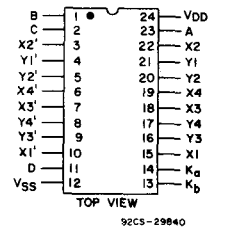


CD22101 Terminal Diagram

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V



CD22102 Terminal Diagram

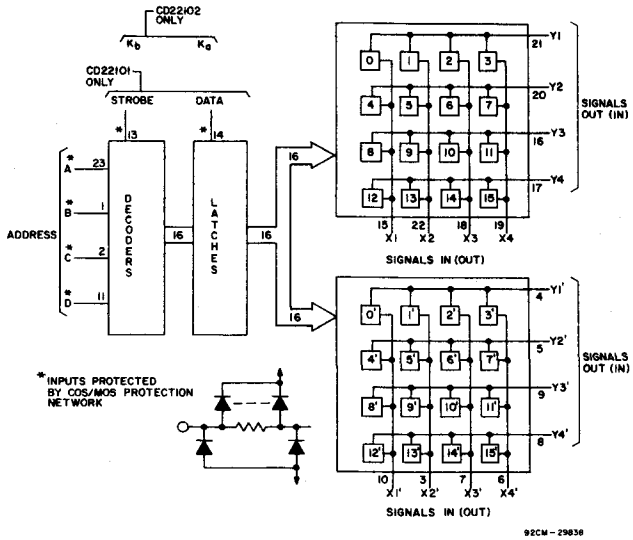


Fig. 1 – Functional block diagram.

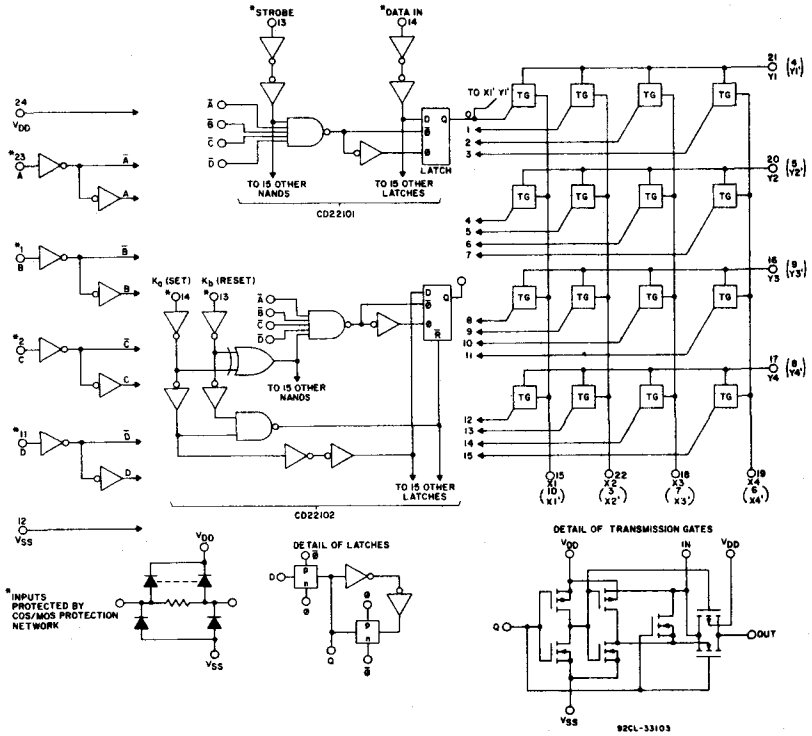


Fig. 2 – Logic diagram.

DECODER TRUTH TABLE

Address				Select	Address				Select
A	B	C	D		A	B	C	D	
0	0	0	0	X1Y1 & X1′Y1′	0	0	0	1	X1Y3 & X1′Y3′
1	0	0	0	X2Y1 & X2′Y1′	1	0	0	1	X2Y3 & X2′Y3′
0	1	0	0	X3Y1 & X3′Y1′	0	1	0	1	X3Y3 & X3′Y3′
1	1	0	0	X4Y1 & X4′Y1′	1	1	0	1	X4Y3 & X4′Y3′
0	0	1	0	X1Y2 & X1′Y2′	0	0	1	1	X1Y4 & X1′Y4′
1	0	1	0	X2Y2 & X2′Y2′	1	0	1	1	X2Y4 & X2′Y4′
0	1	1	0	X3Y2 & X3′Y2′	0	1	1	1	X3Y4 & X3′Y4′
1	1	1	0	X4Y2 & X4′Y2′	1	1	1	1	X4Y4 & X4′Y4′

CONTROL TRUTH TABLE FOR CD22101

Function	Address				Strobe	Data	Select
	A	B	C	D			
Switch On	1	1	1	1	1	1	15 (X4Y4) & 15′ (X4′Y4′)
Switch Off	1	1	1	1	1	0	15 (X4Y4) & 15′ (X4′Y4′)
No Change	X	X	X	X	0	X	X X X X

1 = High Level; 0 = Low Level; X = Don't Care

CONTROL TRUTH TABLE FOR CD22102

Function	Address				K_a	K_b	Select
	A	B	C	D			
Switch On	1	1	1	1	1	0	15 (X4Y4) & 15′ (X4′Y4′)
Switch Off	1	1	1	1	0	1	15 (X4Y4) & 15′ (X4′Y4′)
All Switches Off#	X	X	X	X	1	1	All
No Change	X	X	X	X	0	0	X X X X

1 = High Level; 0 = Low Level; X = Don't Care

In the event that K_a and K_b are changed from levels 1,1 to 0,0 K_b should not be allowed to go to 0 before K_a, otherwise a switch which was off will inadvertently be turned on.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at −55,+25,+125,apply to D,F,H pkg Values at −40,+25,+85,apply to E pkg							Units
		V_{IS} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
CROSSPOINTS											
Quiescent Device Current, I_{DD} Max.		–	5	5	5	150	150	–	0.04	5	μA
		–	10	10	10	300	300	–	0.04	10	
		–	15	20	20	600	600	–	0.04	20	
		–	20	100	100	3000	3000	–	0.08	100	
ON Resistance R_{ON} Max.	Any Switch V_{IS} = 0 to V_{DD}	–	5	475	500	725	800	–	225	600	Ω
		–	10	135	145	205	230	–	85	180	
		–	12	100	110	155	175	–	75	135	
		–	15	70	75	110	125	–	65	95	
ΔON Resistance, ΔR_{ON}	Between any two switches	–	5	–	–	–	–	–	25	–	Ω
		–	10	–	–	–	–	–	10	–	
		–	12	–	–	–	–	–	8	–	
		–	15	–	–	–	–	–	5	–	
OFF Leakage Current I_L Max.	All switches OFF	0,18	18	±1000				–	±1	±100*	nA
CONTROLS											
Input Low Voltage V_{IL} Max.	OFF switch I_L <0.2 μA;	–	5	1.5				–	–	1.5	V
		–	10	3				–	–	3	
		–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	ON switch see R_{ON} characteristic	–	5	3.5				3.5	–	–	
		–	10	7				7	–	–	
		–	15	11				11	–	–	
Input Current, I_{IN} Max.	Any control	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

* Determined by minimum feasible leakage measurement for automatic testing.

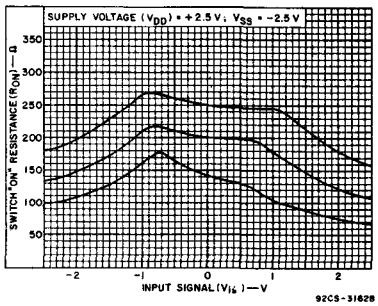


Fig. 3 – Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS} = 2.5$ V.

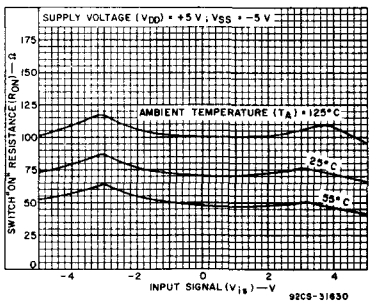


Fig. 4 – Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS} = 5$ V.

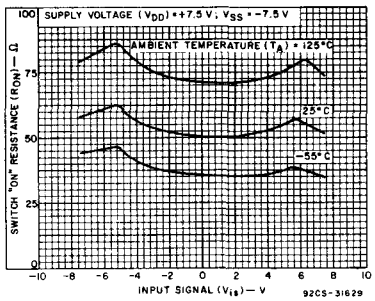


Fig. 5 – Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS} = 7.5$ V.

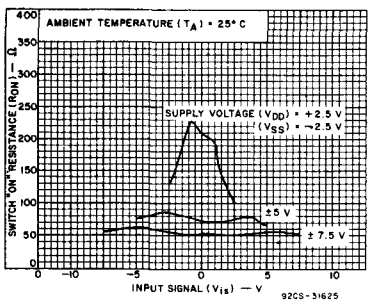


Fig. 6 – Typical ON resistance as a function of input signal voltage at $T_A = 25°C$.

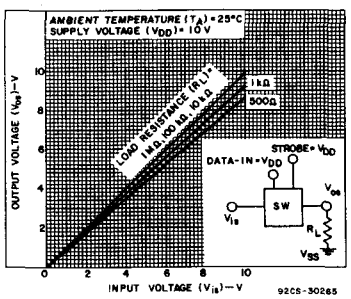


Fig. 7 – Typical switch ON transfer characteristics (1 of 16 switches).

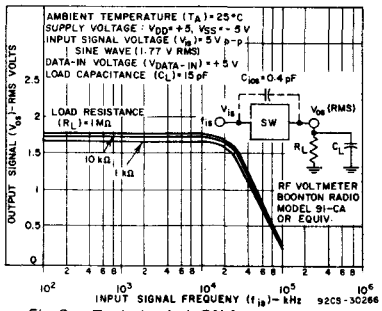


Fig. 8 – Typical switch ON frequency response characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	CONDITIONS f_{is} kHz	R_L kΩ	V_{is}● (V)	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
CROSSPOINTS								
Propagation Delay Time, (Switch ON) Signal Input to Output, t_{PHL}, t_{PLH}	–	10	5	5	–	30	60	ns
			10	10	–	15	30	
			15	15	–	10	20	
	C_L = 50 pF; t_r, t_f = 20 ns							
Frequency Response, (Any Switch ON)	1	1	5	10	–	40	–	MHz
	Sine wave input, $20 \log \frac{V_{os}}{V_{is}} = -3$ dB							
Sine Wave Response, (Distortion	1	1	2.5	5	–	1	–	%
	1	1	5	10	–	0.25	–	
	1	1	7.5	15	–	0.15	–	
Feedthrough All Switches OFF (See Fig. 24)	1.6	0.6	2■	10	–	–96	–	dB
	Sine wave input							
Frequency for Signal Crosstalk Attenuation of 40 dB	–	0.6	1■	10	–	2.5	–	MHz
Attenuation of 95 dB (See Fig. 23)	Sine wave input					0.1		kHz
Capacitance, X_n to Ground		–	–	–	–	25	–	pF
Y_n to Ground		–	–	–	–	60	–	
Feedthrough		–	–	–	–	0.6	–	
CONTROLS			See Fig.					
Propagation Delay Time, High Impedance to High Level or Low Level, t_{PZH}, t_{PZL} Strobe to Output, CD22101	R_L = 1 kΩ, C_L = 50 pF, t_r, t_f = 20 ns		16	5	–	500	1000	ns
				10	–	230	460	
				15	–	170	340	
Data-In to Output, CD22101			17	5	–	515	1000	
				10	–	220	440	
				15	–	170	340	
K_a to Output, CD22102				5	–	500	1000	
				10	–	215	430	
				15	–	160	320	
Address to Output, CD22101, CD22102			18	5	–	480	960	
				10	–	225	450	
				15	–	155	300	
Propagation Delay Time, High Level or Low Level to High Impedance, t_{PHZ}, t_{PLZ} Strobe to Output, CD22101			16	5	–	450	900	
				10	–	200	400	
				15	–	135	270	
K_b to Output, CD22102				5	–	450	900	
				10	–	200	400	
				15	–	130	260	
Data-In to Output, CD22101				5	–	450	900	
				10	–	165	330	
				15	–	110	220	
K_a·K_b to Output, CD22102				5	–	280	560	
				10	–	130	260	
				15	–	90	180	

● Peak-to-peak voltage symmetrical about V_{DD} unless otherwise specified. ■ RMS

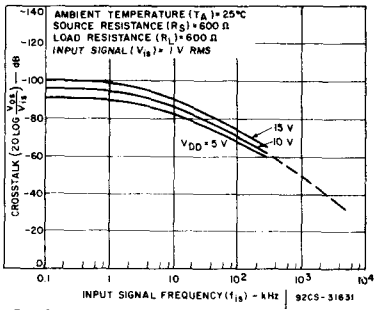


Fig. 9 — Typical crosstalk between switches as a function of signal frequency.

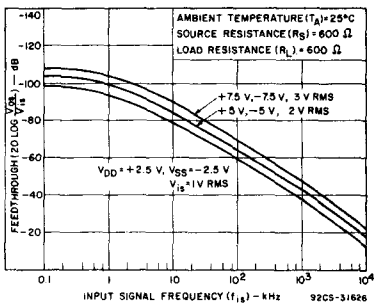


Fig. 10 — Typical feedthrough, any OFF switch as a function of frequency.

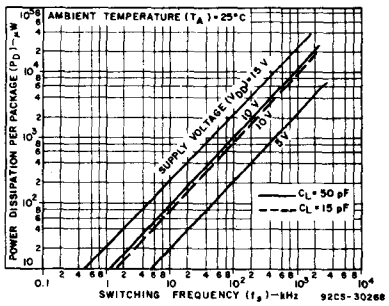


Fig. 11 — Typical dynamic power dissipation as a function of switching frequency for CD22101.

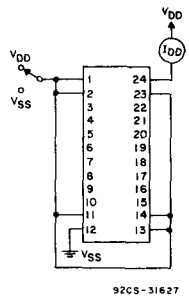


Fig. 12 — Quiescent current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)

CHARACTERISTIC	CONDITIONS				LIMITS			UNITS
	f_{is} kHz	R_L kΩ	V_{is}● (V)	V_{DD} (V)	Min.	Typ.	Max.	
CONTROLS (cont'd)			See Fig.					
Address to Output, CD22101, CD22102	R_L = 1 k, C_L = 50 pF, t_r,t_f = 20 ns		18	5	–	425	850	ns
				10	–	190	380	
				15	–	130	260	
Minimum Strobe Pulse Width t_W CD22101				5	–	260	500	
				10	–	120	240	
				15	–	80	160	
Address to Strobe Setup or Hold Times, t_{SU}, t_h, CD22101			19	5	–	−160	0	
				10	–	−70	0	
				15	–	−50	0	
Strobe to Data-In Hold Time, Time, t_{HL}; t_{LH}, CD22101			20	5	–	200	400	
				10	–	80	160	
				15	–	60	120	
Address to K_a and K_b Setup or Hold Times, t_{SU}, t_H, CD22102				5	–	−160	0	
				10	–	−70	0	
				15	–	−50	0	
Minimum K_a*K_b Pulse Width, t_W CD22102				5	–	375	750	
				10	–	160	320	
				15	–	110	220	
Minimum K_a Pulse Width, t_W CD22102				5	–	425	850	
				10	–	175	350	
				15	–	120	240	
Minimum K_b Pulse Width, t_W CD22102				5	–	200	400	
				10	–	90	180	
				15	–	70	140	
Control Crosstalk, Data-In, Address, or Strobe to Output,	100	10	21	5	–	75	–	mv (peak)
	Square wave input = 5 V, t_r,t_f=20 ns, R_s=1kΩ							
Input Capacitance, C_{IN}	Any Control Input			–	–	5	7.5	pF

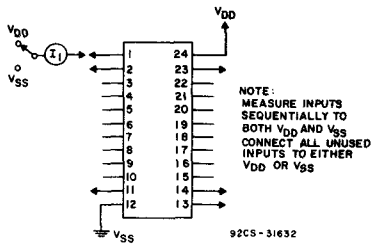


Fig. 13 – Input current test circuit.

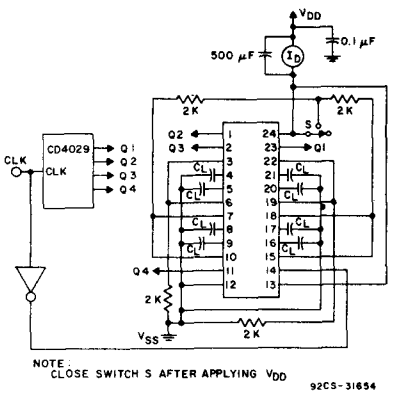


Fig. 14 – Dynamic power dissipation test circuit for CD22101.

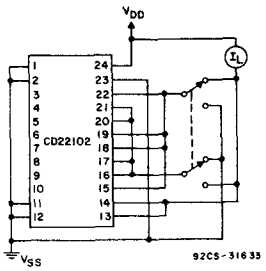


Fig. 15 – OFF switch input or output leakage current test circuit (16 of 32 switches).

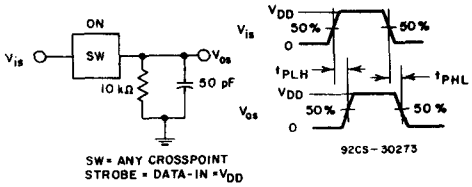


Fig. 16 – Propagation delay time test circuit and waveforms (signal input to signal output, switch ON).

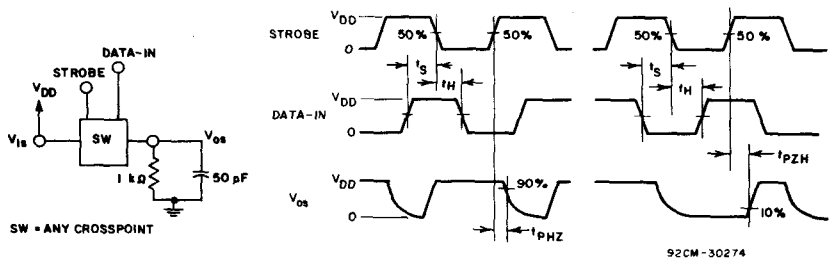


Fig. 17 – Propagation delay time test circuit and waveforms (strobe to signal output, switch Turn-ON or Turn-OFF).

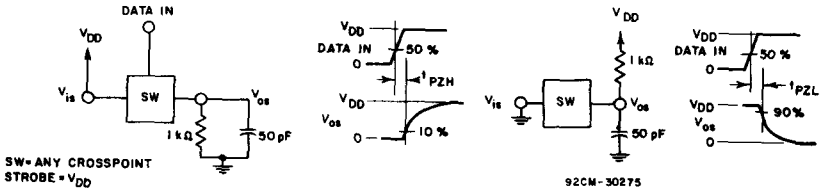


Fig. 18 – Propagation delay time test circuit and waveforms (data-in to signal output, switch Turn-ON to high or low level).

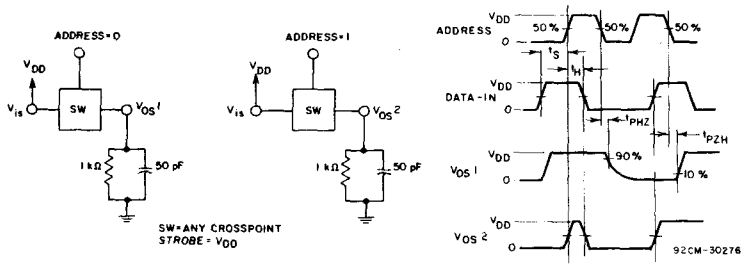


Fig. 19 – Propagation delay time test circuit and waveforms (address to signal output, switch turn-ON or Turn-OFF).

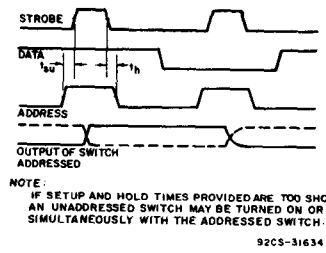


Fig. 20 – Address to strobe setup and hold times.

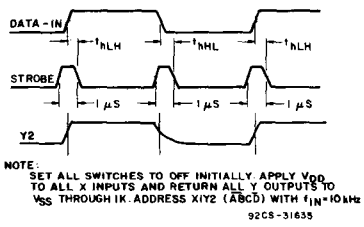


Fig. 21 – Strobe to Data-In hold time t_h, for CD22101.

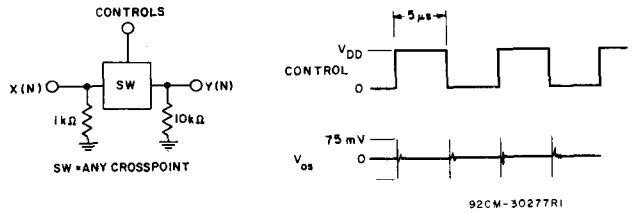


Fig. 22 – Test circuit and waveforms for crosstalk (control input to signal output).

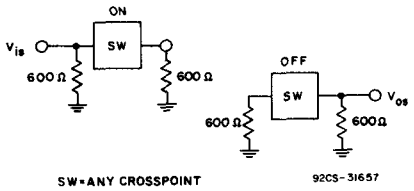


Fig. 23 – Test circuit for crosstalk between switch circuits in the same package.

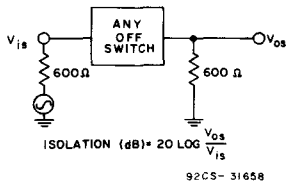
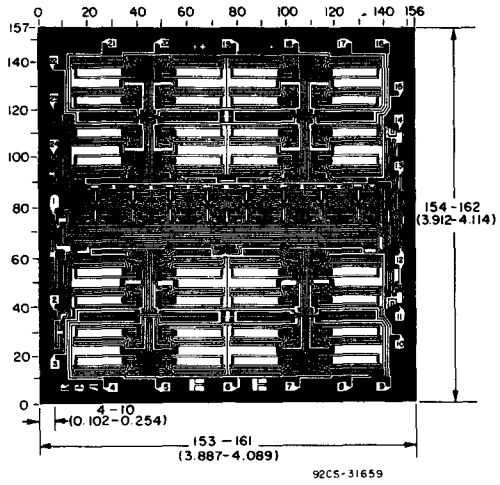
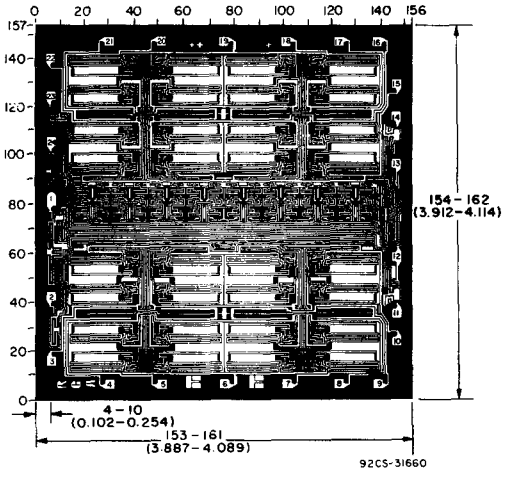


Fig. 24 – Test circuit for feedthrough (any OFF switch).



Dimensions and pad layout for CD22101H.



Dimensions and pad layout for CD22102H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.