CD22301
PCM Line Repeater

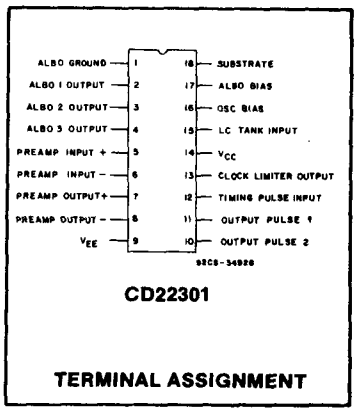
Preliminary Data

Features:

- *Automatic line buildout*
- *5.1 V supply voltage*
- *Buffered output*

Applications:

- *T1 1.544 Mbits/s bipolar carrier system*
- *T148 2.37 Mbits/s ternary carrier system*



CD22301

TERMINAL ASSIGNMENT

The RCA-CD22301 monolithic PCM repeater circuit is designed for T1 carrier systems operating with a bipolar pulse train of 1.544 Mbits/s. It can also be used in the T148 carrier system operating with a ternary pulse train of 2.37 Mbits/s. The circuit operates from a 5.1 V ± 5 % externally regulated supply.

The CD22301 provides active circuitry to perform all functions of signal equalization and amplification, automatic line buildout (ALBO), threshold detection, clock extraction, pulse timing, and buffered output formation.

The CD22301 is supplied in an 18-lead dual-in-line plastic package (E suffix).

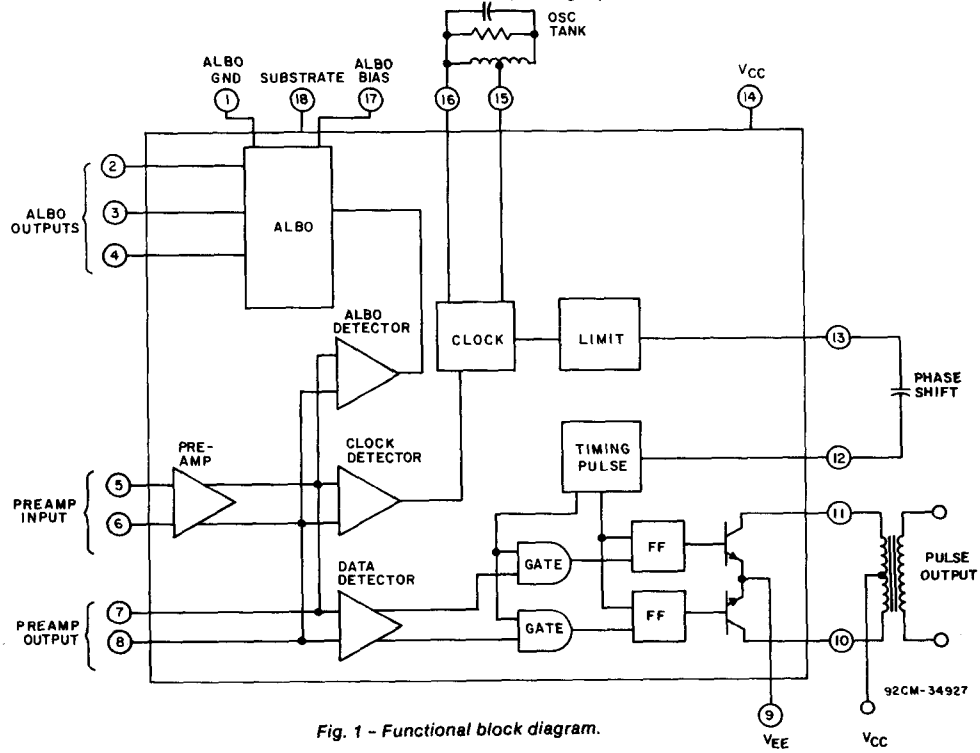


Fig. 1 - Functional block diagram.

MAXIMUM RATINGS, *Absolute Maximum Values:*

At ambient temperature (T_A) = 25°C

DC SUPPLY ..... 10 V
DC CURRENT (Into Pin 9 or 10) ..... 25 mA
PEAK CURRENT (Into Pin 9 or 10) ..... 100 mA
INPUT SURGE VOLTAGE (Between Pins 5 and 6, t = 10 ms) ..... 50 V
OUTPUT SURGE VOLTAGE (Between Pins 10 and 11, t = 1 ms) ..... 50 V
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to +60°C ..... 500 mW
For T_A = +60°C to +85°C ..... Derate linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = Full Package-Temperature Range ..... 100 mW
OPERATING TEMPERATURE RANGE (T_A) ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max. ..... +256°C

STATIC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5.1 V ± 5% (See Fig. 2)

CHARACTERISTIC	LIMITS			UNITS
	Min.	Typ.	Max.	
DC VOLTAGES				
Pins 2, 3, 4 and 17	—	0	0.1	V
Pins 5, 6, 7 and 8	2.4	2.9	3.4	V
Pins 10 and 11	—	5.1	—	V
Pins 12, 13, 15 and 16	3.1	3.6	4.1	V
DC CURRENTS				
Pin 14	—	22	30	mA
Pins 10 and 11	—	0	100	μA

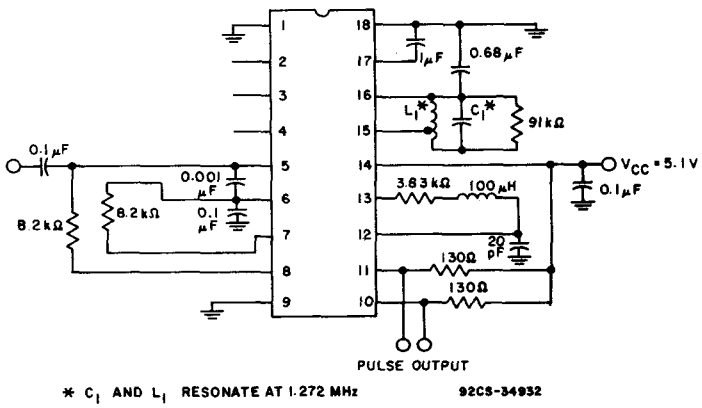


Fig. 2 - DC and output pulse test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5.1 V ± 5%

CHARACTERISTIC	SYMBOL	FIG.	NOTE	LIMITS			UNITS
				MIN.	TYP.	MAX.	
Preamplifier Input Imedance	Z_{in}	3		20	—	—	kΩ
Preamplifier Output Impedance	Z_{out}	3		—	—	2	kΩ
Preamplifier Gain @ 2.37 MHz	A_o	3		47	50	—	dB
Preamplifier Output Offset Voltage	ΔV_{out}	3	1	-50	0	50	mV
Clock Limiter Input Impedance	$Z_{in}(CL)$	4	2	10	—	—	kΩ
ALBO Off Impedance	$Z_{ALBO}(off)$	4	3	20	—	—	kΩ
ALBO On Impedance	$Z_{ALBO}(on)$	4	4	—	—	10	Ω
DATA Threshold Voltage	$V_{TH}(D)$	5	5, 8	0.75	0.8	0.85	V
CLOCK Threshold Voltage	$V_{TH}(CL)$	5	6, 8	—	1.12	—	V
ALBO Threshold	$V_{TH}(AL)$	5	7, 8	1.5	1.6	1.7	V
$V_{TH}(D)$ as % of $V_{TH}(AL)$				42	45	49	%
$V_{TH}(CL)$ as % of $V_{TH}(AL)$				65	70	75	%
Buffer Gate Voltage (low)	V_{OL}	2	9	0.65	0.8	0.95	V
Differential Buffer Gate Voltage	ΔV_{OL}	2	9	-0.15	0	0.15	V
Output Pulse Rise Time	t_r	2, 6	9, 10	—	—	40	ns
Output Pulse Fall Time	t_f	2, 6	9, 10	—	—	40	ns
Output Pulse Width	t_w	2, 6	9, 10	290	324	340	ns
Pulse Width Differential	Δt_w	2, 6	9, 10	-10	0	10	ns
Clock Drive Current	I_{CL}			—	2	—	mA

Notes:

1. No signal input. Measure voltage between pins 7 and 8.
2. Measure clock limiter input impedance at pin 15.
3. Adjust potentiometer for 0 volts. Measure ALBO off impedances from pins 2, 3 and 4 to pin 1.
4. Increase potentiometer until voltage at pin 17 = 2 Vdc. Measure ALBO on impedances from pins 2, 3 and 4 to pin 1.
5. Adjust potentiometer for ΔV = 0 volts. Then slowly increase ΔV in the positive direction until pulses are observed at the DATA terminal.
6. Continue increasing ΔV until the DC level at the clock terminal drops to 4 volts.
7. Continue increasing ΔV until the ALBO terminal rises to 1 volt.
8. Turn potentiometer in the opposite direction and measure negative threshold voltages by repeating tests outlined in notes 5, 6 and 7.
9. Set e_{in} = 2.75 mV(rms) at f ≈ 1.185 MHz. Adjust frequency until maximum amplitude is obtained at pin 15. Observe output pulses at pins 10 and 11.
10. Adjust input signal amplitude until pulses just appear in outputs. Increase input amplitude by three dB.

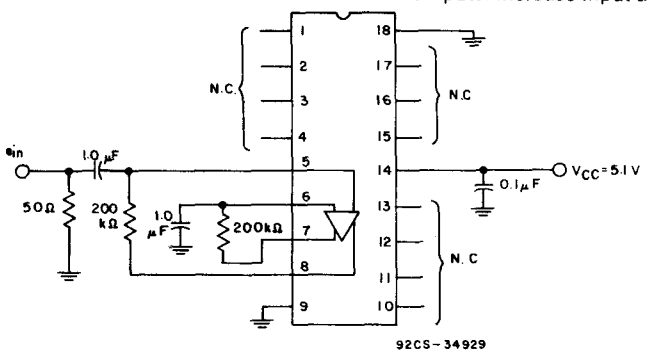


Fig. 3 - Preamplifier gain and impedance measurement circuit.

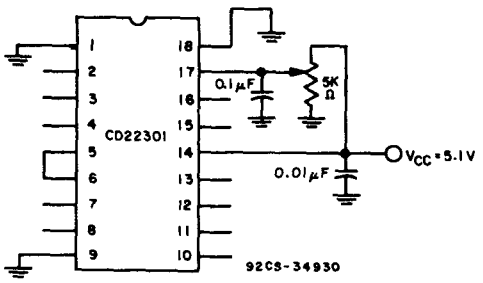


Fig. 4 – Test circuit for impedance measurement.

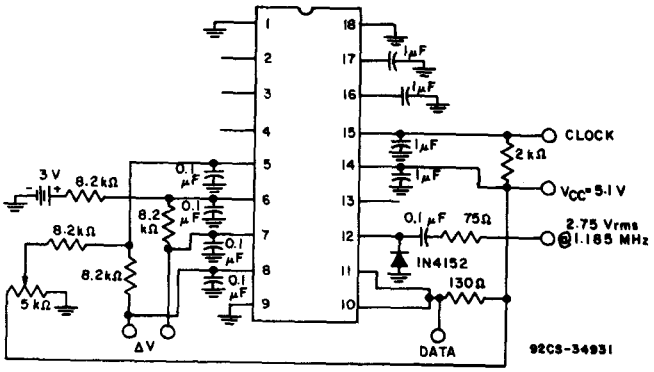


Fig. 5 – Test circuit for threshold voltage measurement.

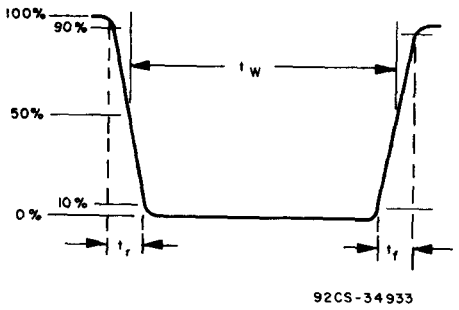


Fig. 6 – Output pulse waveform.