CMOS 16-Channel Precision Timer/Driver

Features:

- *Provides 17 precision-timed output pulses*
- *Variable output pulse width as a function of an external timer clock frequency*
- *High source current drive output pulses- up to 15 mA using bipolar drivers*
- *Serial data interface via shift register*
- *EP inputs provide added control logic flexibility for output selection in addition to shift register data*
- *Static operation- shift register and timers can operate at DC and still retain counts and data levels*
- *For multiple device use, shift registers can be cascaded*
- *Provides inherent serial-to-parallel data conversion*
- *Offers output disable capability using inhibit features*
- *Low power CMOS logic*
- *Input/output protection circuitry*

"E" Suffix

40-Lead Dual-In-Line Plastic Package

H-1892

The RCA CD22401 is a precision timer/driver. It is an interface circuit and has been designed to provide critically timed output pulses for high-speed printers. The device is fabricated using CMOS enhancement-mode technology with the resulting low power consumption.

The circuit consists of a 16-stage (optionally 17) shift register with each register output connected to a latch and its respective timer and output buffer stage. Thus, there are 17 latches, timers, and driver (output buffer) stages. The output driver pulse width is a function of the timer clock frequency, since it depends upon a fixed count in hardware.

Data is fed serially into the shift register by means of the shift register clock. Then the input sequence is strobed out in parallel to the shift register latch. A particular output is turned on (pulsed high) if the associated latch holds a logic "1" and when the proper enable signal is activated. Simultaneously, the enable signal starts the associated timer which controls the output pulse width. After a time period of 100 negative edges of the clock (99 to 100 clock pulses), the output is turned off. This provides timing accuracy within 1%.

The CD22401 is supplied in the 40-lead dual-in-line plastic package (E suffix) and in chip form (H suffix). It is useful in applications requiring precision pulse widths.

Register Operation

In operation, a serial string of 16 (17 using the optional flip-flop) bits is fed into the shift register (see Fig. 4 for shift register timing). Ones ("1s") determine an output drive pulse and zeros ("0s") indicate no drive. Any one output enable (EP) line is connected to four selected timers giving the potential for four outputs per one $\overline{EP}$ pulse with the exception that $\overline{EP5}$ connects one timer only. EP lines may be connected to each other.

After a sequence of 16 bits (or 17) is serially loaded into the shift register, a strobe pulse activates the latch so that the register data "word" is transferred out in parallel into the register latch. Here the data waits until an active enable signal combines with a "one" from any latch at which time the counter begins and the respective output driver goes high. The output will continue high until the counter achieves 100 negative edges. It has been assumed that the output inhibit control has not been activated. The inhibit is a control which gates the output "OFF" and can thereby prevent start-up or transient situations.

The register latch has 17 outputs each of which feeds its respective timer (one timer circuit for each output from the register latch). Also, each timer provides access to an output driver.

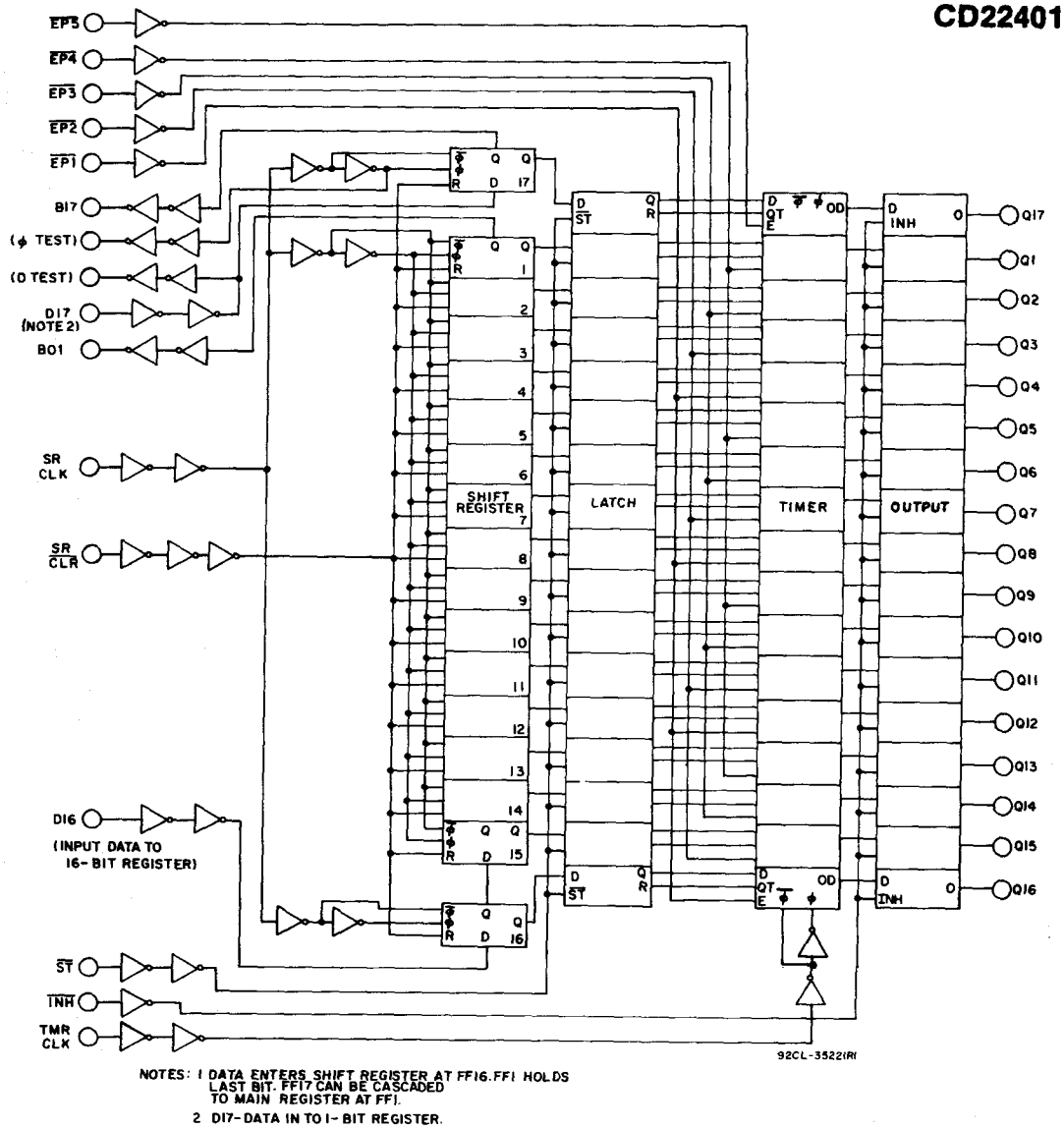
Timer Operation

When the timer begins counting and the output goes high, the latch is held reset to prevent retriggering before the count is finished.

During start-up (before reliable count operation), the timers need 128 clock pulses at the timer inputs to guarantee a reset condition before enable pulses are applied.

After an output pulse goes low (becomes inactive), seven clock pulses should be applied at the timer clock input before any timer is retriggered by means of an enable and data "one" combination (repeat of another output pulse at same pin).

The data and the enable pulses together control which combination of timers and driver stages become activated to produce output pulses.



NOTES: 1 DATA ENTERS SHIFT REGISTER AT FF16.FF1 HOLDS LAST BIT. FF17 CAN BE CASCADED TO MAIN REGISTER AT FF1.
2 DI7-DATA IN TO 1-BIT REGISTER.

Fig. 1 - CD22401 block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal) ..... -0.5 to 6.5 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = 0°C to 70°C (PACKAGE TYPE E) ..... 500 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... 0°C to 70°C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

CD22401

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

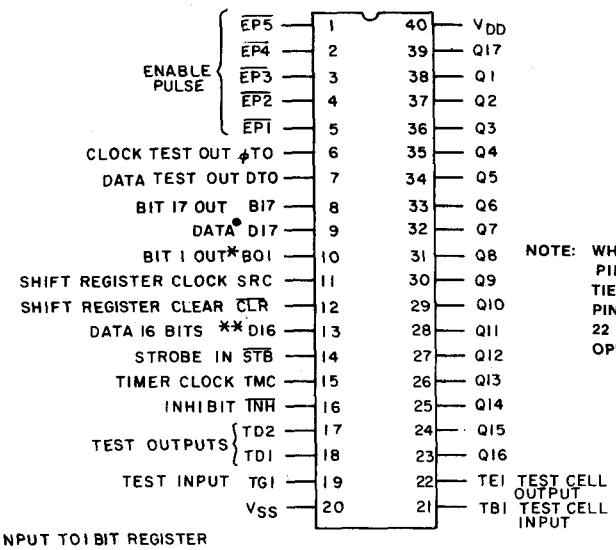
CHARACTERISTIC	LIMITS		UNITS
	V_{DD}	V_{SS}	
Supply Voltage Range (For T_A = Full Package Temperature Range)	5	0	V

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V

CHARACTERISTIC		CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Input Low Voltage	V_{IL}		—	—	0.8	V
Input High Voltage	V_{IH}		2.4	—	—	
Output Voltage Low-Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	—	—	—	
		I_{OL} = 0 μA *	—	—	0.05	
		I_{OL} = 1.6 mA ‡	—	—	0.4	
		I_{OL} = 1 mA *	—	—	0.5	
Output Voltage High Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	—	—	—	
		I_{OH} = 0 μA *	3.5	—	—	
		I_{OH} = 5 mA *	3.2	—	—	
		I_{OH} = 10 mA *	2.5	—	—	
		I_{OH} = 15 mA *	2.2	—	—	
		I_{OH} = 0 μA ‡	4.9	—	—	

* Output Pins 23-39

‡ Output Pins 8, 10



NOTE: WHEN USING CD22401 PIN 19 SHOULD BE TIED TO V_{SS} (OR V_{DD}). PINS 6,7,17,18,21, AND 22 SHOULD BE LEFT OPEN.

•INPUT TO1 BIT REGISTER

*OUTPUT OF 16 BIT REGISTER

**INPUT TO 16 BIT REGISTER

92CS-35201RI

TERMINAL ASSIGNMENT

DYNAMIC ELECTRICAL CHARACTERISTICS At T_A = 25° C, Input t_r, t_f = 20 ns, C_L = 50 pF

CHARACTERISTIC		FIG.	TEST CONDITIONS		LIMITS			UNITS
			V_{DD}(V)	C_L	Min.	Typ.	Max.	
Timer Clock Frequency	t_{rTCL}	3	5	—	0	0.7	1	MHz
Timer Clock Pulse Width	t_{WTCL}	3	5	—	500	—	—	nsec
Timer Clock Rise and Fall Time	t_{rCK}, t_{fCK}	5	5	—	—	—	2	μsec
Output Inhibit Pulse Width	t_{WOI}	5	5	—	500	—	—	nsec
Inhibit Output Turn-Off Delay	t_{PHLI}	5	5	50	—	—	550	nsec
Output Turn-On Delay after Inhibit is OFF	t_{PLHI}	5	5	50	—	—	550	nsec
Enable Pulse (EP) Width	t_{WHEP}	3	5	—	500	—	—	nsec
Transfer Strobe Pulse Width *	t_{WTS}	3	5	—	350	—	—	nsec
Output L-H Transition Time	t_{TLH}	5	4.5	50	—	—	85	nsec
Output H-L Transition Time	t_{THL}	5	4.5	50	—	—	150	nsec
Output Turn-On Prop. Delay Time	t_{PLH}	5	4.5	50	—	—	1200	nsec
Output Turn-Off Prop. Delay Time	t_{PHL}	5	4.5	50	—	—	1200	nsec
High-Level Output Driver Pulse Width	t_{out}	3	4.5	50	99	—	100	Timer Clock Pulses
Shift Register Input Clock Frequency	t_{fSRCL}	2, 4	5	—	—	2	2.5	MHz
Shift Register Clock Pulse Width	t_{WSRCL}	2	5	—	200	—	—	nsec
Shift Register Data Set-Up Time	t_{setup}	2	5	—	100	—	—	nsec
Shift Register Data Hold Time	t_{SRHOLD}	2	5	—	200	—	—	nsec
Shift Register Data Pulse Width	t_{WSRD}	2	5	—	300	—	—	nsec
Shift Register Data Output Prop. Delay Time	t_{PDLH}	2	5	50	—	—	200	nsec
Shift Register Clear Pulse Width	t_{SRCLR}	2	5	—	200	—	—	nsec

* Data from shift register must be stable at time of transfer.

AC Waveforms

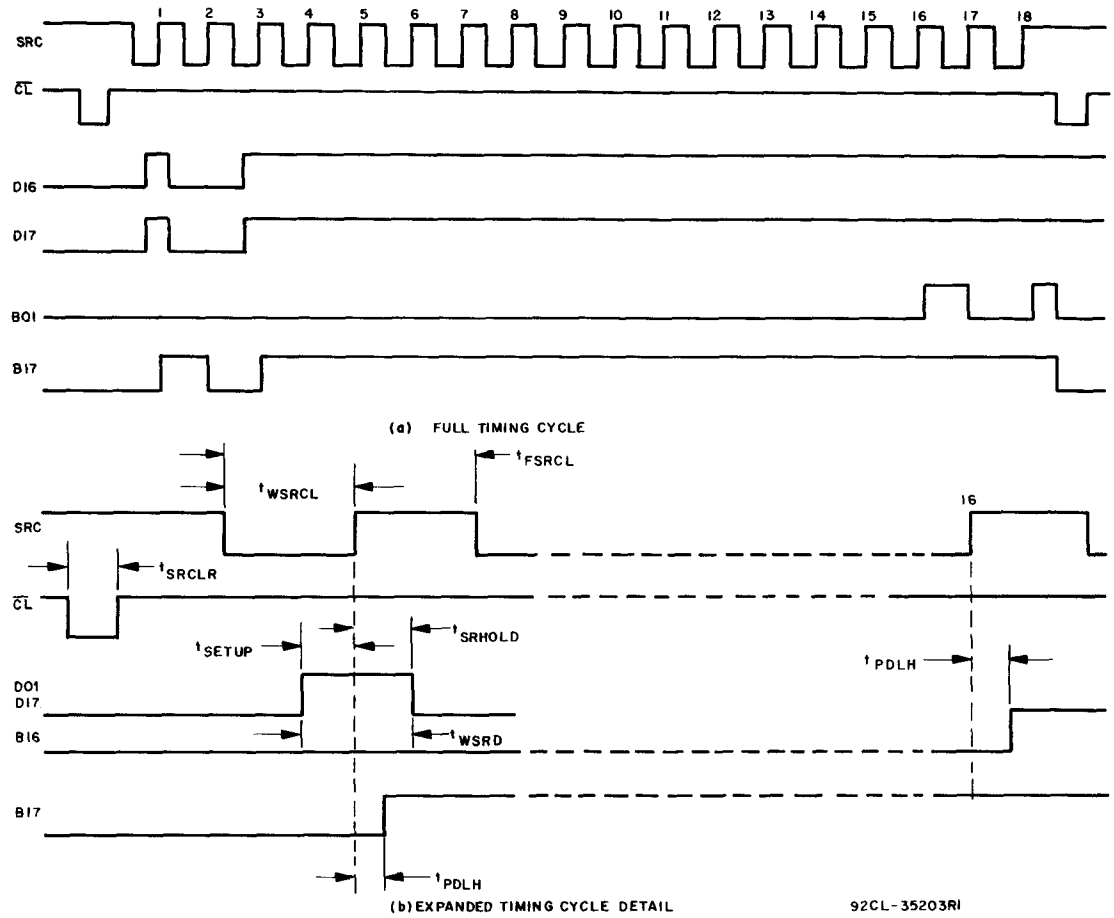


Fig. 2 - Functional timing diagram-shift registers function.

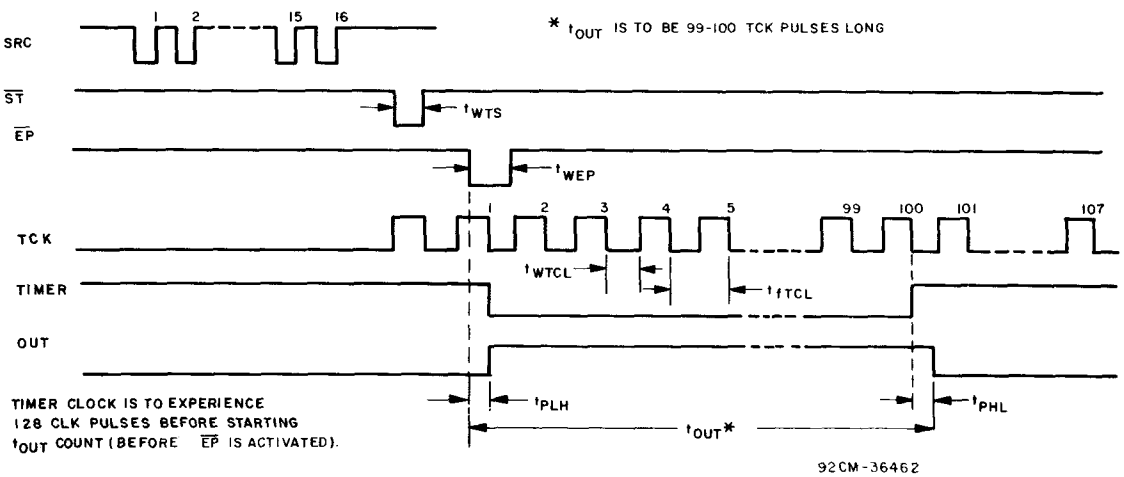


Fig. 3 - Functional timing diagram-shift registers function.

AC Waveforms (cont'd)

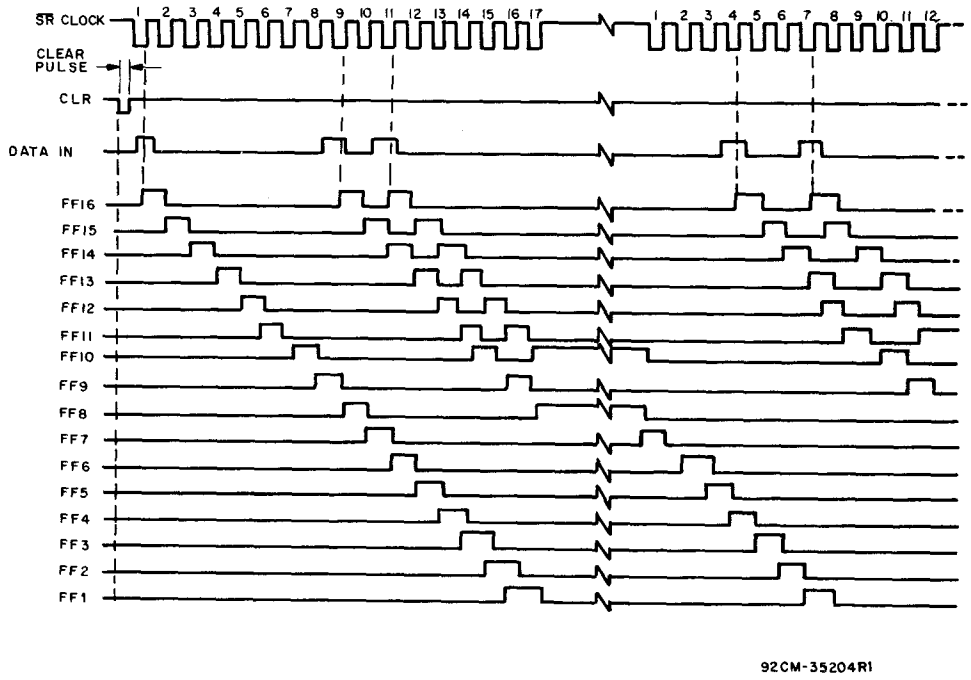


Fig. 4 - Functional timing diagram-shift registers function.

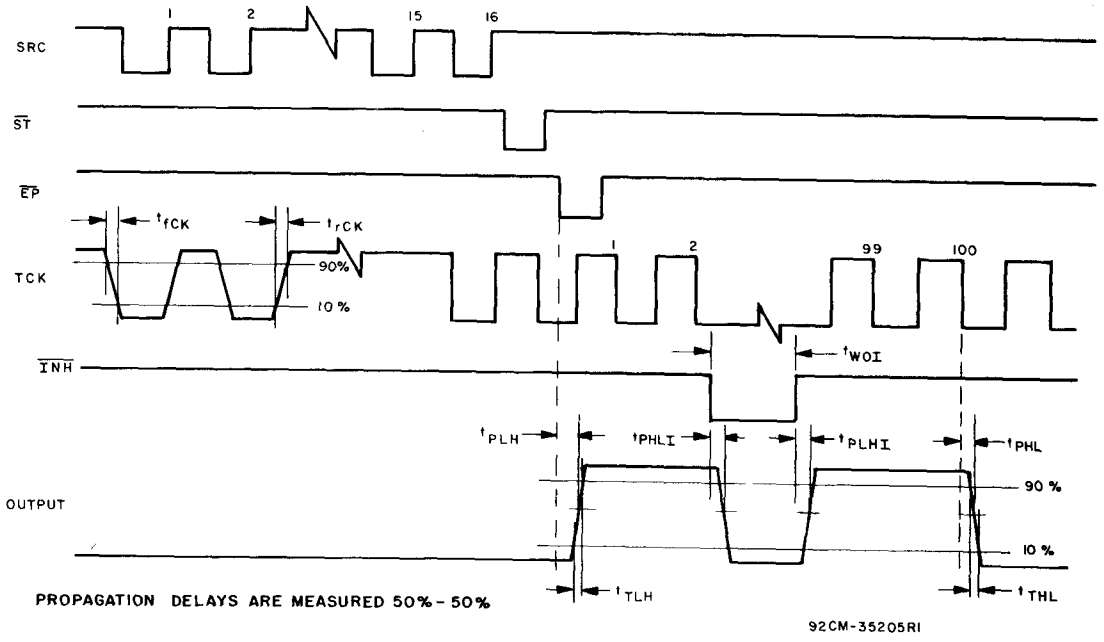


Fig. 5 - Functional timing diagram-shift register function detail.