CMOS Pulse Code Modulation Sampled — Data Filters

Preliminary Data

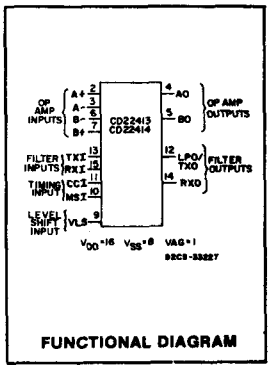
The RCA-CD22413 and CD22414 are sampled-data, switched-capacitor filters intended for use in PCM CODEC systems or other telecommunication systems requiring band limiting. Transmit and receive filters in both devices are 5-pole elliptical types, operating at a sample rate of 128 kHz. In addition, the CD22413 contains a 3-pole Chebyshev high-pass filter in the transmit section that provides 50/60 Hz and 15 Hz rejection. Both devices also include two operational amplifiers which may be used as building blocks in a system.

A 50% duty-cycle clock on the convert-clock input (CCI) determines the cutoff frequencies for the filters. The cutoff frequency (f_o) is given by the equation; f_o = 0.02422 X Clock Frequency. Normally, the clock frequency is 128 kHz for a cutoff frequency of 3100 Hz. The master sync input (MSI) should be 8 kHz and have it's low-to-high transition coincide with each new PAM sample received at Receive-Filter-In (RXI). RXI will accept 19% to 100% duty cycle PAM at 8 kHz.

Timing and synchronization signals (CCI and MSI) may be made either TTL- or CMOS-compatible through use of the Logic-Shift Voltage (VLS) input. Specific input conditions are listed in the table of Logic-Shift-Voltage inputs. The analog ground (VAG) should be held at approximately (V_{DD}-V_{SS})/2. If VAG is within one volt of V_{DD2} the chip will be powered down. The CD22413 is pin-compatible with the MC14413; the CD22414 is pin-compatible with the MC14414.

The CD22413 and CD22414 are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffix), 16-lead dual-in-line plastic packages (E suffix), and chip form (H suffix).

Features:
- *Single supply (10V-16V) or dual supply operation*
- *Transmit bandpass and receive low pass filters (CD22413)*
- *Transmit and receive low pass filters (CD22414)*
- *30 mW (typ.) operating power*



FUNCTIONAL DIAGRAM

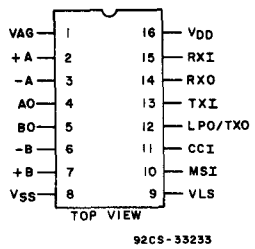
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +18 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPES D, F, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Terminal Designation	LIMITS			UNITS
		Min.	Typ.	Max.	
DC Supply Voltage (For T_A = Full Package Temperature Range)	V_{DD} - V_{SS}	10	12	16	Vdc
Convert Clock Frequency	CCI	50	128	400	kHz
Master Sync Frequency	MSI	—	8	32	



TERMINAL ASSIGNMENTS

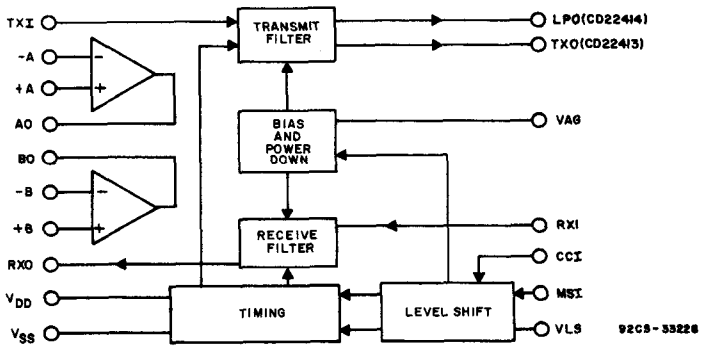


Fig. 1 - Block diagram of CD22413 and CD22414.

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V, T_A = 25°C)

CHARACTERISTIC		V_{DD} Vdc	LIMITS Min.	Typ.	Max.	UNITS
Operating Current	I	12	—	2.5	3.5	mA
Power-Down Current, (PDI = V_{SS})	I_{PD}	12	—	10	50	μA
Input Capacitance	C_{IN}	12	—	5	7.5	pF

MODE CONTROL LOGIC LEVELS

CHARACTERISTIC		V_{DD} Vdc	LIMITS Min.	Typ.	Max.	UNITS
VLS Power-Down Mode	V_{IH}	12	11	—	—	V
		15	14	—	—	
VLS TTL Mode		12	2	—	10	V
		15	2	—	13	
VLS CMOS Mode	V_{IL}	12	—	—	0.8	V
		15	—	—	0.8	
VAG Power-Down Mode	V_{IH}	12	11	—	—	V
		15	14	—	—	
VAG Analog-Ground Mode	V_{IL}	12	—	—	8	V
		15	—	—	11	

CMOS LOGIC LEVELS (VLS = V_{SS})

CHARACTERISTIC		V_{DD} Vdc	LIMITS Min.	Typ.	Max.	UNITS
Input Current	I_{IN}					
CCI		12	—	±0.00001	±0.3	μA
MSI "1" Level		—	—	30	—	
(Internal Pulldown Resistors) "0" Level		—	—	−0.00001	−0.3	
Input Voltage CCI, MSI						
"0" Level	V_{IL}	12	—	5.25	3.6	V
		15	—	6.75	4	
"1" Level	V_{IH}	12	8.4	6.75	—	
		15	11	8.25	—	

TTL LOGIC LEVELS (VLS = 6 V, V_{SS} = 0 V)

CHARACTERISTIC		V_{DD} Vdc	LIMITS Min.	Typ.	Max.	UNITS
Input Current	I_{IN}					
CCI		12	—	±0.00001	±0.3	μA
MSI "1" Level		—	—	3	—	
(Internal Pulldown Resistor) "0" Level		—	—	−0.00001	−0.3	
Input Voltage CCI, MSI						
"0" Level	V_{IL}	12	—	—	VLS +0.8	V
"1" Level	V_{IH}	12	VLS+2	—	—	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V, T_A = 25° C)

CHARACTERISTIC		LIMITS Min.	Typ.	Max.	UNITS
Input Current, (RXI, TXI, VAG)	I_{IN}	—	±0.00001	±0.03	μA
AC Input Impedance (1 kHz) (RXI, TXI, VAG)	Z_{IN}	—	2	—	MΩ
Input Common Mode Voltage Range (TXI, RXI, +A, −A, +B, −B)	V_{ICR}	1.5	—	10.5	V
Input Offset Current (+A to −A, +B to −B)	I_{IO}	—	±10	—	nA
Input Bias Current (+A, −A, +B, −B)	I_{IB}	—	±0.10	±1	nA
Input Offset Voltage (+A to −A, +B to −B)	V_{IO}	—	±10	±25	mV
Output Voltage Range (AO, BO, TXO, LPO, RXO)	V_{OR}				
(R_L = 20 kΩ to VAG, R_B = ∞)		1.5	—	10.5	V
(R_L = 600 Ω to VAG, R_B = 1.6 kΩ to V_{DD})		4.3	—	7.9	
(R_L = 900 Ω to VAG, R_B = 1.8 kΩ to V_{DD})		4	—	8.2	
Small Signal Output Impedance (1 kHz) (TXO CD22413)	Z_O	—	50	—	Ω
(LPO CD22414)		—	50	—	
(RXO)		—	50	—	
Output Current (V_{OH} = 11V) (TXO, LPO, RXO, AO, BO)	I_{OH}	—	−400	—	μA
(V_{OL} = 1V) (TXO, LPO, RXO, AO, BO)	I_{OL}	—	5	—	mA

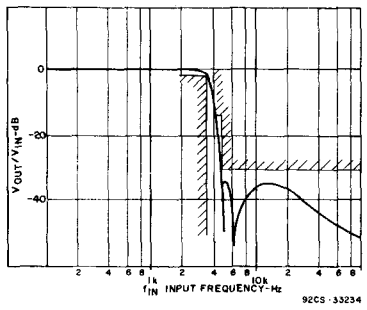


Fig. 3 - Receive filter typical and minimum performance for CD22413 or CD22414 with sinx x correction included.

RECEIVE FILTER SPECIFICATIONS (V_{DD} - V_{EE} 12V, CCI = 128 kHz, MSI = 8 kHz. includes sinx x correction, V_{in} = 0 dBm0, full scale = +3 dBm0, 7 V_{p-p}, T_A = 25°C)

CHARACTERISTIC		LIMITS Min.	Typ.	Max.	UNITS
Gain (1020 Hz)		−0.2	0	+0.2	dB
Passband Ripple (50 Hz to 300 Hz)		—	0.24	0.3	
Out of Band Rejection	See Note 1				
3400 Hz		—	−0.8	−1.5	
4000 to 4600 Hz		−14	−15.5	—	
4600 to 64 kHz		−30	−33	—	
Output Noise (RXI = VAG)	See Note 2	—	10	15	dBrnc0
Dynamic Range		78	83	—	dB
Differential Group Delay					
1150 to 2300 kHz Delay		—	12	22	μs
1000 to 2500 kHz Delay		—	25	35	
800 to 2700 kHz Delay		—	31	41	

Note 1: Referenced to passband minimum. Note 2: Referenced to 900Ω.

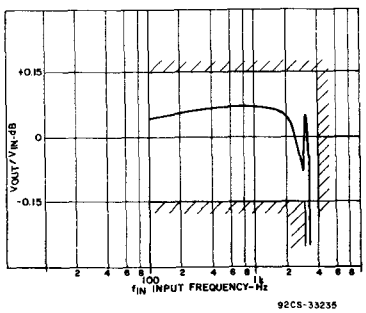


Fig. 4 - Receive filter typical and minimum passband performance for CD22413 or CD22414.

TRANSMIT FILTER SPECIFICATIONS (V_{DD}-V_{EE} = 12 V, CCI = 128 kHz MSI = 8 kHz, V_{in} = 0 dBm0, full scale = +3 dBm0, 7 V_{p-p}, T_A = 25°)

CHARACTERISTIC		LIMITS Min.	Typ.	Max.	UNITS
Gain (1020 Hz)		-0.15	—	+0.15	
Passband Ripple (300 Hz to 3000 Hz)		—	0.22	0.3	
Rejection	See Note 1				
60 Hz	CD22413 only	-20	-24	—	dB
180 Hz	CD22413 only	—	-0.6	-1	
3400 Hz		—	-0.8	-1.5	
4000 to 4600 Hz		-14	-15.5	—	
4600 to 64 kHz		-32	-33	—	
Output Noise	CD22413	—	—	—	
(300 to 3400 Hz)	CD22414	—	8	12	dBrnc0
Dynamic Range (7 Vpp Max)		81	87	—	dB
Differential Group Delay					
1150 to 2300 kHz Delay		—	12	22	μs
1000 to 2500 kHz Delay		—	25	35	
800 to 2700 kHz Delay		—	31	41	

Note 1: Referenced to passband minimum.

SWITCHING CHARACTERISTICS (V_{DD} - V_{SS} = 10 V, T_A = 25° C)

CHARACTERISTIC		LIMITS Min.	Typ.	Max.	UNITS
Input Rise and Fall Time, t_r, t_f	CCI, MSI	—	—	4	μs
Pulse Width, t_{WH}	CCI, MXI	100	50	—	ns
Clock Pulse Frequency, f_{CL}	CCI	50	—	500	kHz
Set Up Time, t_{SU} MSI Rising Edge to CCI Rising Edge (CCI = 128 kHz)*		-3	—	+3	μs

*Specifications assume use of 50% duty cycle for clocks.

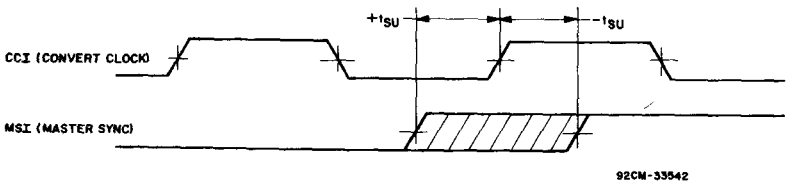


Fig. 2 - Switching characteristics wave forms.

LOGIC SHIFT VOLTAGE INPUTS

VLS PIN	LOGIC INPUT (CCI AND MSI)
VSS < VLS < VSS + 0.8V	CMOS
VDD - 1V < VLS < VDD	POWER DOWN
VSS + 2V < VLS < VDD - 2V	TTL (VLS + 0.8V < INPUT < VLS + 2V)

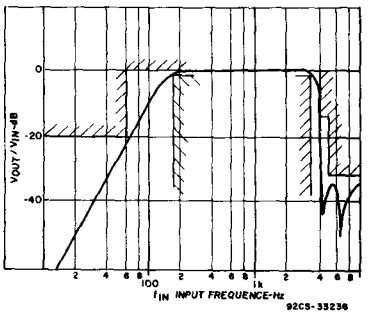


Fig. 5 - Transmit filter typical and minimum performance for CD22413 or CD22414 using Figs. 11 and 12.

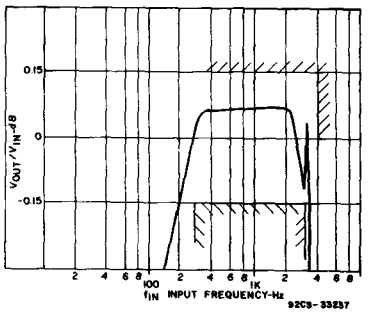


Fig. 6 - Transmit filter typical and minimum passband performance for CD22413 or CD22414 using Figs. 11 or 12.

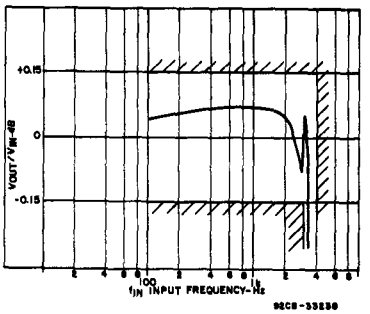


Fig. 7 - Transmit filter typical and minimum passband performance for CD22414.

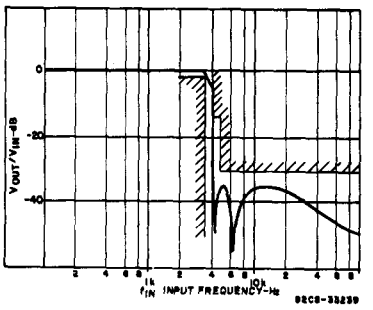


Fig. 8 - Transmit filter typical and minimum performance for CD22414.

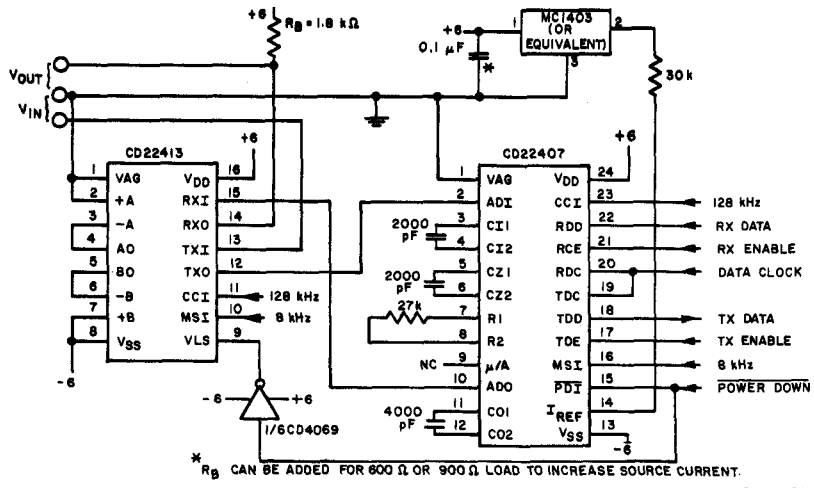


Fig. 9 - Typical circuit configuration using the CD22407 CODEC and CD22413 filter (split supply).

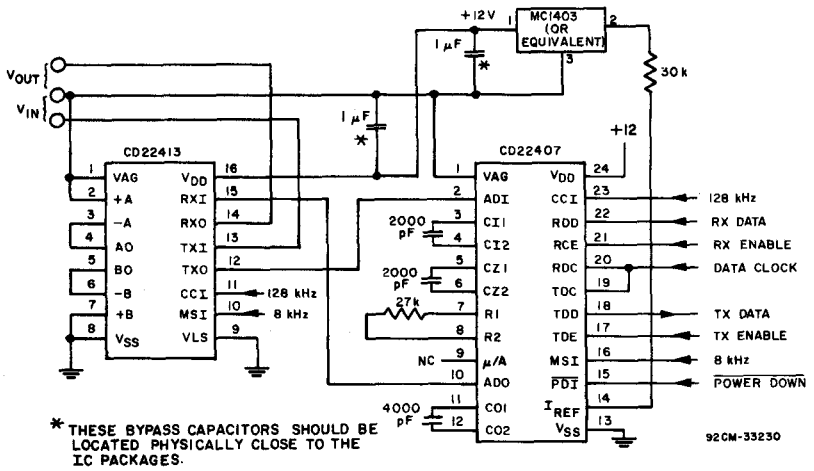


Fig. 10 - Typical circuit configuration using the CD22407 CODEC and CD22413 filter (single supply).

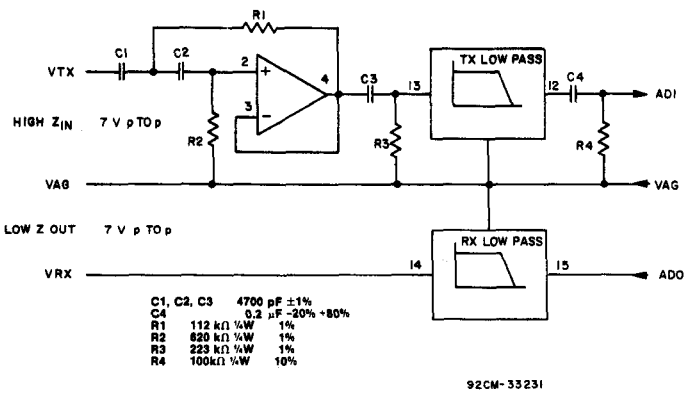


Fig. 11 - Filter schematic for CD22413 with 60-Hz reject filter.

VAG — (Analog Ground) This pin should be held at approximately (V_{DD}-V_{EE})/2. All analog inputs and outputs are referenced to this pin. If this pin is brought to within approximately 1 V of V_{DD}, the chip will be powered down.

+A Non-inverting input of op-amp A.

-A Inverting input of op-amp A.

AO Output of uncommitted op-amp A

BO Output of uncommitted op-amp B

-B Inverting input of op-amp B

+B Non-inverting input of op-amp B

V_{SS} This is the most negative supply pin and digital ground for the package.

VLS (Logic Shift Voltage) The voltage on this pin determines the logic compatability for the CCI and MSI inputs. If VLS is within 0.8 V of V_{SS}, the thresholds will be for CMOS operating between V_{DD} and V_{SS}. If VLS is within 1 V of V_{DD}, the chip will power down. If VLS is between V_{DD} - 2 V and V_{SS} 2 V, the thresholds for logic inputs at CCI and MSI will be between VLS + 0.8 V and VLS + 2 V for TTL compatability.

CCI (Convert Clock Input) Normally, a 128 kHz clock signal should be applied to this pin to operate both filters at f_o = 3100 Hz. For other break frequencies use the following equation: f_o = 0.02422 f clock.

MSI (Master Sync Input) This pin should receive a low-to-high transition concurrent with each new PAM sample received at the receive filter input, ADI. A new transmit filter output sample will be presented at this time.

TXO (Transmit Bandpass Output — CD22413) This is the output of the transmit-bandpass filter. It is 100% duty cycle PAM at 8 kHz.

LPO (Transmit Lowpass Output — (CD22414) This is the output of the transmit-lowpass filter. It is 100% duty cycle PAM at 128 kHz.

TXI (Transmit Input) This is the transmit-filter input.

RXO (Receive Output) This pin is the output of the receive filter. It is 100% duty cycle PAM at the same frequency as the CCI pin, normally 128 kHz.

RXI (Receive Input) This is the receive filter input. It will accept 3/16 to 100% duty cycle PAM at 8 kHz.

V_{DD} Nominally 12 volts.

NOTE: Both VAG and VLS are high-impedance units.

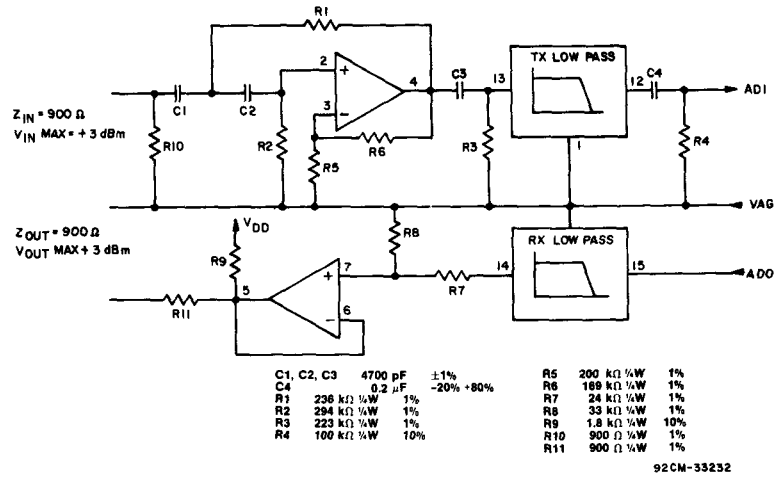


Fig. 12 - Filter schematic for CD22414 with 60-Hz rejection and 900-Ω termination.

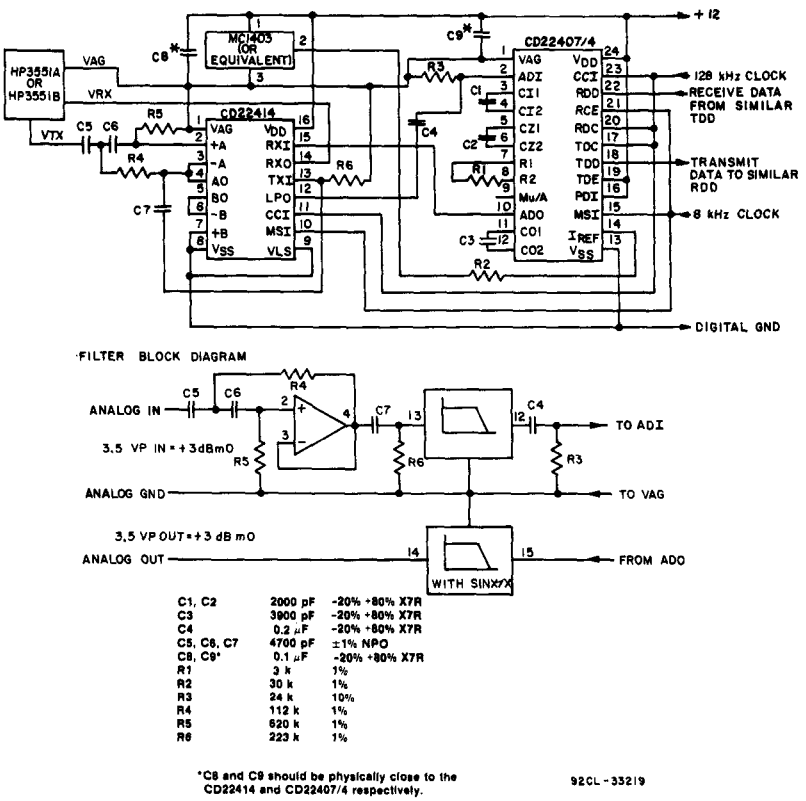


Fig. 13 - Analog transmission test circuit for CD22414 PCM filter and CD22407/CD22404 PCM CODEC.

TYPICAL END TO END PERFORMANCE OF RCA CODEC & FILTER

All measurements made using HP3779B PCM Test Set. See Fig. 13.

SPECIFICATION	Performance of CD22407/4 CODEC & CD22414 Filter	Bell System D3 Voice Freq. Requirements PUB 43801	CCITT G7.12 Voice Freq. Requirements
Channel Saturation	+3 dBm0	+3 dBm0	+3 dBm0
Gain Tracking with 1 kHz tone			
+3 to −40 dBm0	±0.3 dB	≤±0.5 dB	≤±0.5 dB
−40 to −50 dBm0	±0.6 dB	≤±1 dB	≤±1 dB
−55 dBm0	±2 dB	≤±3 dB	≤±3 dB
Quantizing Distortion @ 1 kHz			
+3 to −30 dBm0	37 dB	≥33 dB	>33 dB
−35 dBm0	34 dB	≥30 dB	≥30 dB
−40 dBm0	31 dB	≥27 dB	≥27 dB
−45 dBm0	26 dB	≥22 dB	≥22 dB
Idle Channel Noise with			
VTX = VAG	17 dBrnc0	≤23 dBrncO	≤−64 dBm0P
Quiet Code Noise (all 1's at decoder (RDD) Input)	15 dBrnc0	≤15 dBrnc0	≤−75 dBm0P
Selective Response @ multiples of 8 kHz	−60 dBm0	See Frequency Response	≤−50 dBm0
Frequency Response @ 0 dBm0 input			
50 Hz gain	−26 dB	—	≤−24 dB
60 Hz gain	−22 dB	≤−20 dB	—
200 to 300 Hz ripple	45 dB	≤0.6 dB	≤1 dB
3400 Hz gain	−1.6 dB	≥−3 dB	≥−1.8 dB
4000 Hz gain	−35 dB	≤−28 dB	≤−28 dB
≥4600 Hz gain	<−62 dB	≤−60 dB	≤−60 dB
Single Frequency Spurious Response			
In band with input 1 kHz @ 0 dBm	≤−44 dB	≤−40 dB	≤−40 dB
Out of band with input 0 to 12 kHz @ 0 dBm	≤−32.5 dB	≤−28 dB	≤−25 dB
Differential Delay Distortion			
1150 to 2300	58 μs	≤60 μs	—
1000 to 2500	72 μs	≤100 μs	—
900 to 2700	91 μs	≥200 μs	—

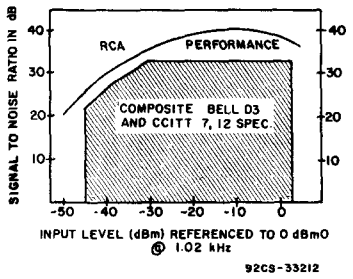


Fig. 14 - Signal-to-noise performance for CD22407 and CD22414. (See Fig. 13.)

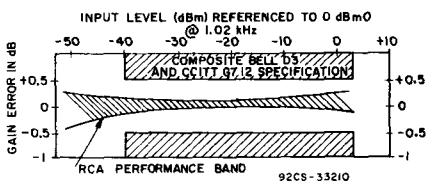


Fig. 15 - Gain tracking error for CD22407 and CD22414. (See Fig. 13.)

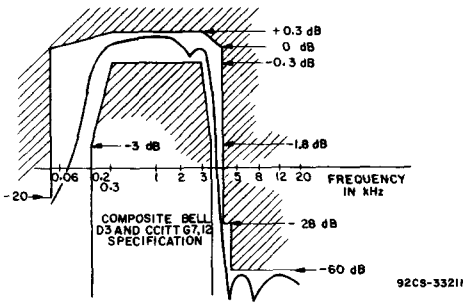


Fig. 16 - Frequency response of CD22407 and CD22414 CODEC and filter. (See Fig. 13.)