

CMOS 18-Stage Static Shift Register

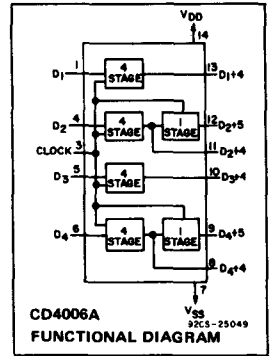
The RCA-CD4006A types are comprised of 4 separate shift register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single-rail data path.

A common clock signal is used for all stages. Data are shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 stages can be implemented using one CD4006A package. Longer shift register sections can be assembled by using more than one CD4006A.

Features:

- Fully static operation
- Shifting rates up to 5 MHz
- Permanent register storage with clock line high or low — no information recirculation required
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μ A at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).



MAXIMUM RATINGS, Absolute-Maximum Values:

- STORAGE-TEMPERATURE RANGE (T_{stg}) -65 to +150°C
- OPERATING-TEMPERATURE RANGE (T_A):
 - PACKAGE TYPES D, F, K, H -55 to +125°C
 - PACKAGE TYPE E -40 to +85°C
- DC SUPPLY-VOLTAGE RANGE, (V_{DD})
 - (Voltages referenced to V_{SS} Terminal). -0.5 to +15 V
- POWER DISSIPATION PER PACKAGE (P_D):
 - FOR $T_A = -40$ to +60°C (PACKAGE TYPE E) 500 mW
 - FOR $T_A = +60$ to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C to 200 mW
 - FOR $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K) 500 mW
 - FOR $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/°C to 200 mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR
 - FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) 100 mW
- INPUT VOLTAGE RANGE, ALL INPUTS -0.5 to $V_{DD} + 0.5$ V
- LEAD TEMPERATURE (DURING SOLDERING):
 - At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79 mm) from case for 10 s max. +265°C

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
 For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_s	5 10	80 40	—	100 50	—	ns
Clock Pulse Width, t_W	5 10	500 200	—	830 250	—	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 2.5	dc dc	0.6 2	MHz
Clock Rise and Fall Time, t_{rCL} , t_{fCL} *	5 10	— —	15 5	— —	15 5	μ s

* If more than one unit is cascaded t_{rCL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Applications:

- Serial shift registers
- Time delay circuits
- Frequency division

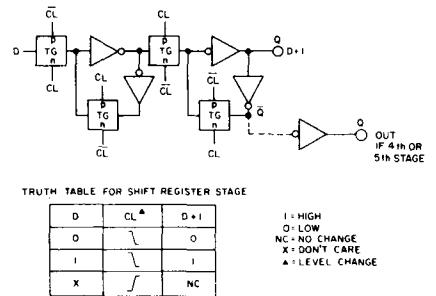


Fig. 1 — Logic diagram and truth table (one register stage).

CD4006A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	+25		+125	-40	+25		+85	
Quiescent Device Current, I _L Max.	-	-	5	0.5	0.01	0.5	30	5	0.03	5	70	μA
	-	-	10	1	0.01	1	60	10	0.05	10	140	
Output Voltage: Low-Level, VOL	-	5	5	0 Typ.; 0.05 Max.								V
	-	10	10	0 Typ.; 0.05 Max.								
High Level, VOH	-	0	5	4.95 Min.; 5 Typ.								V
	-	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V _{NL}	4.2	-	5	1.5 Min.; 2.25 Typ.								V
	9	-	10	3 Min.; 4.5 Typ.								
Inputs High, V _{NH}	0.8	-	5	1.5 Min.; 2.25 Typ.								V
	1	-	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V _{NML}	4.5	-	5	1 Min.								V
	9	-	10	1 Min.								
Inputs High, V _{NMH}	0.5	-	5	1 Min.								V
	1	-	10	1 Min.								
Output Drive Current: n-Channel (Sink), I _{DN} Min.	0.5	-	5	0.155	0.25	0.125	0.085	0.072	0.25	0.06	0.048	mA
	0.5	-	10	0.31	0.5	0.25	0.175	0.15	0.5	0.125	0.1	
p-Channel (Source), I _{DP} Min.	4.5	-	5	-0.125	-0.15	-0.1	-0.07	-0.06	-0.15	-0.05	-0.04	mA
	9.5	-	10	-0.25	-0.3	-0.2	-0.14	-0.12	-0.3	-0.1	-0.08	
Input Leakage Current, I _{IL} , I _{IH}	Any Input	-	15	±10 ⁻⁵ Typ., ±1 Max.								μA

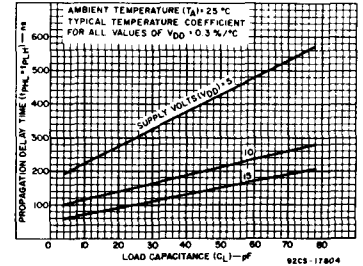


Fig. 2 - Typical propagation delay time vs. load capacitance.

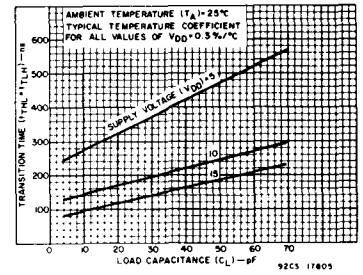


Fig. 3 - Typical transition time vs. load capacitance.

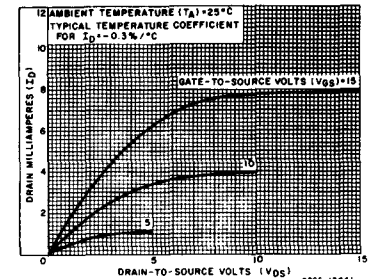


Fig. 5 - Typical output n-channel drain characteristics.

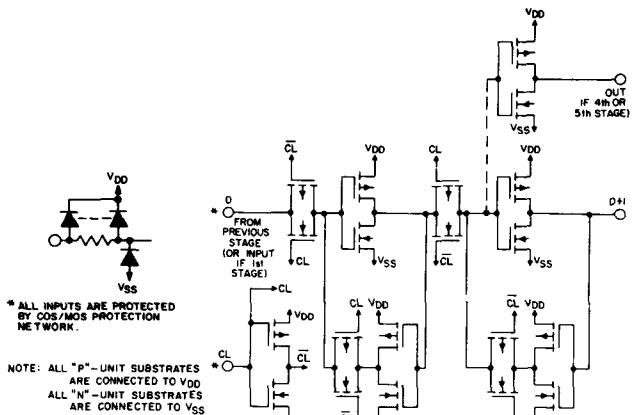


Fig. 4 - Schematic diagram (one register stage).

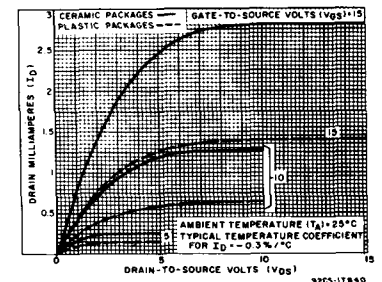


Fig. 6 - Minimum output n-channel drain characteristics.

CD4006A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$, Input $t_r, t_f = 20\text{ ns}$,

$C_L = 15\text{ pF}, R_L = 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS	
		V_{DD} (V)	D, F, K, H Packages			E Package			
			Min.	Typ.	Max.	Min.	Typ.		Max.
Propagation Delay Time; t_{PLH}, t_{PHL}	5	—	250	400	—	250	500	ns	
	10	—	125	200	—	125	250		
Transition Time; t_{THL}, t_{TLH}	5	—	250	400	—	250	500	ns	
	10	—	125	200	—	125	250		
Maximum Clock Input Frequency, f_{CL}	5	1	2.5	—	0.6	2.5	—	MHz	
	10	2.5	5	—	2	5	—		
Minimum Clock Pulse Width, t_W	5	—	200	500	—	200	830	ns	
	10	—	100	200	—	100	250		
Clock Rise & Fall Time; $t_{r,CL}, t_{f,CL}^*$	5	—	—	15	—	—	15	μs	
	10	—	—	5	—	—	5		
Minimum Data Set Up Time, t_S	5	—	50	80	—	50	100	ns	
	10	—	25	40	—	25	50		
Average Input Capacitance, C_i	Data Input	—	5	—	—	5	—	pF	
	Clock Input	—	30	—	—	30	—		

* If more than one unit is cascaded $t_{r,CL}$ should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

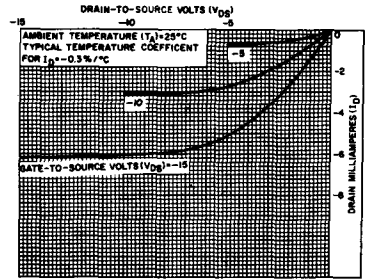


Fig. 7 - Typical output p-channel drain characteristics.

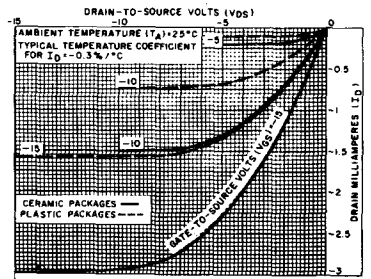


Fig. 8 - Minimum output p-channel drain characteristics.

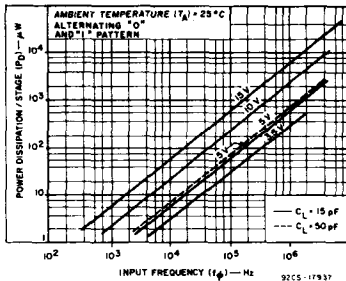


Fig. 9 - Typical dissipation characteristics.

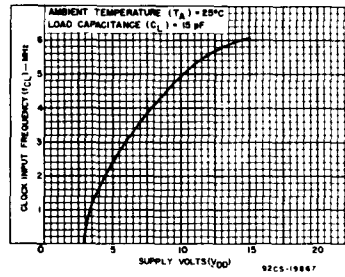


Fig. 10 - Typical clock input frequency vs. supply voltage.

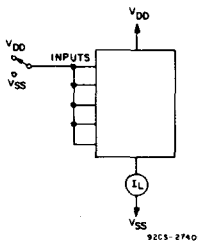


Fig. 11 - Quiescent device current test circuit.

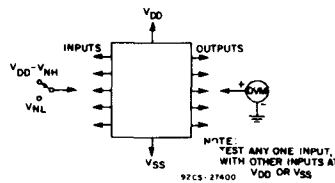


Fig. 12 - Noise immunity test circuit.

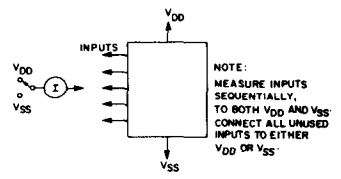


Fig. 13 - Input leakage current test circuit.