

CD4006B Types

CMOS 18-Stage Static Shift Register

High-Voltage Types (20-Volt Rating)

The RCA-CD4006B types are composed of 4 separate shift register sections: two sections of four stages and two sections of five stages with an output tap at the fourth stage. Each section has an independent single-rail data path.

A common clock signal is used for all stages. Data are shifted to the next stage on negative-going transitions of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8, and 9 stages or single register sections of 10, 12, 13, 14, 16, 17 and 18 stages can be implemented using one CD4006B package. Longer shift register sections can be assembled by using more than one CD4006B.

To facilitate cascading stages when clock rise and fall times are slow, an optional output (D_1+4') that is delayed one-half clock-cycle, is provided (see Truth Table for Output from Term. 2).

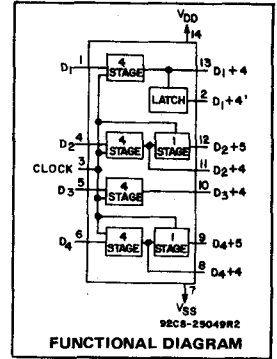
The CD4006B types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- Fully static operation
- Shifting rates up to 12 MHz @ 10 V (typ.)
- Permanent register storage with clock line high or low — no information recirculation required
- 100% tested for quiescent current at 20 V
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Serial shift registers
- F frequency division
- Time delay circuits



TRUTH TABLE FOR SHIFT REGISTER STAGE

D	CL [▲]	D + 1
0		0
1		1
X		NC

TRUTH TABLE FOR OUTPUT FROM TERM2

D_1+4	CL [▲]	D_1+4'
0		0
1		1
X		NC

1 = HIGH X = DON'T CARE
 0 = LOW ▲ = LEVEL CHANGE
 NC = NO CHANGE

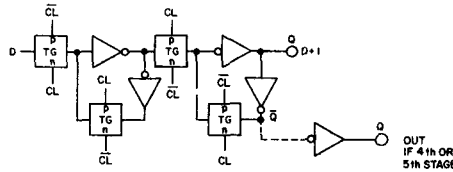
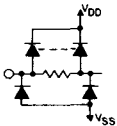
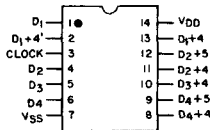


Fig. 1 - Logic diagram and truth table (one register stage).

TERMINAL ASSIGNMENT



ALL INPUTS (TERMINALS 1, 3, 4, 5, 6) PROTECTED BY COS/MOS PROTECTION NETWORK

92CS-28974

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A =$ Full Package Temperature Range)	—	3	18	V
Clock Pulse Width, t_{W}	5	180	—	ns
	10	80	—	
	15	50	—	
Data Setup Time, t_S	5	100	—	ns
	10	50	—	
	15	40	—	
Data Hold Time, t_H	5	60	—	ns
	10	40	—	
	15	30	—	
Clock Rise or Fall Time: t_r, t_f	5, 10, 15	—	15	μ S
Clock Input Frequency, f_{CL}	5	—	2.5	MHz
	10	—	5	
	15	—	7	

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MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at $12\text{ mW}/^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F, K)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F, K)	Derate Linearly at $12\text{ mW}/^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES ($^\circ\text{C}$)							UNITS
				Values at $-55, +25, +125$ Apply to D, F, K, H Packages Values at $-40, +25, +85$ Apply to E Package							
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	-	0.5	5	5	5	150	150	-	0.04	5	μA
	-	0.10	10	10	10	300	300	-	0.04	10	
	-	0.15	15	20	20	600	600	-	0.04	20	
	-	0.20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I_{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, V_{OL} Max.	-	0.5	5			0.05			0	0.05	V
	-	0.10	10			0.05			0	0.05	
	-	0.15	15			0.05			0	0.05	
Output Voltage: High-Level, V_{OH} Min.	-	0.5	5			4.95		4.95	5	-	V
	-	0.10	10			9.95		9.95	10	-	
	-	0.15	15			14.95		14.95	15	-	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	-	5			1.5		-	-	1.5	V
	1, 9	-	10			3		-	-	3	
	1.5, 13.5	-	15			4		-	-	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	-	5			3.5		3.5	-	-	V
	1, 9	-	10			7		7	-	-	
	1.5, 13.5	-	15			11		11	-	-	
Input Current I_{IN} Max.	-	0.18	18	± 0.1	± 0.1	± 1	± 1	-	$\pm 10^{-5}$	± 0.1	μA

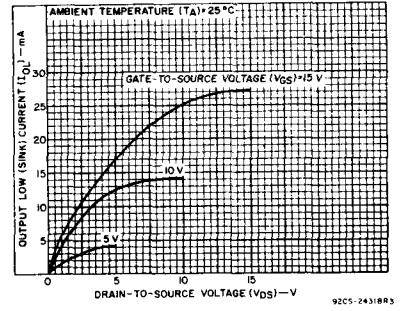


Fig. 2 - Typical output low (sink) current characteristics.

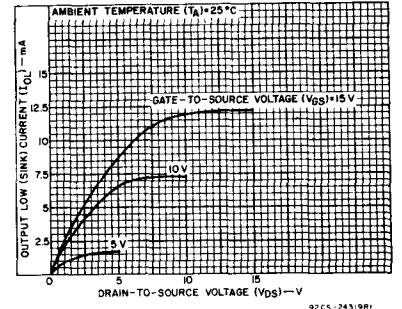


Fig. 3 - Minimum output low (sink) current characteristics.

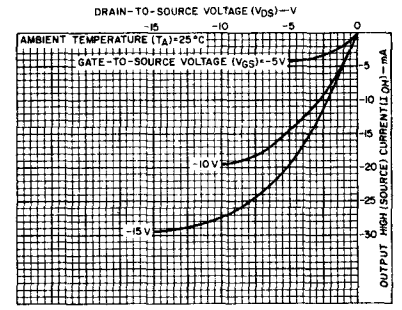


Fig. 4 - Typical output high (source) current characteristics.

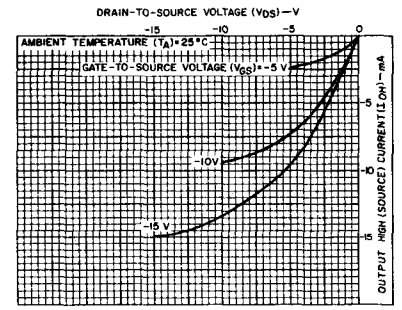


Fig. 5 - Minimum output high (source) current characteristics.

CD4006B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$,
 $C_L = 50\text{ pF}$, $R_L = 200\text{ K}\Omega$

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	TYPICAL VALUES	UNITS
Propagation Delay Time, t_{PHL}, t_{PLH}	5 10 15	200 100 80	ns
Transition Time, t_{THL}, t_{TLH}	5 10 15	100 50 40	ns
Minimum Data Setup Time, t_S	5 10 15	50 25 20	ns
Minimum Clock Pulse Width, t_W	5 10 15	100 45 30	ns
Maximum Clock Input Frequency, f_{CL}	5 10 15	5 12 16	MHz
Maximum Clock Input Rise or Fall Time t_{rCL}, t_{fCL}^*	5 10 15	15 15 15	μs
Input Capacitance, C_{IN}	Any Input	5	pF

* If more than one unit is cascaded t_{rCL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

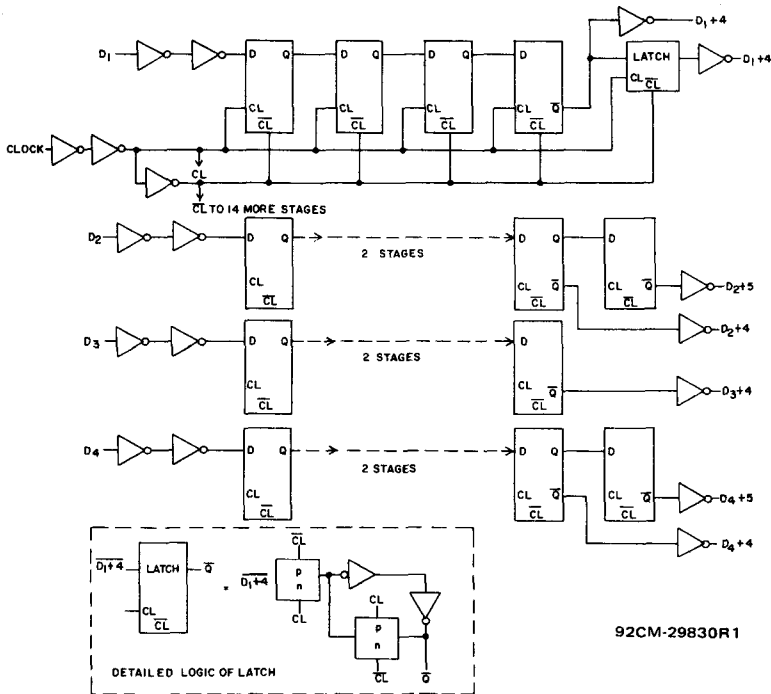


Fig. 6 - Logic diagram with detail of latch.

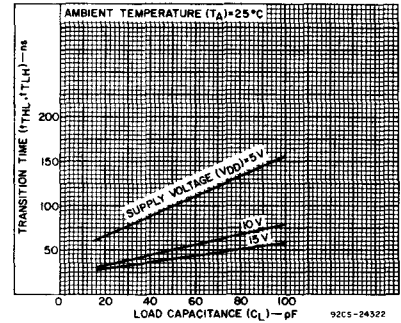


Fig. 7 - Typical transition time as a function of load capacitance.

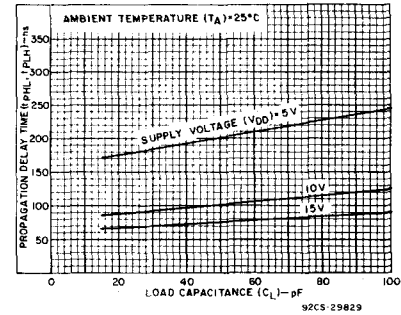


Fig. 8 - Typical propagation delay time as a function of load capacitance.

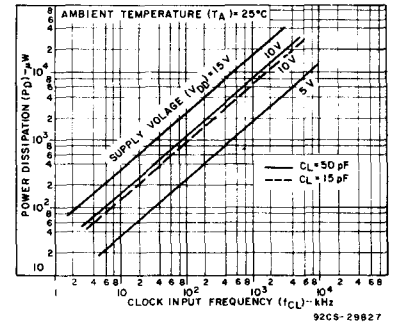


Fig. 9 - Typical dynamic power dissipation as a function of clock frequency.

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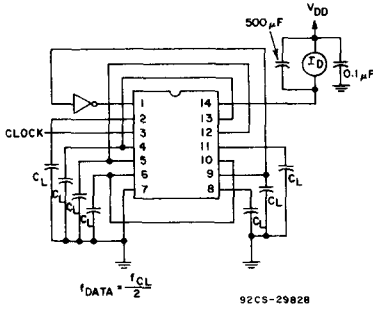


Fig. 10 - Dynamic power dissipation test circuit.

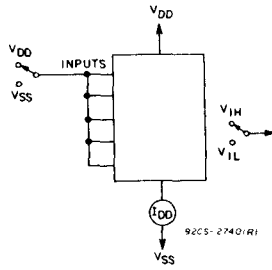


Fig. 11 - Quiescent device current test circuit.

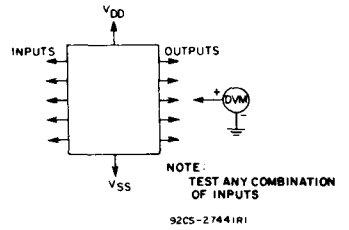


Fig. 12 - Input voltage test circuit.

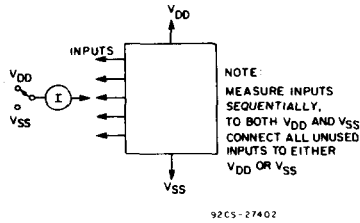
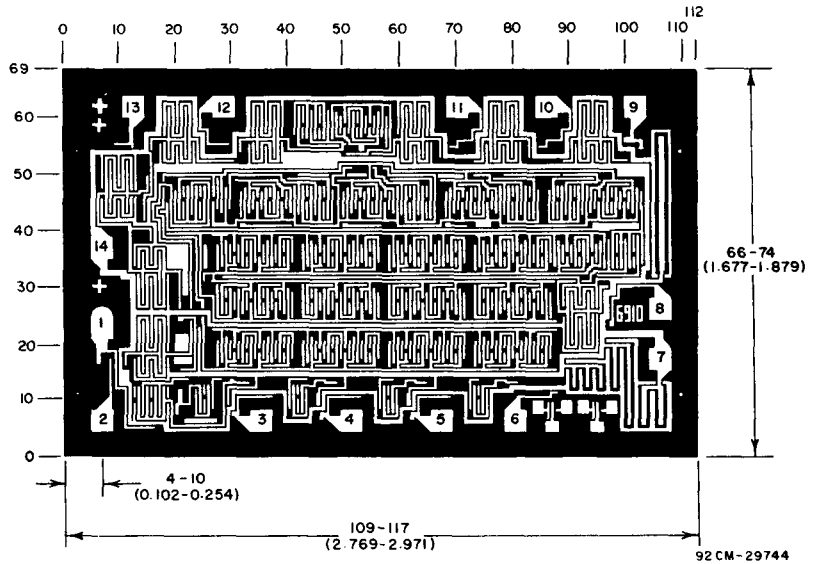


Fig. 13 - Input current test circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to $+16$ mils applicable to the nominal dimensions shown.

Dimensions and pad layout for CD4006BH.