CMOS 9-Bit Parity Generator/Checker

High-Voltage Types (20-Volt Rating)

The RCA-CD40101B is a 9-bit (8 data bits plus 1 parity bit) parity generator/checker. It may be used to detect errors in data transmission or data retrieval. Odd and even outputs facilitate odd or even parity generation and checking.

When used as a parity generator, a parity bit is supplied along with the data to generate an even or odd parity output.

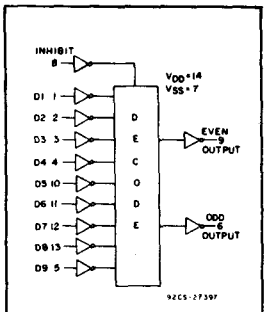
When used as a parity checker, the received data bits and parity bits are compared for correct parity. The even or odd outputs are used to indicate an error in the received data.

Word-length capability is expandable by cascading. The CD40101B is also provided with an inhibit control. If the inhibit control is set at logical "1", the even and odd outputs go to a logical "0".

The CD40101B types are supplied in 14-lead dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **100% tested for maximum quiescent current at 20 V**
- **Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C**
- **Noise margin (full package-temperature range): 1 V at V_{DD} = 5 V; 2 V at V_{DD} = 10 V; 2.5 V at V_{DD} = 15 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Standardized, symmetrical output characteristics**
- **Meets all requirements of JEDEC Tentative Standard No.13A, "Standard Specifications for Description of 'B' Series CMOS Devices."**

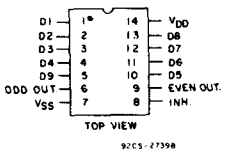


FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

TERMINAL ASSIGNMENT



RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

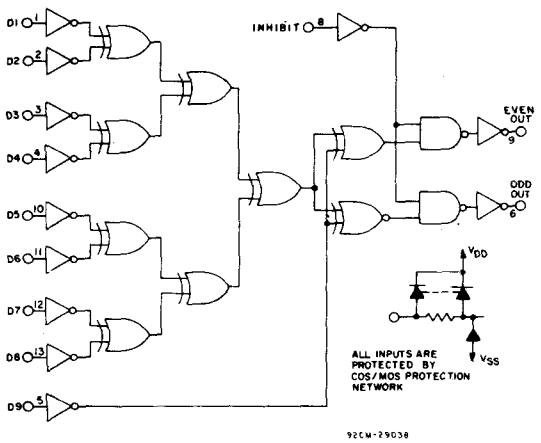


Fig. 1 – CD40101B logic diagram.

Truth Table

Inputs		Outputs	
D1-D9	Inhibit	Even	Odd
Σ 1's=Even	0	1	0
Σ 1's=Odd	0	0	1
X	1	0	0

X = Don't Care
Logic 1 = High
Logic 0 = Low

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, K, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3 4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				–	–	1.5	V
	1, 9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	–	–	
	1, 9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS
	V_{DD} (V)	Typ.	Max.	
Data Propagation Delay Time, t_{PHL}, t_{PLH}	5	350	700	ns
	10	150	300	
	15	100	200	
Inhibit-to-Output Propagation Delay Time, t_{PHL}, t_{PLH}	5	140	280	
	10	70	140	
	15	50	100	
Transition Time, t_{THL}, t_{TLH}	5	100	200	
	10	50	100	
	15	40	80	
Input Capacitance, C_{IN}	Any Input	5	7.5	pF

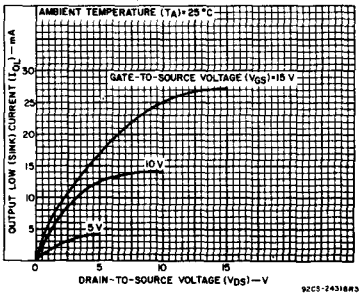


Fig.2 – Typical output low (sink) current characteristics.

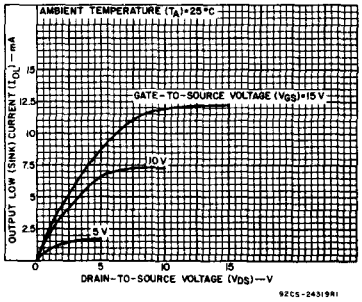


Fig.3 – Minimum output low (sink) current characteristics.

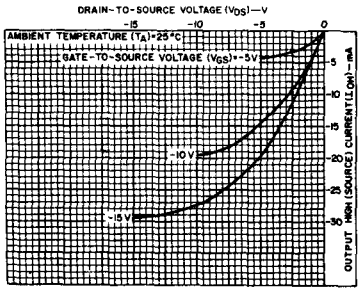


Fig.4 – Typical output high (source) current characteristics.

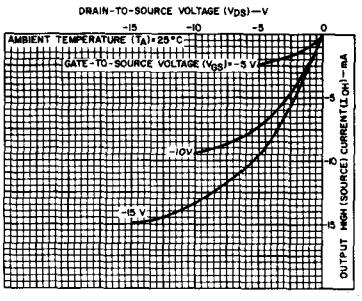


Fig.5 – Minimum output high (source) current characteristics.

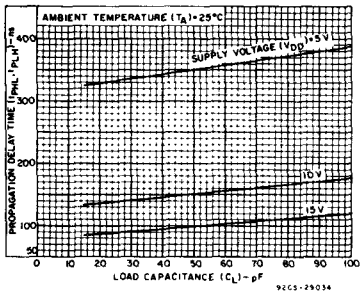


Fig.6 – Typical propagation delay time as a function of load capacitance.

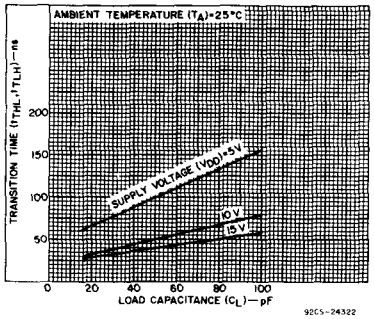


Fig. 7 – Typical transition time as a function of load capacitance.

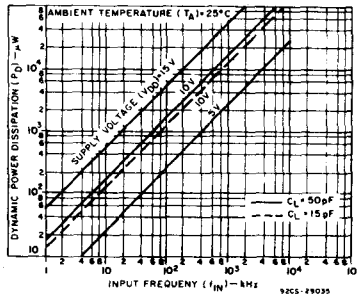


Fig. 8 – Typical dynamic power dissipation as a function of input frequency.

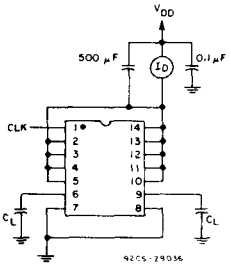


Fig.9 – Dynamic power dissipation test circuit.

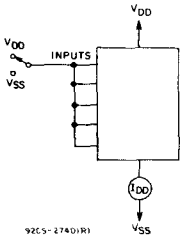


Fig.10 – Quiescent-device-current test circuit.

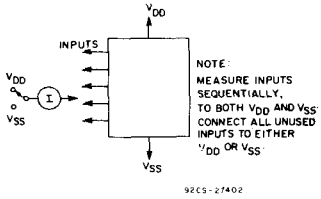


Fig.11 – Input-leakage current.

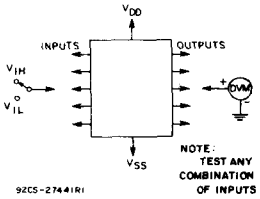
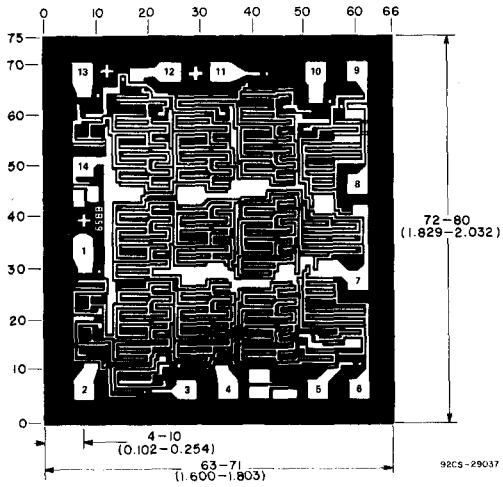


Fig.12 – Input-voltage test circuit.

DIMENSIONS AND PAD LAYOUT FOR CD40101B



The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of –3 mils to +16 mils applicable to the nominal dimensions shown.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).