CMOS 4-Bit Bidirectional Universal Shift Register

High-Voltage Types (20 Volt Rating)

The RCA-CD40104B is a universal shift register featuring parallel inputs, parallel outputs, SHIFT RIGHT and SHIFT LEFT serial inputs, and a high-impedance third output state allowing the device to be used in bus-organized systems.

In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift-right and shift-left are accomplished synchronously on the positive clock edge with serial data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clearing the register is accomplished by setting both mode controls low and clocking the register. When the output enable input is low, all outputs assume the high impedance state.

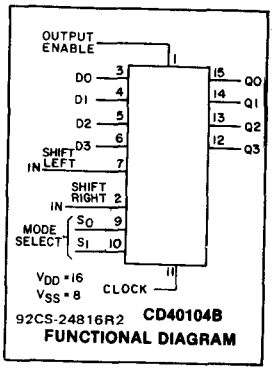
The RCA-CD40194B is a universal shift register featuring parallel inputs, parallel outputs SHIFT RIGHT and SHIFT LEFT serial inputs, and a direct overriding clear input. In the parallel-load mode (S0 and S1 are high), data is loaded into the associated flip-flop and appears at the output after the positive transition of the CLOCK input. During loading, serial data flow is inhibited. Shift right and shift left are accomplished synchronously on the positive clock edge with data entered at the SHIFT RIGHT and SHIFT LEFT serial inputs, respectively. Clocking of the register is inhibited when both mode control inputs are low. When low, the $\overline{\text{RESET}}$ input resets all stages and forces all outputs low.

Features:

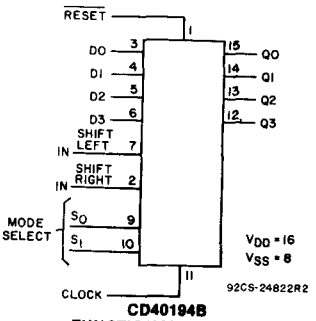
- **Medium-speed: f_{CL} = 12 MHz (typ.) @ V_{DD} = 10 V**
- **Fully static operation**
- **Synchronous parallel or serial operation**
- **Three-state outputs (CD40104B)**
- **Asynchronous master reset (CD40194B)**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices**

Applications:

- **Arithmetic unit bus registers**
- **Serial/parallel conversions**
- **General-purpose register for bus-organized systems**
- **General-purpose registers**



CD40104B
FUNCTIONAL DIAGRAM



CD40194B
FUNCTIONAL DIAGRAM

The CD40104B and CD40194B types are supplied in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD40194B is similar to industry types 340194 and MC40194.

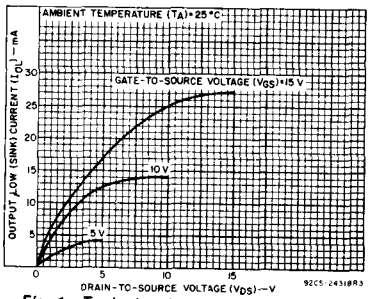


Fig. 1—Typical n-channel output low (sink) current characteristics.

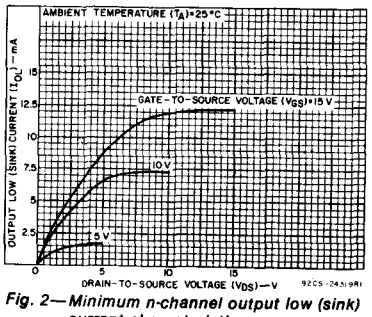


Fig. 2—Minimum n-channel output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = -40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:	
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC		VDD (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For Package-Temperature Range)			3	18	V
Setup Time, D0, D3, SR_{IN}, SL_{IN} to clock	t_s	5	100	—	ns
		10	70	—	
		15	50	—	
SELECT 0, SELECT 1 to clock		5	400	—	
		10	220	—	
		15	130	—	
Hold Time, D0, D03, SR_{IN}' SL_{IN} to clock	t_H	5	0	—	
		10	0	—	
		15	0	—	
SELECT 0, SELECT 1 to clock		5	0	—	
		10	0	—	
		15	0	—	
Clock Pulse Width,	t_W	5	180	—	
		10	80	—	
		15	50	—	
Clock Input Frequency	f_{CL}	5	—	3	MHz
		10	—	6	
		15	—	8	
Clock Input Rise or Fall Time,	t_rCL, t_fCL	5	1000	—	μs
		10	100	—	
		15	100	—	
Reset Pulse Width,*	t_{WR}	5	300	—	ns
		10	200	—	
		15	140	—	

* For CD40194B series only.

CONTROL TRUTH TABLE FOR CD40194B SERIES

CLOCK▲	MODE SELECT S_0	MODE SELECT S_1	OUTPUT ENABLE	ACTION
⎍	0	0	1	Reset
⎍	1	0	1	Shift right (Q_0 toward Q_3)
⎍	0	1	1	Shift left (Q_3 toward Q_0)
⎍	1	1	1	Parallel load
X	X	X	0	Operations occur as shown above, but outputs assume high impedance

CONTROL TRUTH TABLE FOR CD40194B SERIES

CLOCK	MODE SELECT S_0	MODE SELECT S_1	$\overline{RESET}$	ACTION
X	0	0	1	No Change
⎍	1	0	1	Shift Right (Q0 toward Q3)
⎍	0	1	1	Shift Left (Q3 toward Q0)
⎍	1	1	1	Parallel Load
X	X	X	0	Reset

1 = High level
0 = Low level
X = Don't care
▲ = Level change

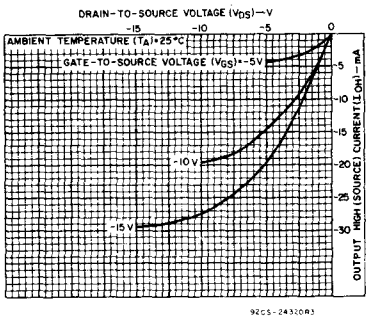


Fig. 3—Typical p-channel output high (source) current characteristics.

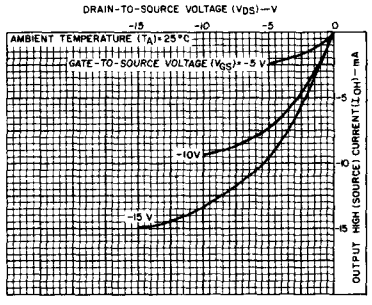


Fig. 4—Minimum p-channel output high (source) current characteristics.

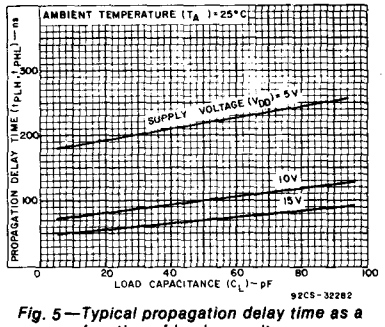


Fig. 5—Typical propagation delay time as a function of load capacitance, (CLOCK to Q).

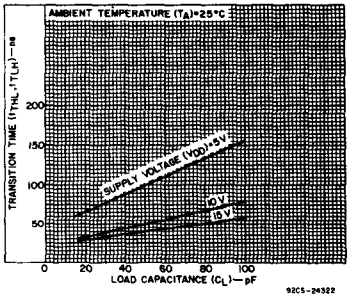


Fig. 6—Typical transition time as a function of load capacitance.

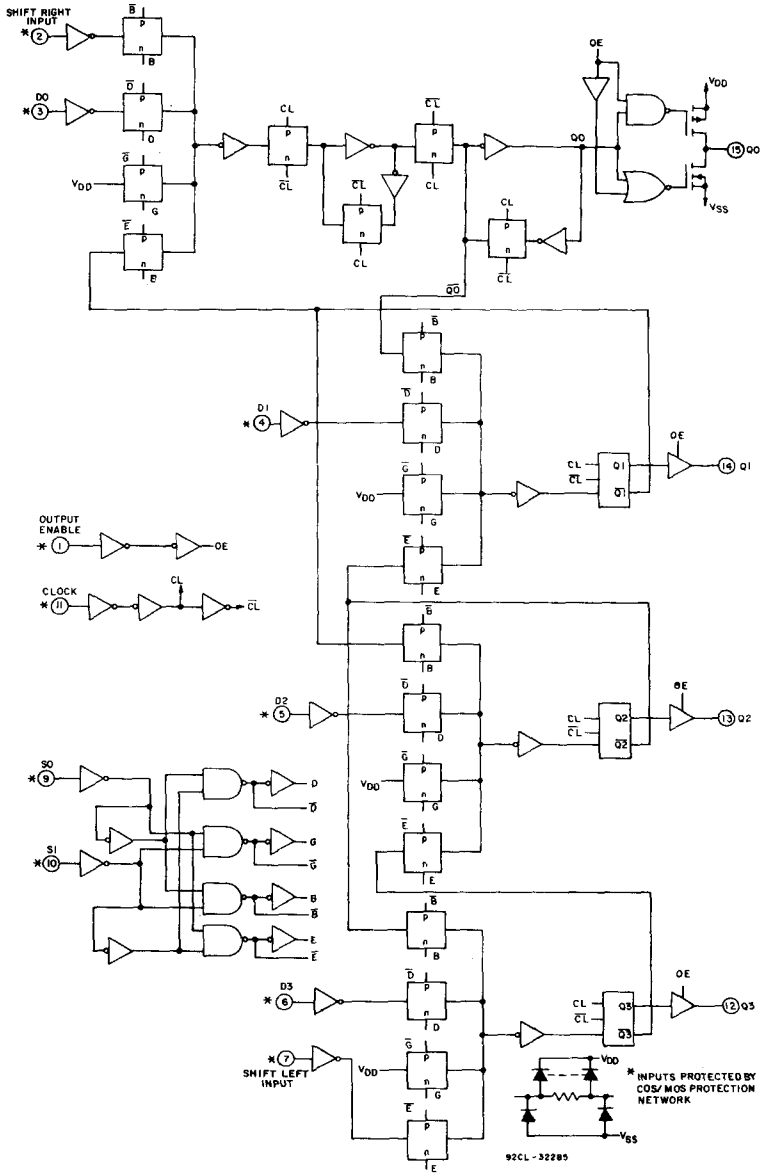


Fig. 7—CD40104B logic diagram.

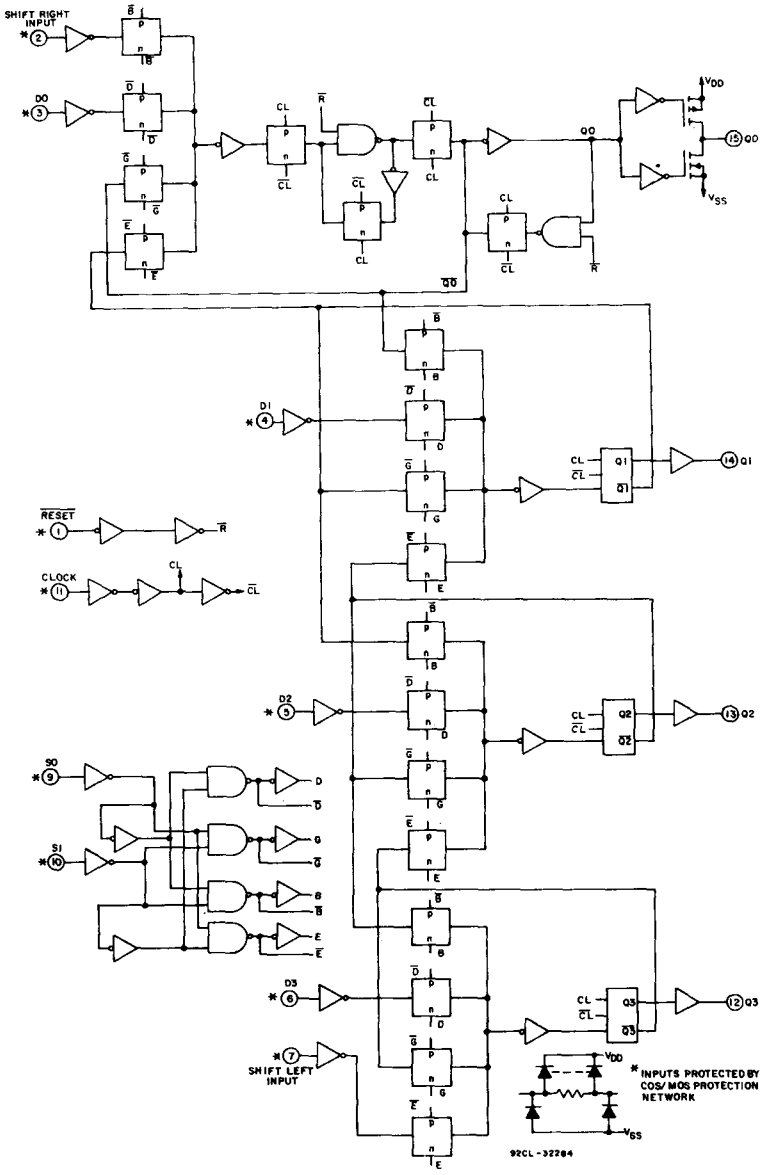


Fig. 8—CD40194B logic diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, K, H Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	—	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	—	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	—	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	$±10^{-5}$	±0.1	μA
3-State Output Leakage Current, I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	—	$±10^{-4}$	±0.4	μA

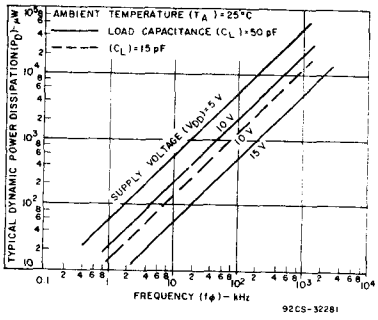


Fig. 9—Typical power dissipation as a function of frequency.

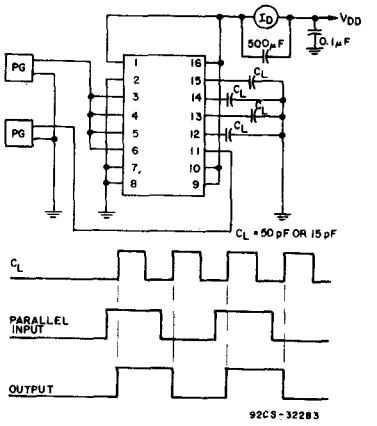


Fig. 10—Dynamic power dissipation test circuit.

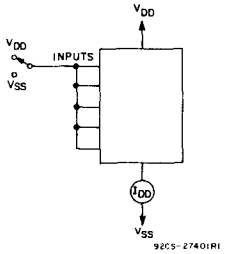


Fig. 11—Quiescent-device-current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} V	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: Clock to Q t_{PHL}, t_{PLH}	5	—	220	440	ns
	10	—	100	200	
	15	—	70	140	
3-State Outputs:■ High Impedance t_{PZH}, t_{PZL}, t_{PLZ}	5	—	80	160	
	10	—	35	70	
	15	—	25	50	
t_{PHZ}	5	—	45	90	
	10	—	25	50	
	15	—	20	40	
Output Transition Time t_{THL}, t_{TLH}	5	—	100	200	
	10	—	50	100	
	15	—	40	80	
Minimum Setup Time: t_S D0, D3, SR_{IN}, SL_{IN} to Clock	5	—	80	100	
	10	—	35	70	
	15	—	20	50	
SELECT 0, SELECT 1 to Clock	5	—	200	400	
	10	—	110	220	
	15	—	65	130	
Minimum Hold Time: t_H D0, D3, SR_{IN}, SL_{IN} to Clock	5	—	−65	0	
	10	—	−25	0	
	15	—	−15	0	
SELECT 0, SELECT 1 to Clock	5	—	−170	0	
	10	—	−95	0	
	15	—	−55	0	
Minimum Clock Pulse Width t_W	5	—	90	180	
	10	—	40	80	
	15	—	25	50	
Maximum Clock Input Frequency f_{CL}	5	3	6	—	MHz
	10	6	12	—	
	15	8	15	—	
Maximum Clock Rise or Fall Time t_rCL, t_fCL	5	—	—	1000	μs
	10	—	—	100	
	15	—	—	100	
Mininum Reset Pulse Width* t_{WR}	5	—	150	300	ns
	10	—	100	200	
	15	—	70	140	
Reset Propagation Delay* t_{PRHL}	5	—	230	460	
	10	—	90	180	
	15	—	65	130	
Input Capacitance C_{IN}	Any Input	—	5	7.5	pF

■ For CD40104B series only. * For CD40194B series only.

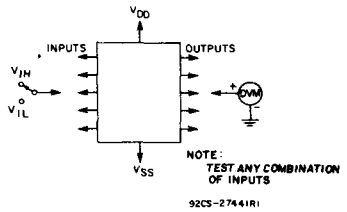


Fig. 12—Input-voltage test circuit.

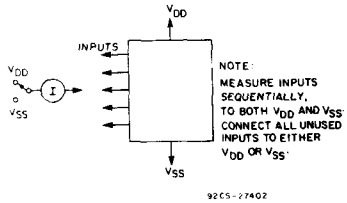
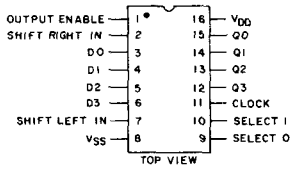


Fig. 13—Input current test circuit.

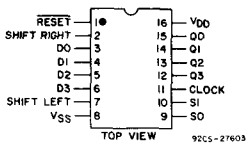
TERMINAL DIAGRAMS

Top View

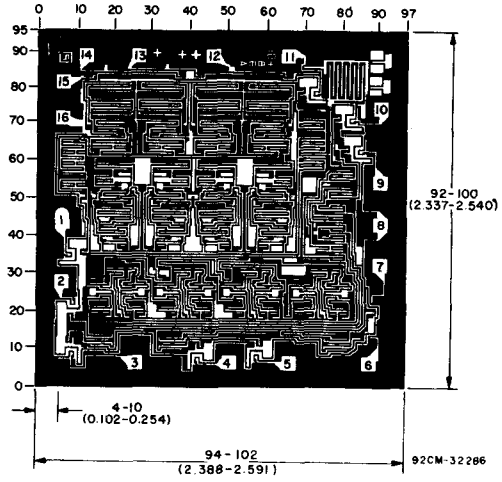


CD40104B

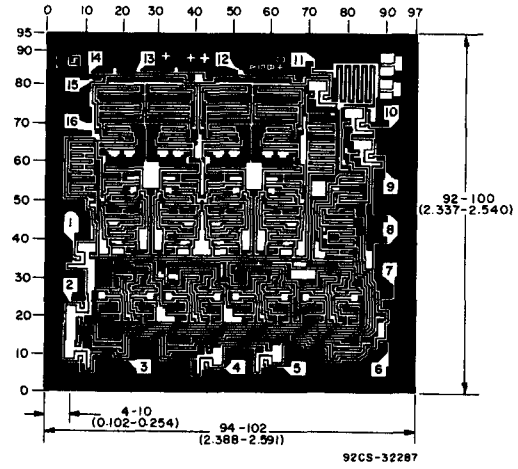
Top View



CD40194B



Dimensions and pad layout for CD40104BH



Dimensions and pad layout for CD40194BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.