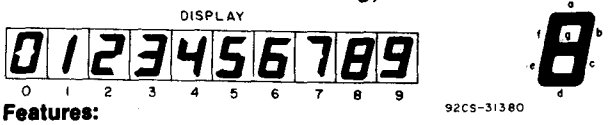
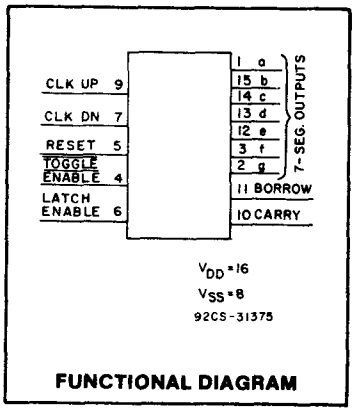
CMOS Decade Up-Down Counter/Latch/Display Driver

High-Voltage Type (20-V Rating)



Features:

- *Separate clock-up and clock-down lines*
- *Capable of driving common cathode LEDs and other displays directly*
- *Allows cascading without any external circuitry*
- *100% tested for quiescent current at 20 V*
- *Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25° C*



FUNCTIONAL DIAGRAM

The RCA-CD40110B is a dual-clocked up/down counter with a special preconditioning circuit that allows the counter to be clocked, via positive going inputs, up or down regardless of the state or timing (within 100 ns typ.) of the other clock line.

The clock signal is fed into the control logic and Johnson counter after it is preconditioned. The outputs of the Johnson counter (which include anti-lock gating to avoid being locked at an illegal state) are fed into a latch. This data can be fed directly to the decoder through the latch or can be strobed to hold a particular count while the Johnson counter continues to be clocked. The decoder feeds a seven-segment bipolar output driver which can source up to 25 mA to drive LEDs and other displays such as low-voltage fluorescent and incandescent lamps.

A short durating negative-going pulse appears on the BORROW output when the count changes from 0 to 9 or the CARRY output when the count changes from 9 to 0. At the other times the BORROW and CARRY outputs are a logic 1.

The CARRY and BORROW outputs can be tied directly to the clock-up and clock-down lines respectively of another CD40110B for easy cascading of several counters.

- *Noise margin (full package-temperature range) =*
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- *5 V, 10 V and 15 V parametric ratings*
- *Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices".*

Applications:

- *Rate comparators*
- *General counting applications where display is desired*
- *Up-down counting applications where input pulses are random in nature*

The CD40110B types are supplied in 16-lead dual-in-line ceramic packages (D and F suffixes), and 16-lead dual-in-line plastic package (E suffix), and also available in chip form, (H suffix).

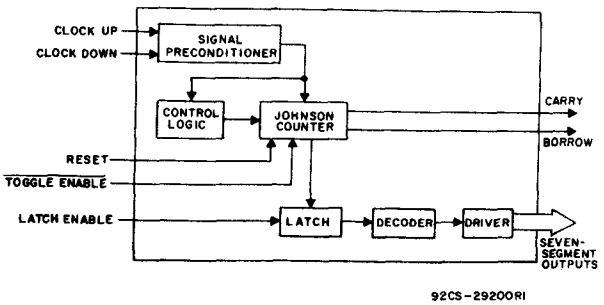


Fig. 1 - Functional diagram.

MAXIMUM RATINGS, Absolute Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C
(PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F) ..... 500 mW
For T_A = +100 to +125°C
(PACKAGE TYPES D, F) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE
(All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm)
from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} V	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package Temperature Range)	—	3	18	V
Clock Input Frequency f_{CL} (Sum of CL_{UP} & CL_{DN} Freqs.)	5 10 15	— — —	1 3 5	MHz
Clock Pulse Width t_W	5 10 15	110 40 30	— — —	ns
Latch Enable Pulse Width	5 10 15	110 30 24	— — —	ns
Reset Removal-Time	5 10 15	550 200 130	— — —	ns
Reset Pulse Width	5 10 15	350 170 120	— — —	ns

CD40110B Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions				Limits at Indicated Temperatures (°C) Values at -55, +25, +125 for D, F, H Packages Values at -40, +25, +85 for E Packages							Units
									+25			
	I_{OH} (mA)	V_{OH} (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current Max. I_{DD}	—	—	—	5	5	5	150	150	—	0.04	5	μA
	—	—	—	10	10	10	300	300	—	0.04	10	
	—	—	—	15	20	20	600	600	—	0.04	20	
	—	—	—	20	100	100	3000	3000	—	0.08	100	
Output Voltage Low-Level Max. V_{OL}	—	—	0,5	5	0.05				—	0	0.05	V
	—	—	0,10	10	0.05				—	0	0.05	
	—	—	0,15	15	0.05				—	0	0.05	
High-Level Min. V_{OH}	—	—	0,5	5	—	—	—	—	—	4.55	—	V
	—	—	0,10	10	—	—	—	—	—	9.55	—	
	—	—	0,15	15	—	—	—	—	—	14.55	—	
Input Low Voltage Max. V_{IL}	—	0.5, 3.8	—	5	1.5				—	—	1.5	V
	—	1, 8.8	—	10	3				—	—	3	
	—	1.5, 13.8	—	15	4				—	—	4	
Input High Voltage Min. V_{IH}	—	0.5, 3.8	—	5	3.8				3.5	—	—	V
	—	1, 8.8	—	10	7				7	—	—	
	—	1.5, 13.8	—	15	11				11	—	—	
7-Segment Outputs Output Drive Voltage, High Min. V_{OH}	■	—	—	5	3.9		4		3.9	4.5	—	V
	-5	—	—		3.65		3.7		3.7	4.3	—	
	-10	—	—		3.55		3.65		3.65	4.25	—	
	-15	—	—		3.5		3.5		3.6	4.15	—	
	-20	—	—		3.45		3.35		3.45	4	—	
	-25	—	—		3.4		3.3		3.4	3.9	—	
	■	—	—	10	8.75		8.85		8.75	9.5	—	
	-5	—	—		8.45		8.55		8.55	9.3	—	
	-10	—	—		8.42		8.5		8.5	9.25	—	
	-15	—	—		8.4		8.47		8.47	9.2	—	
	-20	—	—		8.4		8.40		8.45	9.1	—	
	-25	—	—		8.3		8.25		8.3	9	—	
	■	—	—	15	13.8		13.9		13.8	14.5	—	
	-5	—	—		13.65		13.75		13.75	14.35	—	
	-10	—	—		13.6		13.72		13.72	14.3	—	
	-15	—	—		13.6		13.7		13.7	14.2	—	
	-20	—	—		13.6		13.6		13.65	14.1	—	
	-25	—	—		13.3		13.25		13.3	14.0	—	
7-Segment Outputs Output Low (Sink) Current Min. I_{OL}	—	0.4	0, 5	5	1.28	1.22	0.84	0.72	1	2	—	mA
	—	0.5	0, 10	10	3.2	3	2.2	1.8	2.6	5.2	—	
	—	1.5	0, 15	15	8.4	8	5.6	4.8	6.8	13.6	—	
Carry Outputs Output Low (Sink) Current Min. I_{OL}	—	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	
	—	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	—	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current Min. I_{OH}	—	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
	—	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	—	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	—	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Input Current Max. I_{IN}	—	0, 18	0, 18	18	±0.1	±0.1	±1	±1	—	$±10^{-5}$	±0.1	μA

■ 0(10 μA)

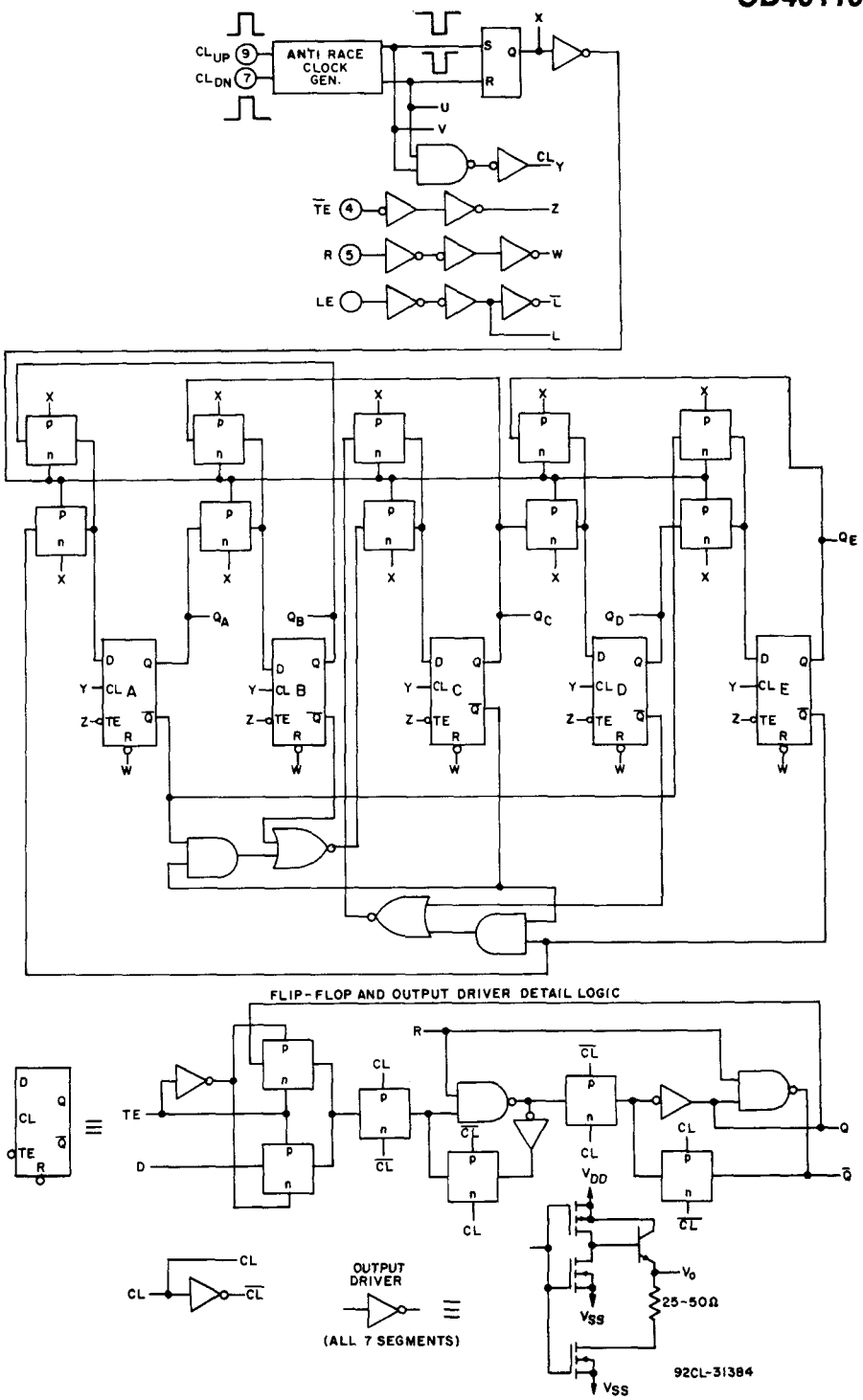


Fig. 2 - Logic diagram with flip-flop and output-driver details.
(cont'd on page 5)

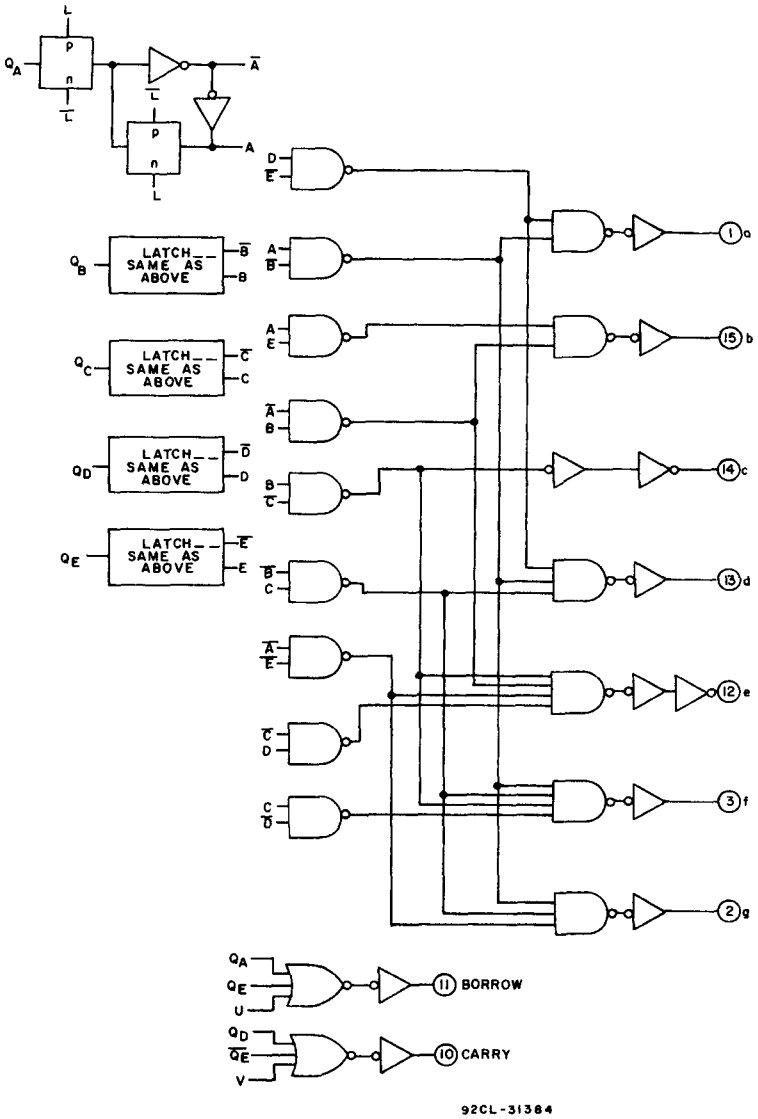
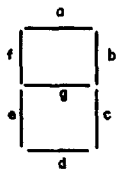
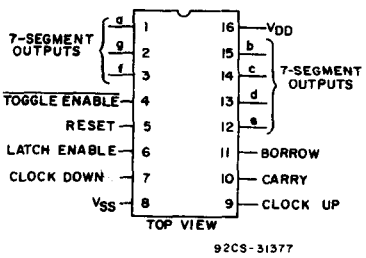


Fig. 2 - Logic diagram with flip-flop and output-driver details.

DISPLAY SEGMENTS



TERMINAL ASSIGNMENT



DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25° C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC		V_{DD} (V)	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Clock Up/Clock Down						
Propagation Delay Time: Clock to Carry or Borrow	t_{PLH}, t_{PHL}	5	—	300	600	ns
		10	—	100	200	
		15	—	70	140	
Clock to Segment	t_{PLH}, t_{PHL}	5	—	925	1850	ns
		10	—	360	720	
		15	—	250	500	
Minimum Clock Pulse Width		5	—	55	110	ns
		10	—	20	40	
		15	—	15	30	
Maximum Clock Input Frequency (Sum of CL_{UP} & CL_{DN} F)	f_{CL}	5	1	2.5	—	MHz
		10	3	6	—	
		15	5	8.5	—	
Minimum Toggle Enable Pulse Width		5	—	175	350	ns
		10	—	75	150	
		15	—	55	110	
Minimum Latch Enable Pulse Width		5	—	55	110	ns
		10	—	15	30	
		15	—	12	24	
Output Pulse Width: Carry		5	115	230	—	ns
		10	60	120	—	
		15	40	75	—	
Borrow		5	140	275	—	ns
		10	65	130	—	
		15	45	85	—	
Transition Time: Carry or Borrow	t_{TLH}, t_{THL}	5	—	85	170	ns
		10	—	45	90	
		15	—	30	60	
Minimum Delay Time Between CL_{UP} & CL_{DN}		5	—	100	—	ns
		10	—	80	—	
		15	—	60	—	
Maximum Clock Rise or Fall Time	t_rCL, t_fCL	5	—	—	15	*μs*
		10	—	—	15	
		15	—	—	15	
Reset						
Propagation Delay Time Reset to Output	t_{PLH}, t_{PHL}	5	—	650	1300	ns
		10	—	350	700	
		15	—	160	320	
Minimum Reset Removal Time		5	—	-275	0	ns
		10	—	-100	0	
		15	—	-65	0	
Minimum Reset Pulse Width		5	—	175	350	ns
		10	—	85	170	
		15	—	60	120	

CD40110B Types

TRUTH TABLE

CLOCK UP *	CLOCK DOWN *	LATCH ENABLE	TOGGLE ENABLE	RESET	COUNTER	DISPLAY
⌐¯	X	0	0	0	Increments by 1	Follows Counter
X	⌐¯	0	0	0	Decrements by 1	Follows Counter
¯⌐	¯⌐	X	X	0	No Change	No Change
X	X	1	X	1	Goes to 00000	Remains Fixed
X	X	0	X	1	Goes to 00000	Follows Counter (Display = 0)
X	X	X	1	0	Inhibited	Remains Fixed
⌐¯	X	1	0	0	Increments by 1	Remains Fixed
X	⌐¯	1	0	0	Decrements by 1	Remains Fixed

X = Don't Care 1 = High State 0 = Low State

* Typically 100 ns between clock-up and clock-down positive transitions are required to ensure proper counting.

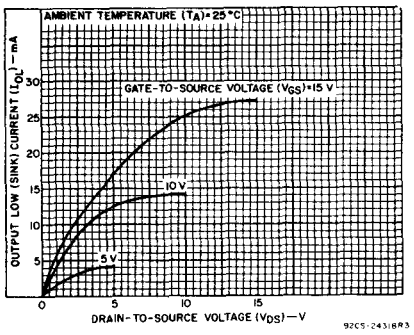


Fig. 3 - Typical carry or borrow output low (sink) current characteristics.

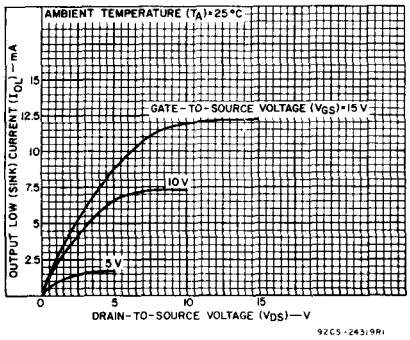


Fig. 4 - Minimum carry or borrow output low (sink) current characteristics.

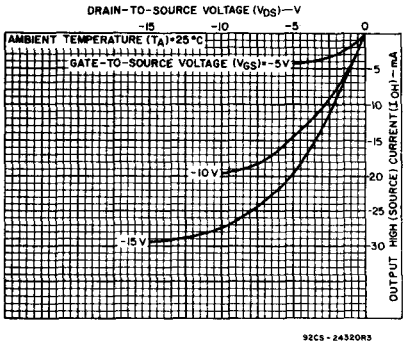


Fig. 5 - Typical carry or borrow output high (source) current characteristics.

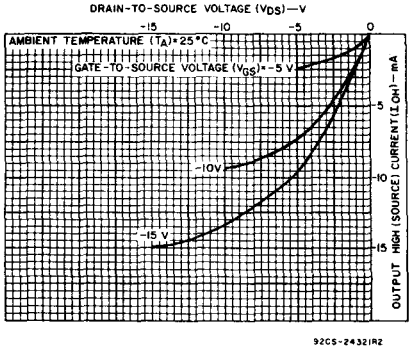


Fig. 6 - Minimum carry or borrow output high (source) current characteristics.

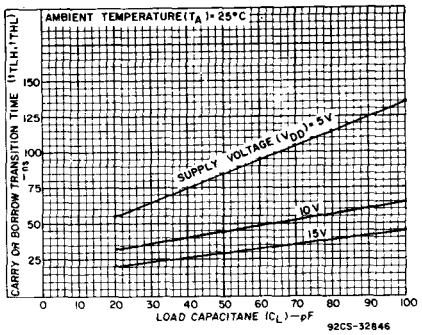


Fig. 7 - Typical carry or borrow transition time vs. load capacitance.

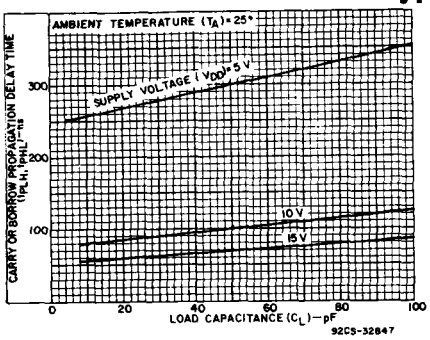


Fig. 8 - Typical carry or borrow propagation delay time vs. load capacitance.

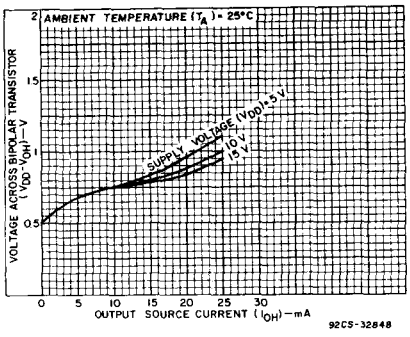


Fig. 9 - Voltage across bipolar transistor vs. output source current.

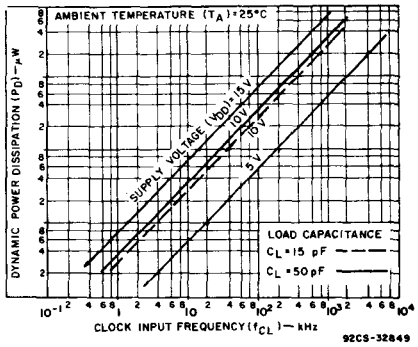


Fig. 10 - Typical dynamic power dissipation vs. frequency.

TEST CIRCUITS

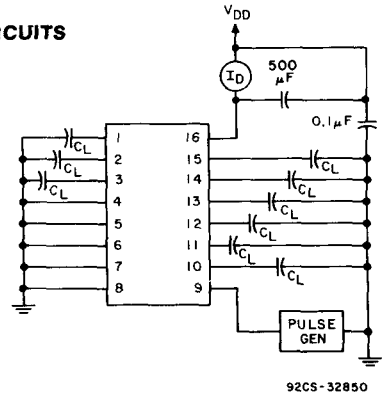


Fig. 11 - Dynamic power dissipation test circuit.

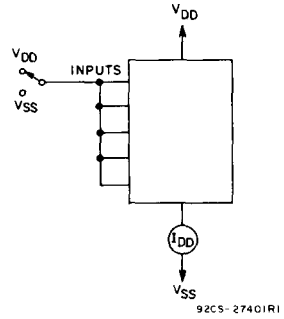


Fig. 12 - Quiescent device current.

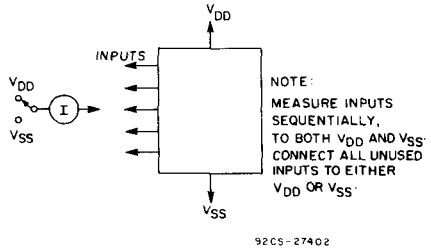


Fig. 13 - Input current.

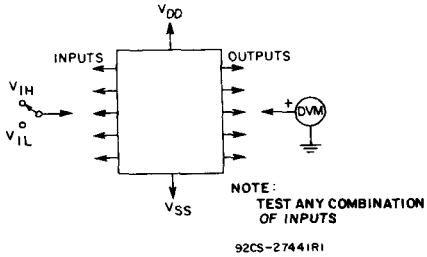


Fig. 14 - Input voltage.

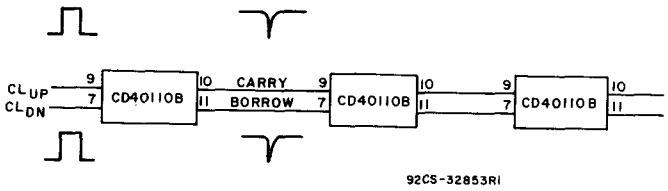
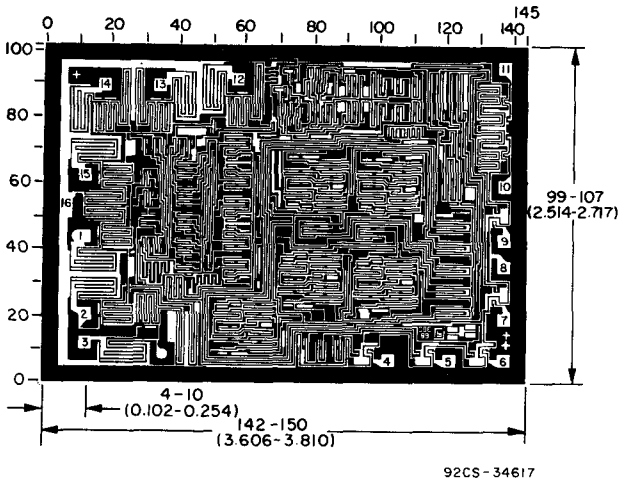


Fig. 15 - Cascading diagram.



Dimensions and pad layout for CD40110B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance −3 mils to +16 mils applicable to the nominal dimensions shown.