

## CD4014B, CD4021B Types

### CMOS 8-Stage Static Shift Registers

High-Voltage Types (20-Volt Rating)

#### CD4014B:

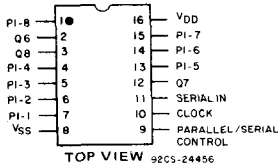
Synchronous Parallel or  
Serial Input/Serial Output

#### CD4021B:

Asynchronous Parallel Input or  
Synchronous Serial Input/Serial Output

The RCA-CD4014B and CD4021B series types are 8-stage parallel- or serial-input/serial-output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the CD4014B. In the CD4021B serial entry is synchronous with the clock but parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the CD4021B, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made. Register expansion using multiple packages is permitted.

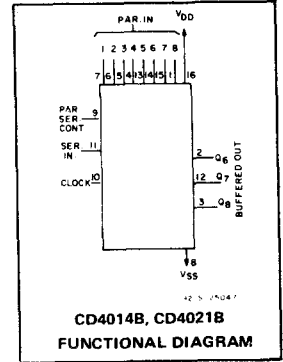
The CD4014B and CD4021B series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).



TOP VIEW 92CS-24456  
TERMINAL DIAGRAM  
CD4014B, CD4021B

#### Features:

- Medium-speed operation . . . 12 MHz (typ.) clock rate at  $V_{DD}-V_{SS} = 10\text{ V}$
- Fully static operation
- 8 master-slave flip-flops plus output buffering and control gating
- 100% tested for quiescent current at 20 V
- Maximum input current of  $1\ \mu\text{A}$  at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) =  $1\text{ V}$  at  $V_{DD} = 5\text{ V}$   
 $2\text{ V}$  at  $V_{DD} = 10\text{ V}$   
 $2.5\text{ V}$  at  $V_{DD} = 15\text{ V}$
- Standardized, symmetrical output characteristics
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



CD4014B, CD4021B  
FUNCTIONAL DIAGRAM

#### Applications:

- Parallel input/serial output data queueing
- Parallel to serial data conversion
- General-purpose register

#### RECOMMENDED OPERATING CONDITIONS AT $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	$V_{DD}$ (V)	LIMITS		UNITS				
		Min.	Max.					
Supply-Voltage Range ( $T_A = \text{Full Package-Temperature Range}$ )	—	3	18	V				
Clock Pulse Width, $t_{W}$	5	180	—	ns				
	10	80	—					
	15	50	—					
Clock Frequency, $f_{CL}$	5	—	3	MHz				
	10	—	6					
	15	—	8.5					
Clock Rise and Fall Time, $t_{rCL}, t_{fCL}$	5	—	15	$\mu\text{s}$				
	10	—	15					
	15	—	15					
Set-up Time, $t_s$ :	5	120	—	ns				
					Serial Input (ref. to CL)	80	—	
					15	60	—	
Parallel Inputs	5	80	—	ns				
					CD4014B (ref. to CL)	10	50	—
					CD4021B (ref. to P/S)	15	40	—
Parallel/Serial Control	5	180	—	ns				
					CD4014B (ref. to CL)	10	80	—
					CD4021B (ref. to CL)	15	60	—
Parallel/Serial Pulse Width, $t_{W}$ (CD4021B)	5	160	—	ns				
					10	80	—	
					15	50	—	
Parallel/Serial Removal Time, $t_{REM}$ (CD4021B)	5	280	—	ns				
					10	140	—	
					15	100	—	

# CD4014B, CD4021B Types

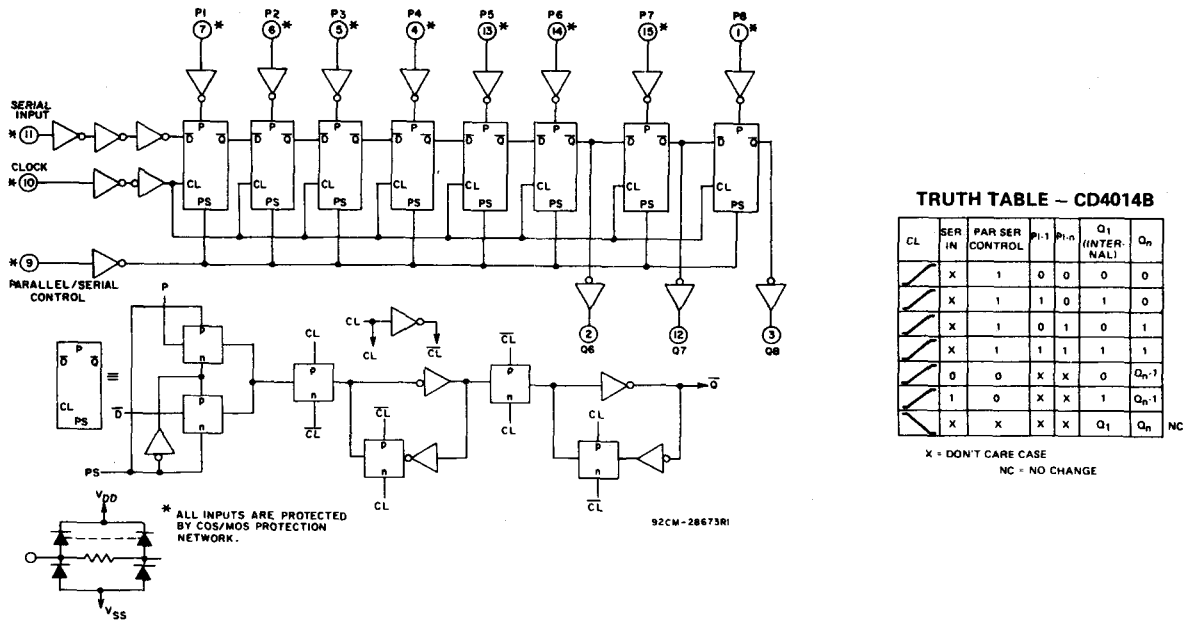


Fig. 1 - Logic diagram for CD4014B.

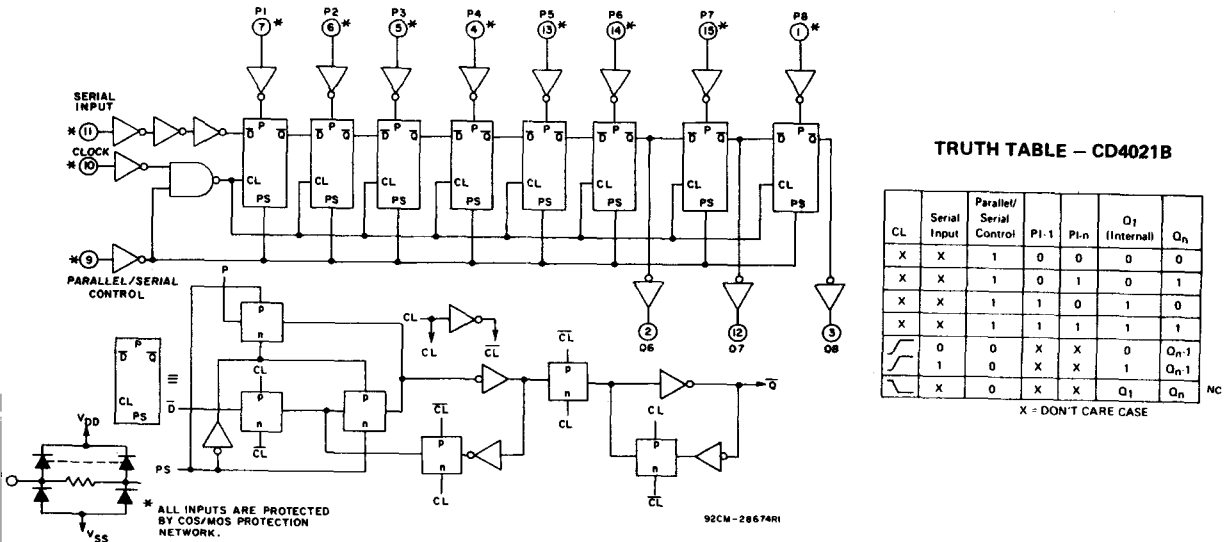


Fig. 2 - Logic diagram for CD4021B.

# CD4014B, CD4021B Types

## MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ ) (Voltages referenced to $V_{SS}$ Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10$ mA
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +80$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F, K)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:	
For $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE ( $T_A$ ):	
PACKAGE TYPES D, F, K, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 $\pm$ 1/32 inch (1.59 $\pm$ 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES ( $^\circ\text{C}$ )							UNITS
				Values at -55, +25, +125 Apply to D, F, K, H, Packages Values at -40, +25, +85 Apply to E Package							
	$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, $I_{DD}$ Max.	-	0.5	5	5	5	150	150	-	0.04	5	$\mu\text{A}$
	-	0.10	10	10	10	300	300	-	0.04	10	
	-	0.15	15	20	20	600	600	-	0.04	20	
	-	0.20	20	100	100	3000	3000	-	0.08	100	
Output Low (Sink) Current $I_{OL}$ Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, $I_{OH}$ Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, $V_{OL}$ Max.	-	0.5	5	0.05				-	0	0.05	V
	-	0.10	10	0.05				-	0	0.05	
	-	0.15	15	0.05				-	0	0.05	
Output Voltage: High-Level, $V_{OH}$ Min.	-	0.5	5	4.95				4.95	5	-	V
	-	0.10	10	9.95				9.95	10	-	
	-	0.15	15	14.95				14.95	15	-	
Input Low Voltage $V_{IL}$ Max.	0.5, 4.5	-	5	1.5				-	-	1.5	V
	1.9	-	10	3				-	-	3	
	1.5, 13.5	-	15	4				-	-	4	
Input High Voltage, $V_{IH}$ Min.	0.5, 4.5	-	5	3.5				3.5	7	-	V
	1.9	-	10	7				7	-	-	
	1.5, 13.5	-	15	11				11	-	-	
Input Current $I_{IN}$ Max.	-	0.18	18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	-	$\pm 10^{-5}$	$\pm 0.1$	$\mu\text{A}$

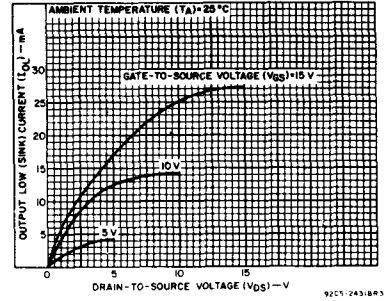


Fig. 3 - Typical output low (sink) current characteristics.

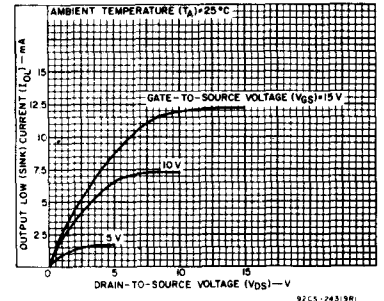


Fig. 4 - Minimum output low (sink) current characteristics.

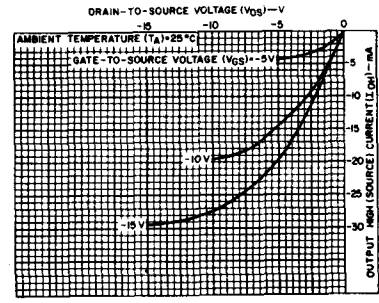


Fig. 5 - Typical output high (source) current characteristics.

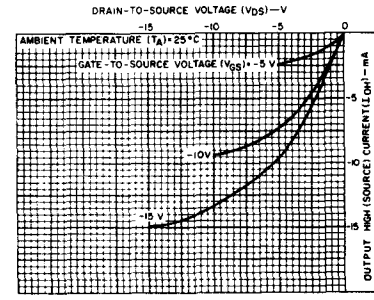


Fig. 6 - Minimum output high (source) current characteristics.

# CD4014B, CD4021B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at  $T_A=25^\circ\text{C}$ , Input  $t_r, t_f=20\text{ ns}$ ,  $C_L=50\text{ pF}$ ,  $R_L=200\text{ K}\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		$V_{DD}$ (V)	Min.	Typ.	
Propagation Delay Time, $t_{PLH}, t_{PHL}$	5	—	160	320	ns
	10	—	80	160	
	15	—	60	120	
Transition Time, $t_{THL}, t_{TLH}$	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Maximum Clock Input Frequency, $f_{CL}$	5	3	6	—	MHz
	10	6	12	—	
	15	8.5	17	—	
Minimum Clock Pulse Width, $t_W$	5	—	90	180	ns
	10	—	40	80	
	15	—	25	50	
Clock Rise and Fall Time, $t_r, t_f$ *	5	—	—	15	$\mu\text{s}$
	10	—	—	15	
	15	—	—	15	
Minimum Set-up Time, $t_s$ : Serial Input (ref. to CL)	5	—	60	120	ns
	10	—	40	80	
	15	—	30	60	
Parallel Inputs CD4014B (ref. to CL)	5	—	40	80	ns
	10	—	25	50	
	15	—	20	40	
Parallel Inputs CD4021B (ref. to P/S)	5	—	25	50	ns
	10	—	15	30	
	15	—	10	20	
Parallel/Serial Control CD4014B (ref. to CL)	5	—	90	180	ns
	10	—	40	80	
	15	—	30	60	
Minimum Hold Time, $t_H$ : Serial In, Parallel In, Parallel/Serial Control	5	—	—	0	ns
	10	—	—	0	
	15	—	—	0	
Minimum P/S Pulse Width, $t_{WH}$ (CD4021B)	5	—	80	160	ns
	10	—	40	80	
	15	—	25	50	
Minimum P/S Removal Time, $t_{REM}$ CD4021B (ref. to CL)	5	—	140	280	ns
	10	—	70	140	
	15	—	50	100	
Average Input Capacitance, $C_I$	Any Input	—	5	7.5	pF

\* If more than one unit is cascaded  $t_r, t_f$  should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

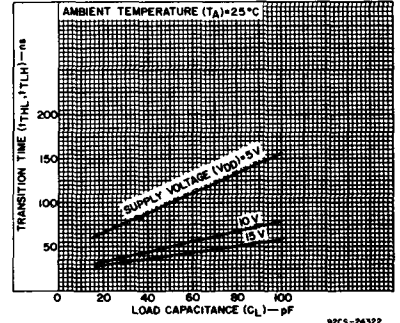


Fig. 7 — Typical transition time as a function of load capacitance.

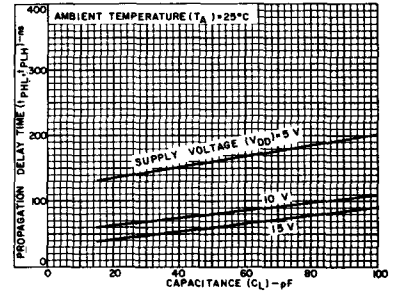


Fig. 8 — Typical propagation delay time as a function of load capacitance.

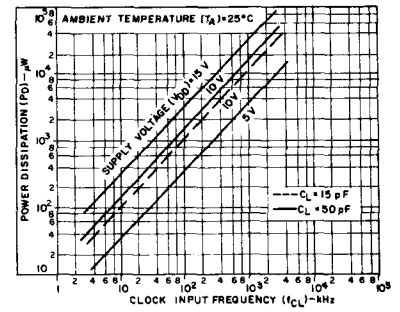


Fig. 9 — Typical dynamic power dissipation as a function of clock input frequency.

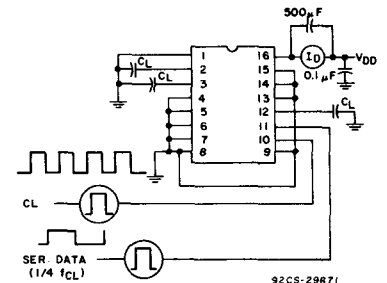


Fig. 10 — Dynamic power dissipation test circuit.

# CD4014B, CD4021B Types

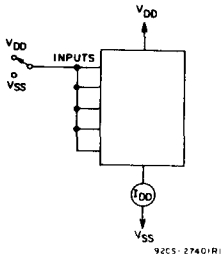


Fig. 11 - Quiescent device current test circuit.

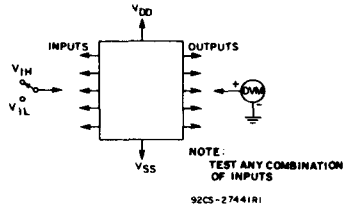


Fig. 12 - Input voltage test circuit.

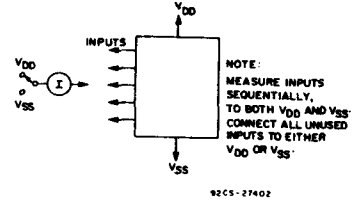
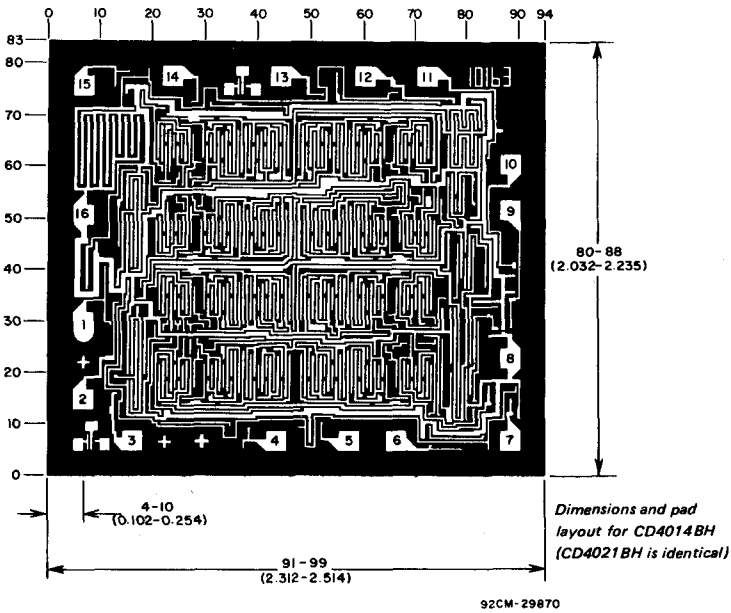


Fig. 13 - Input current test circuit.



The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of  $-3$  mils to  $+16$  mils applicable to the nominal dimensions shown.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).