CMOS Synchronous Programmable 4-Bit Counters

High-Voltage Types (20-Volt Rating)

CD40160B – Decade with Asynchronous Clear
CD40161B – Binary with Asynchronous Clear
CD40162B – Decade with Synchronous Clear
CD40163B – Binary with Synchronous Clear

RCA-CD40160B, CD40161B, CD40162B, and CD40163B are 4-bit synchronous programmable counters. The CLEAR function of the CD40162B and CD40163B is synchronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low on the next positive CLOCK edge. The CLEAR function of the CD40160B and CD40161B is asynchronous and a low level at the $\overline{\text{CLEAR}}$ input sets all four outputs low regardless of the state of the CLOCK, $\overline{\text{LOAD}}$, or ENABLE inputs. A low level at the $\overline{\text{LOAD}}$ input disables the counter and causes the output to agree with the setup data after the next CLOCK pulse regardless of the conditions of the ENABLE inputs.

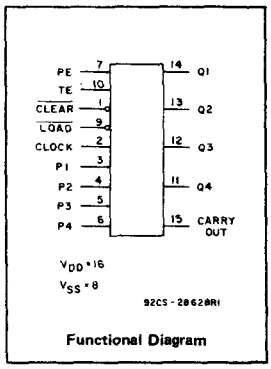
The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output (C_{OUT}). Counting is enabled when both PE and TE inputs are high. The TE input is fed forward to enable C_{OUT}. This enabled output produces a positive output pulse with a duration approximately equal to the positive portion of the Q1 output. This positive overflow carry pulse can be used to enable successive cascaded stages. Logic transitions at the PE or TE inputs may occur when the clock is either high or low.

The CD40160B, CD40161B, CD40162B, and CD40163B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

The CD40160B through CD40163B types are functionally equivalent to and pin-compatible with the TTL counter series 74LS160 through 74LS163 respectively.

Features:

- Internal look-ahead for fast counting
- Carry output for cascading
- Synchronously programmable
- Clear asynchronous input (CD40160B, CD40161B)
- Clear synchronous input (CD40162B, CD40163B)
- Synchronous load control input
- Low-power TTL compatibility
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at V_{DD} = 5 V, 2 V at V_{DD} = 10 V, 2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



Functional Diagram

Applications:

- Programmable binary and decade counting
- Counter control/timers
- Frequency dividing

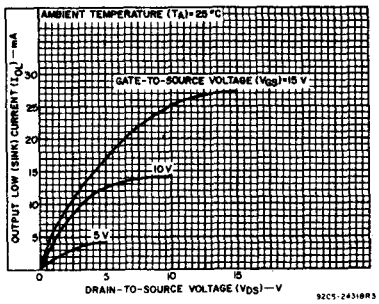


Fig. 1— Typical output low (sink) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

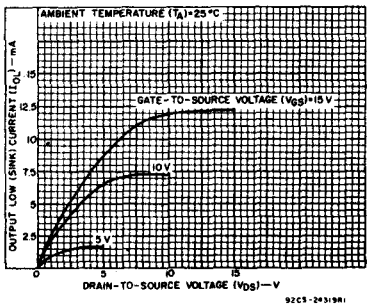


Fig. 2— Minimum output low (sink) current characteristics.

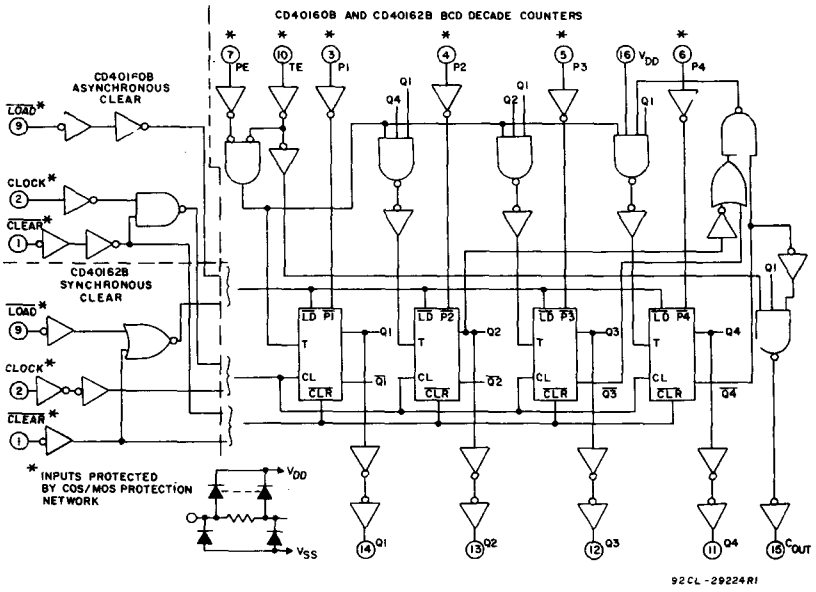


Fig. 3– Logic diagrams for CD40160B and CD40162B BCD decade counters.

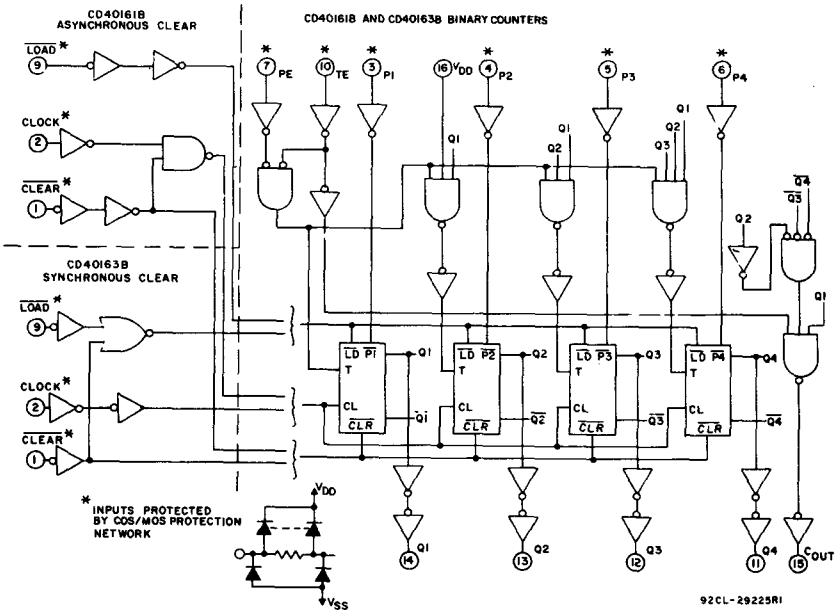


Fig. 4– Logic diagrams for CD40161B and CD40163B binary counters.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply Voltage Range (Full T_A = Full Package-Temperature Range)	–	3	18	V
Setup Time: t_{SU} Data to Clock	5	240	–	ns
	10	90	–	
	15	60	–	
$\overline{\text{Load}}$ to Clock	5	240	–	ns
	10	90	–	
	15	60		
PE or TE to Clock	5	340	–	ns
	10	140	–	
	15	100	–	
$\overline{\text{Clear}}$ to Clock (CD40162B, CD40163B)	5	340	–	ns
	10	140	–	
	15	100		
All Hold Times, t_H	5	0	–	ns
	10	0	–	
	15	0	–	
$\overline{\text{Clear}}$ Removal Time, t_{rem} (CD40160B, CD40161B)	5	200	–	ns
	10	100	–	
	15	70	–	
$\overline{\text{Clear}}$ Pulse Width, t_{WL} (CD40160B, CD40161B)	5	170	–	ns
	10	70	–	
	15	50	–	
Clock Input Frequency, f_{CL}	5	–	2	MHz
	10	–	5.5	
	15	–	8	
Clock Pulse Width, t_W	5	170	–	ns
	10	70	–	
	15	50	–	
Clock Rise or Fall Time, t_rCL or t_fCL	5	–	200	μs
	10	–	70	
	15	–	15	

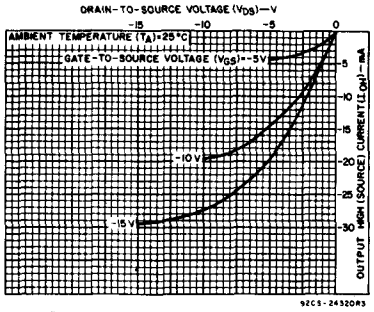


Fig. 5— Typical output high (source) current characteristics.

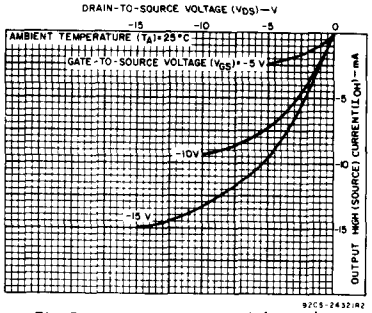


Fig. 6— Minimum output high (source) current characteristics.

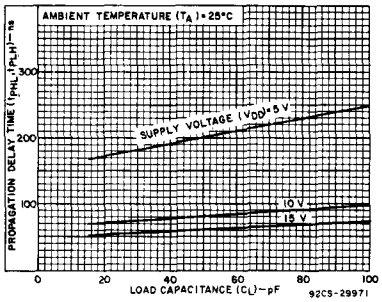


Fig. 7— Typical propagation delay time as a function of load capacitance (CLOCK to Q).

TRUTH TABLE

CLOCK	$\overline{\text{CLR}}$	$\overline{\text{LOAD}}$	PE	TE	OPERATION
⎍	1	0	X	X	PRESET
⎍	1	1	0	X	NC
⎍	1	1	X	0	NC
⎍	1	1	1	1	COUNT
X	0	X	X	X	RESET (CD40160B, CD40161B)
⎍	0	X	X	X	RESET (CD40162B, CD40163B)
⎎	1	X	X	X	NC (CD40162B, CD40163B)

1 = HIGH LEVEL 0 = LOW LEVEL X = DON'T CARE NC = NO CHANGE

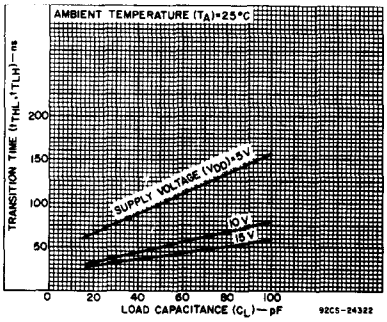


Fig. 8— Typical transition time as a function of load capacitance.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at -55, +25, +125 Apply to D, F, K, H, Packages Values at -40, +25, +85 Apply to E Packages							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	–	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	–	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	–	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

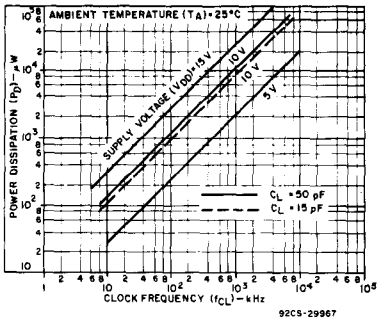


Fig. 9— Typical power dissipation as a function of CLOCK frequency.

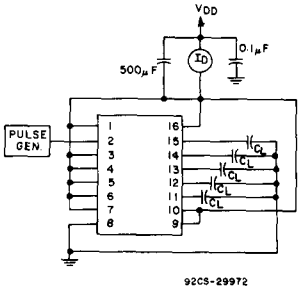


Fig. 10— Dynamic power dissipation test circuit.

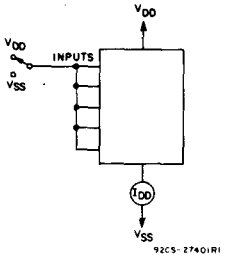


Fig. 11— Quiescent-device-current test circuit.

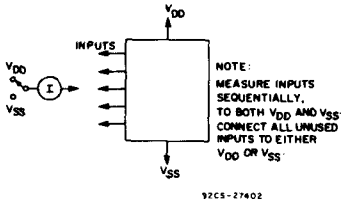


Fig. 12— Input-current test circuit.

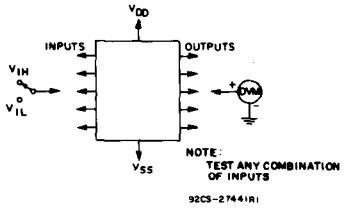
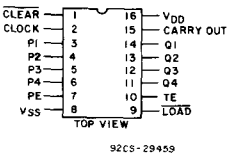


Fig. 13— Input-voltage test circuit.

TERMINAL ASSIGNMENT



DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C;
Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS ALL TYPES*			UNITS
		Min.	Typ.	Max.	
CLOCK OPERATION					
Propagation Delay Time, t_{PHL},t_{PLH} Clock to Q	5	–	200	400	ns
	10	–	80	160	
	15	–	60	120	
Clock to C_{OUT}	5	–	225	450	ns
	10	–	95	190	
	15	–	70	140	
TE to C_{OUT}	5	–	125	250	ns
	10	–	55	110	
	15	–	40	80	
Minimum Setup Time, t_{SU} Data to Clock	5	–	120	240	ns
	10	–	45	90	
	15	–	30	60	
$\overline{\text{Load}}$ to Clock	5	–	120	240	ns
	10	–	45	90	
	15	–	30	60	
PE to TE to Clock	5	–	170	340	ns
	10	–	70	140	
	15	–	50	100	
Minimum Hold Time, t_H	5	–	–	0	ns
	10	–	–	0	
	15	–	–	0	
Transition Time, t_{THL},t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Clock Pulse Width, t_W	5	–	85	170	ns
	10	–	35	70	
	15	–	25	50	
Maximum Clock Frequency, f_{CL}	5	2	3	–	MHz
	10	5.5	8.5	–	
	15	8	12	–	
Maximum Clock Rise or Fall Time,† t_rCL, t_{fCL}	5	200	–	–	μs
	10	70	–	–	
	15	15	–	–	
CLEAR OPERATION					
Propagation Delay Time, t_{PHL} (CD40160B, CD40161B) $\overline{\text{Clear}}$ to Q	5	–	250	500	ns
	10	–	110	220	
	15	–	80	160	
Minimum Setup Time, t_{SU} (CD40162B, CD40163B) $\overline{\text{Clear}}$ to Clock	5	–	170	340	ns
	10	–	70	140	
	15	–	50	100	
Minimum Hold Time, t_H (CD40162B, CD40163B) $\overline{\text{Clear}}$ to Clock	5	–	–	0	ns
	10	–	–	0	
	15	–	–	0	
Minimum $\overline{\text{Clear}}$ Removal Time, t_{rem} (CD40160B, CD40161B)	5	–	100	200	ns
	10	–	50	100	
	15	–	35	70	
Minimum $\overline{\text{Clear}}$ Pulse Width, t_{WL} (CD40160B, CD40161B)	5	–	85	170	ns
	10	–	35	70	
	15	–	25	50	

* Except as noted.
† If more than one unit is cascaded in the parallel clocked application, t_rCL should be made less than or equal to the sum of the fixed propagation delay at 50 pF and the transition time of the carry output driving stage for the estimated capacitive load.

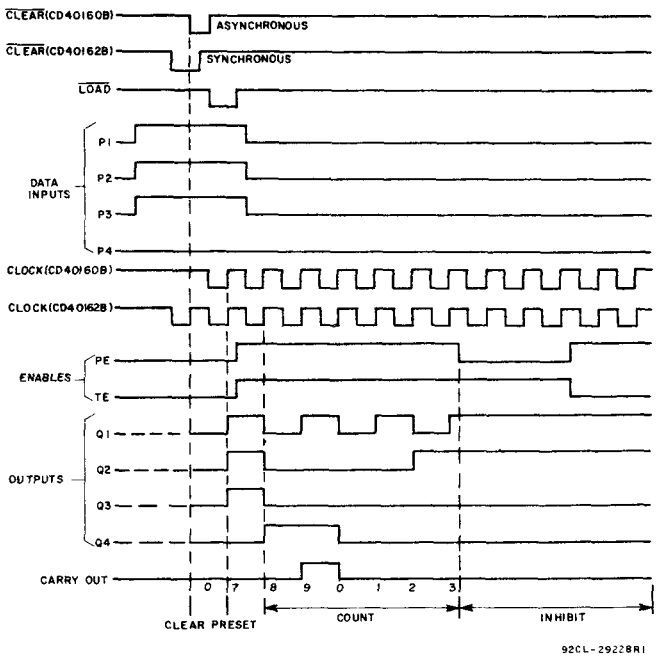


Fig. 14— Timing diagram for CD40160B, CD40162B.

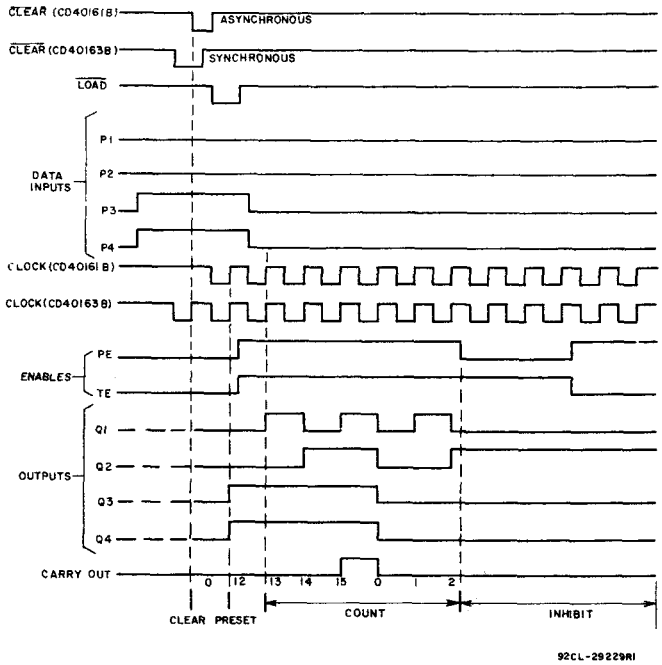


Fig. 15— Timing diagram for CD40161B, CD40163B.

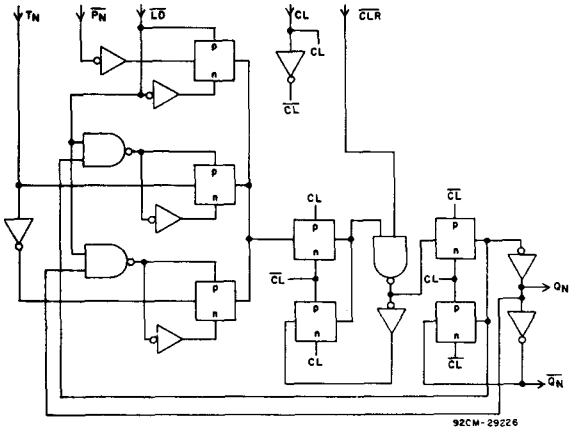


Fig. 16– Detail of flip-flops of CD40160B and CD40161B (asynchronous clear).

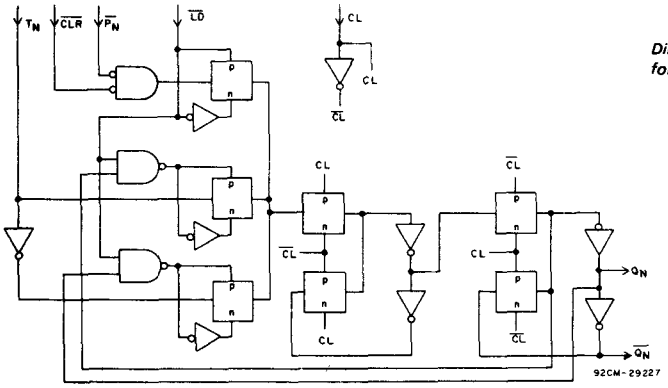
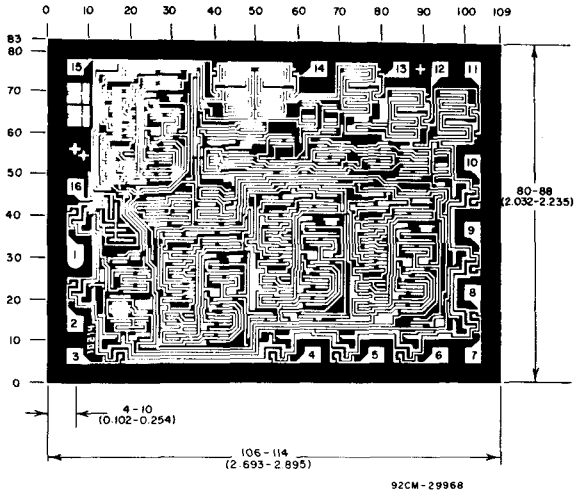


Fig. 17– Detail of flip-flops for CD40162B and CD40163B (synchronous clear).



Dimensions and pad layout for CD40160BH. Dimensions and pad layout for CD40161BH, CD40162BH, and CD40163BH are identical.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

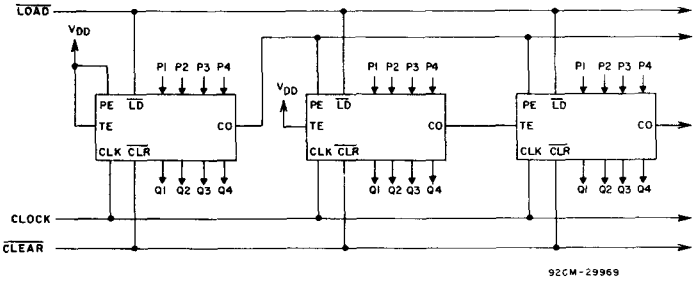


Fig. 18 – Cascaded counter packages in the parallel-clocked mode.

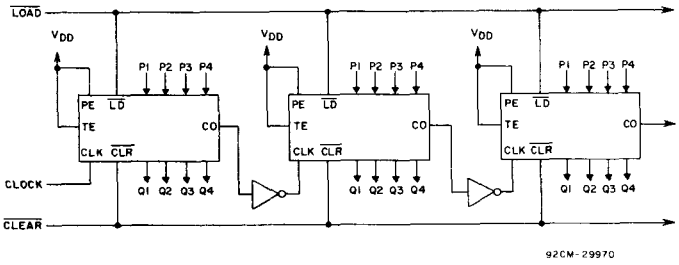


Fig. 19 – Cascaded counter packages in the ripple-clocked mode.