Pulse width modulation circuit

Description：

CD4017 is a 5th order Johnson decoding counter with 10 decoding outputs, CLOCK, RE, INH inputs, and a Schmidt trigger with pulse shaping function at the clock input, which has no limit on the rise and fall time of input clock pulses. INH is low level, and the counter counts on the rising edge of the clock; On the contrary, the counting function is invalid. RE is high level, and the counter is reset to zero. Its main characteristics are as follows:

Features：

-Fully static operation

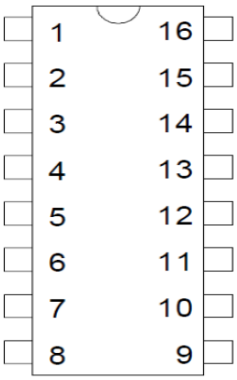
-5V, 10V, 15V parameter standard range

-Standard symmetrical output characteristics

-Working within the industrial standard temperature range (-40~85 ℃) -100% static current tested at 20V

-Packaging form: DIP16/SOP16

Pin Assignment：

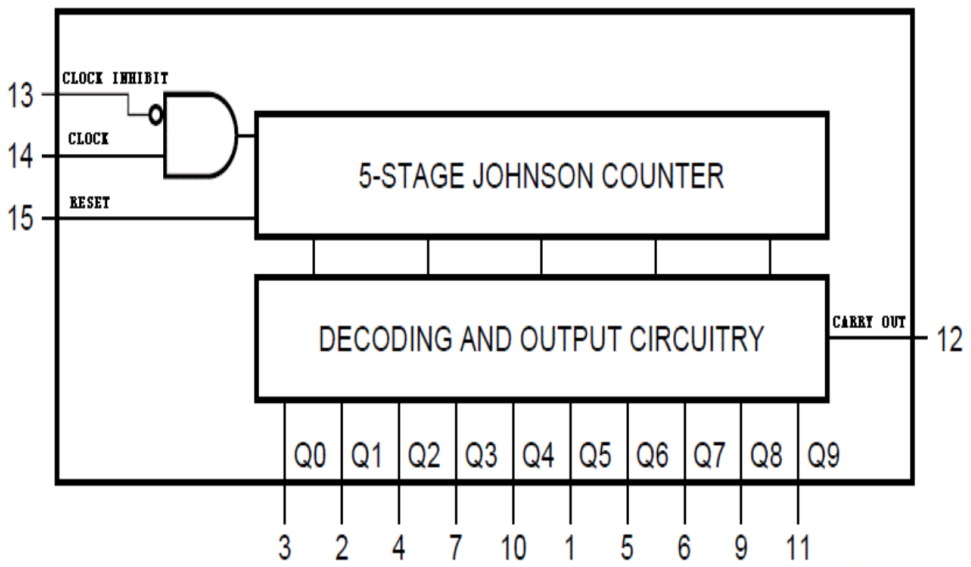


Pin No.	Symbol	Pin Definition	Pin No.	Symbol	Pin Definition
1	Q5	Decoding output terminal	16	VDD	power supply
2	Q1	Decoding output terminal	15	RESET	RESET
3	Q0	Decoding output terminal	14	CLOCK	CLOCK
4	Q2	Decoding output terminal	13	CLOCK INHIBIT	Clock suppression
5	Q6	Decoding output terminal	12	CARRY OUT	Carry output terminal
6	Q7	Decoding output terminal	11	Q9	Decoding output terminal
7	Q3	Decoding output terminal	10	Q4	Decoding output terminal
8	Vss	grounds	9	Q8	Decoding output terminal

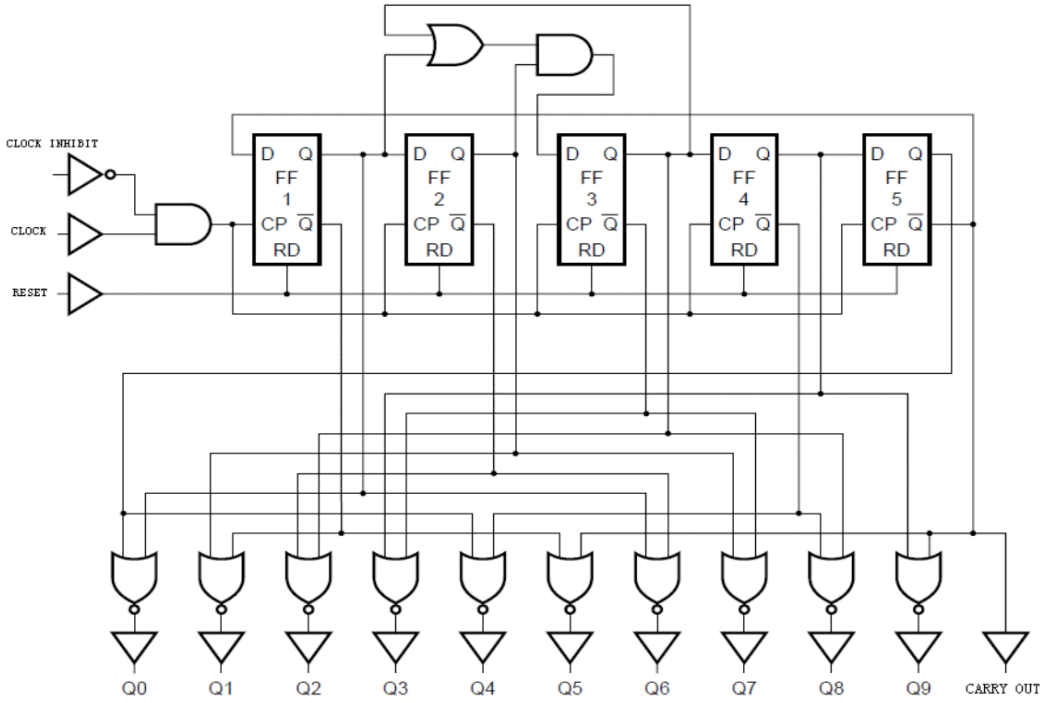
Absolute Maximum Ratings

parameter	symbol	limit value	unit
supply voltage	V_{DD}	-0.5~20	V
INPUT VOLTAGE	V_I	-0.5~VDD+0.5	V
Input and output current	±I	±10	mA
consumption	P_D	500	mW
Output power consumption	P	100	mW
Ambient Temperature	Tamb	-40~+85	℃
Storage temperature	Tstg	-65~+150	℃
welding temperature	T_L	250	℃

Functional Block Diagram



Logic diagram



Truth table

Input			Operation
MR	**CP0**	**$\overline{CP1}$**	
H	X	X	Q0=$\overline{Q}$5-9=H; Q1 to Q9=L
L	H	↓	counter advances
L	↑	L	counter advances
L	L	X	no change
L	X	H	no change
L	H	↑	no change
L	↓	L	no change

Note:

H=HIGH voltage level; L=LOW voltage level; X=don't care;

↑=positive-going transition; ↓=negative-going transition.

Recommended Operating Conditions

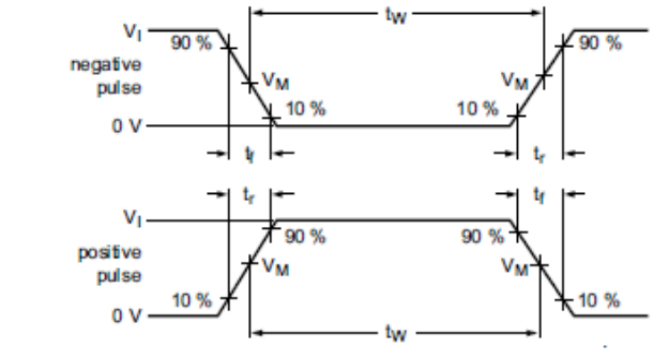
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
supply voltage	V_{DD}	-	3	-	15	V
ambient temperature	T_{amb}	in free air	-40	-	+105	℃
clock input frequency	f_{CL}	V_{DD}=5V	-	-	2.5	MHz
		V_{DD}=10V	-	-	5	MHz
		V_{DD}=15V	-	-	5.5	MHz
clock pulse width	t_w	V_{DD}=5V	200	-	-	ns
		V_{DD}=10V	90	-	-	ns
		V_{DD}=15V	60	-	-	ns
clock rise and fall time	t_{rCL}, t_{fCL}	V_{DD}=5V	unlimited			-
		V_{DD}=10V				-
		V_{DD}=15V				-
clock inhibit setup time	t_s	V_{DD}=5V	230	-	-	ns
		V_{DD}=10V	100	-	-	ns
		V_{DD}=15V	70	-	-	ns
reset pulse width	t_{RW}	V_{DD}=5V	260	-	-	ns
		V_{DD}=10V	110	-	-	ns
		V_{DD}=15V	60	-	-	ns
reset removal time	t_{rec}	V_{DD}=5V	400	-	-	ns
		V_{DD}=10V	280	-	-	ns
		V_{DD}=15V	150	-	-	ns

DC Characteristics

(T_{amb}=25℃, voltages are referenced to V_{SS} (ground=0V), unless otherwise specified.)

Parameter	Symbol	Conditions (V)			T_{amb}=25℃			Unit
		V_O	V_{IN}	V_{DD}	Min.	Typ.	Max.	
supply current	I_{DD}	-	0, 5	5	-	0.04	5	uA
		-	0, 10	10	-	0.04	10	uA
		-	0, 15	15	-	0.04	20	uA
LOW-level output current	I_{OL}	0.4	0, 5	5	0.51	1	-	mA
		0.5	0, 10	10	1.3	2.6	-	mA
		1.5	0, 15	15	3.4	6.8	-	mA
HIGH-level output current	I_{OH}	4.6	0, 5	5	-0.51	-1	-	mA
		2.5	0, 5	5	-1.6	-3.2	-	mA
		9.5	0, 10	10	-1.3	-2.6	-	mA
		13.5	0, 15	15	-3.4	-6.8	-	mA
LOW-level output voltage	V_{OL}	-	0, 5	5	-	0	0.05	V
		-	0, 10	10	-	0	0.05	V
		-	0, 15	15	-	0	0.05	V
HIGH-level output voltage	V_{OH}	-	0, 5	5	4.95	5	-	V
		-	0, 10	10	9.95	10	-	V
		-	0, 15	15	14.95	15	-	V
LOW-level input voltage	V_{IL}	0.5, 4.5	-	5	-	-	1.5	V
		1, 9	-	10	-	-	3	V
		1.5, 13.5	-	15	-	-	4	V
HIGH-level input voltage	V_{IH}	0.5, 4.5	-	5	3.5	-	-	V
		1, 9	-	10	7	-	-	V
		1.5, 13.5	-	15	11	-	-	V
input leakage current	I_I	-	0, 15	15	-	$\pm10^{-5}$	±0.1	uA

AC Testing Circuit



a. Input waveforms

b. Test circuit

Figure 6. Test circuit for switching times

Definitions for test circuit:

DUT=Device Under Test.

C_L=Load capacitance including jig and probe capacitance.

R_T=Termination resistance should be equal to the output impedance Z_o of the pulse generator.

AC Testing Waveforms

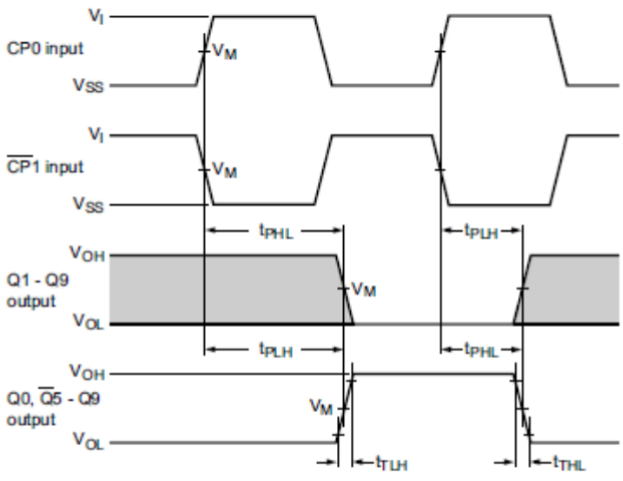
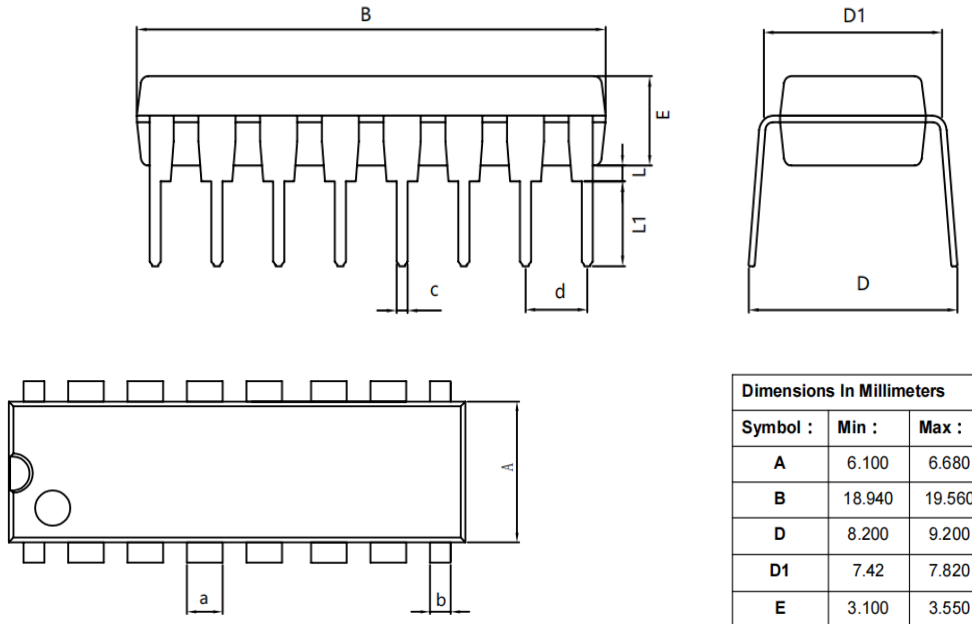


Figure 7. Waveforms showing the propagation delays for CP0, $\overline{CP1}$ to Qn, $\overline{Q5}$-9 outputs and the output transition times

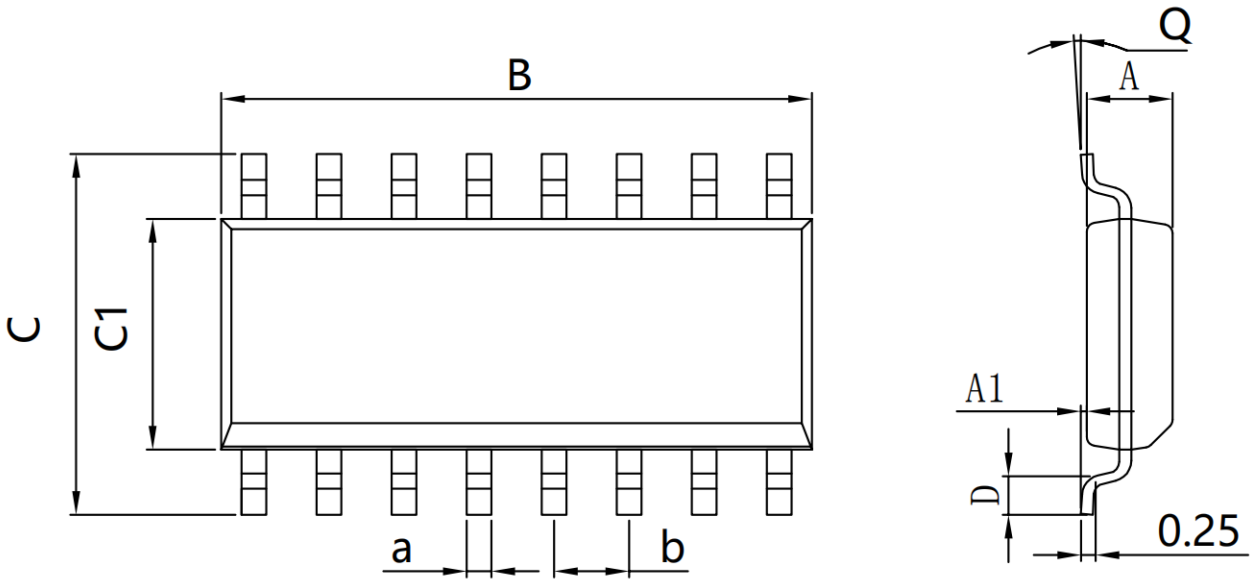
PACKAGE MECHANICAL DATA

DIP16



Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	6.100	6.680	L	0.500	0.800
B	18.940	19.560	a	1.524 TYP	
D	8.200	9.200	b	0.889 TYP	
D1	7.42	7.820	c	0.457 TYP	
E	3.100	3.550	d	2.540 TYP	
L	0.500	0.800			

SOP16



Dimensions In Millimeters					
Symbol :	Min :	Max :	Symbol :	Min :	Max :
A	1.225	1.570	D	0.400	0.950
A1	0.100	0.250	Q	0°	8°
B	9.800	10.00	a	0.420 TYP	
C	5.800	6.250	b	1.270 TYP	
C1	3.800	4.000			