

CMOS Hex 'D'-Type Flip-Flop

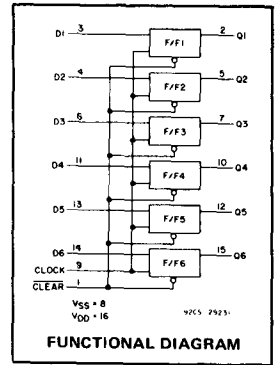
High-Voltage Types (20-Volt Rating)

The RCA-CD40174B consists of six identical 'D'-type flip-flops having independent DATA inputs. The CLOCK and CLEAR inputs are common to all six units. Data is transferred to the Q outputs on the positive-going transition of the clock pulse. All six flip-flops are simultaneously reset by a low level on the CLEAR input.

The CD40174B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- 5-V, 10-V, and 15-V parametric rating
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range): 1 V at $V_{DD} = 5$ V
2 V at $V_{DD} = 10$ V
2.5 V at $V_{DD} = 15$ V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"



MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT	± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)	500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F, K)	500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/ $^\circ\text{C}$ to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:	
For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	-55 to $+125^\circ\text{C}$
PACKAGE TYPE E	-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 \pm 1/32 inch (1.59 \pm 0.79 mm) from case for 10 s max.	$+265^\circ\text{C}$

Applications:

- Shift Registers
- Buffer/Storage Registers
- Pattern Generators

TRUTH TABLE FOR 1 OF 6 FLIP-FLOPS

CLOCK	INPUTS		OUTPUT
	DATA	CLEAR	
	0	1	0
	1	1	1
	X	1	NC
X	X	0	0

1 = High Level
0 = Low Level
X = Don't Care
NC = No Change

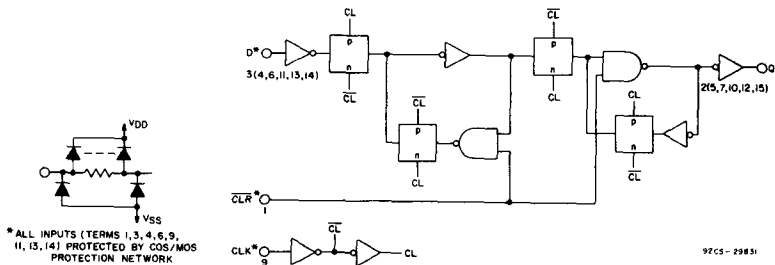


Fig. 1 - Logic diagram (1 of 6 flip-flops).

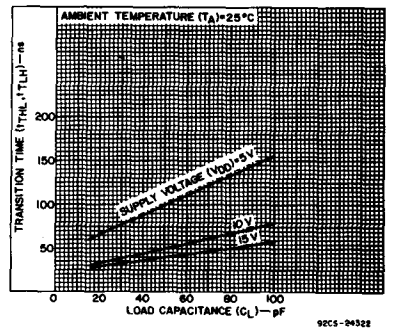


Fig. 2 - Typical transition time as a function of load capacitance.

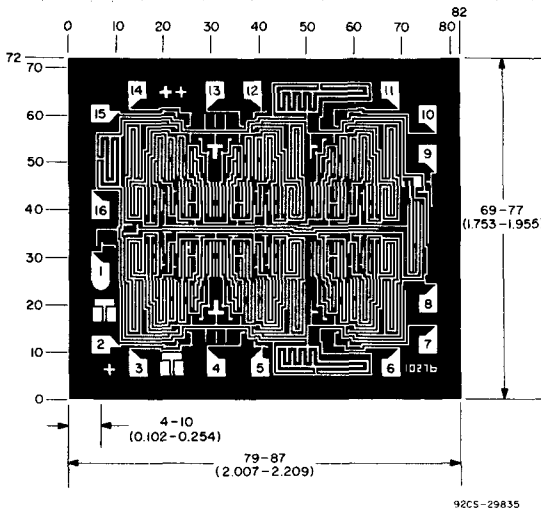
* ALL INPUTS (TERMS 1, 3, 4, 6, 9, 11, 13, 14) PROTECTED BY COS/MOS PROTECTION NETWORK

CD40174B Types

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)	—	3	18	V
Data Setup Time, t_{SU}	5 10 15	40 20 10	— — —	ns
Data Hold Time, t_H	5 10 15	80 40 30	— — —	ns
Clock Input Frequency, f_{CL}	5 10 15	— dc —	3.5 6 8	MHz
Clock Input Rise or Fall Time, t_{rCL} , t_{fCL}	5 10 15	— — —	15 15 15	μs
Clock Input Pulse Width, t_{WL} , t_{WH}	5 10 15	130 60 40	— — —	ns
Clear Pulse Width, t_{WL}	5 10 15	100 50 40	— — —	ns
Clear Removal Time, t_{REM}	5 10 15	0 0 0	— — —	ns



Dimensions and pad layout for CD40174BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to $+16$ mils applicable to the nominal dimensions shown.

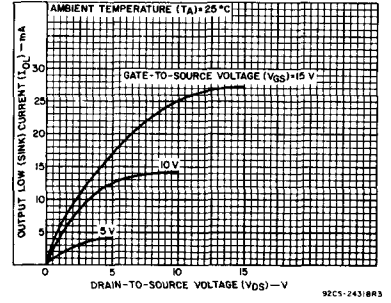


Fig. 3—Typical output low (sink) current characteristics.

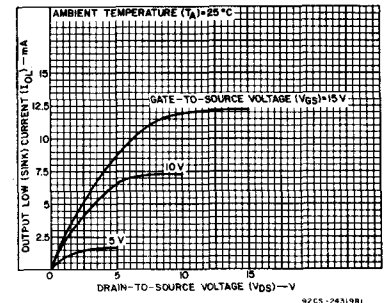


Fig. 4—Minimum output low (sink) current characteristics.

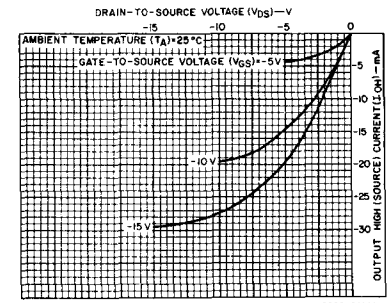


Fig. 5—Typical output high (source) current characteristics.

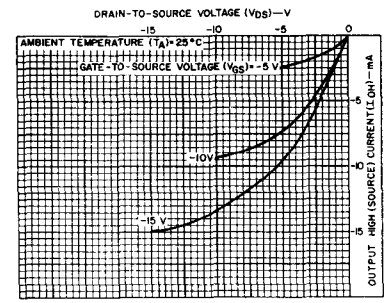


Fig. 6—Minimum output high (source) current characteristics.

CD40174B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V _O (V)	V _{IN} (V)	V _{DD} (V)	Values at -55, +25, +125 Apply to D, F, K, H Packages				Values at -40, +25, +85 Apply to E Package			
				-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I _{DD} Max.	-	0,5	5	1	1	30	30	-	0.02	1	μA
	-	0,10	10	2	2	60	60	-	0.02	2	
	-	0,15	15	4	4	120	120	-	0.02	4	
	-	0,20	20	20	20	600	600	-	0.04	20	
Output Low (Sink) Current I _{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, I _{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
Output Voltage: Low-Level, V _{OL} Max.	-	0,5	5	0.05				-	0	0.05	V
	-	0,10	10	0.05				-	-	0.05	
	-	0,15	15	0.05				-	0	0.05	
Output Voltage: High-Level, V _{OH} Min.	-	0,5	5	4.95				4.95	5	-	V
	-	0,10	10	9.95				9.95	10	-	
	-	0,15	15	14.95				14.95	15	-	
Input Low Voltage, V _{IL} Max.	0.5, 4.5	-	5	1.5				-	-	1.5	V
	1.9	-	10	3				-	-	3	
	1.5, 13.5	-	15	4				-	-	4	
Input High Voltage, V _{IH} Min.	0.5, 4.5	-	5	3.5				3.5	-	-	V
	1.9	-	10	7				7	-	-	
	1.5, 13.5	-	15	11				11	-	-	
Input Current I _{IN} Max.	-	0,18	18	±0.1	±0.1	±1	±1	-	±10 ⁻⁵	±0.1	μA

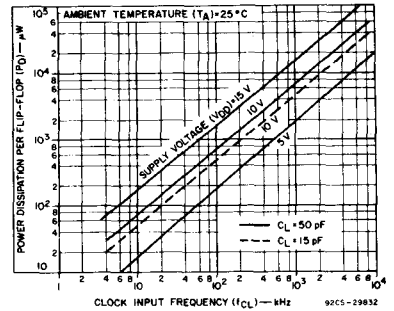


Fig. 7—Typical dynamic power dissipation as a function of CLOCK frequency.

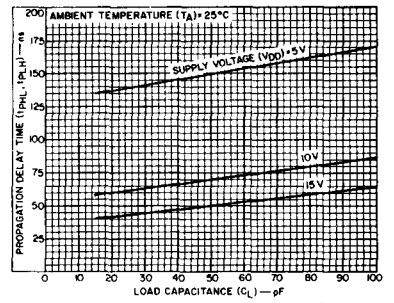


Fig. 8—Typical propagation delay time (CLOCK to OUTPUT) as a function of load capacitance.

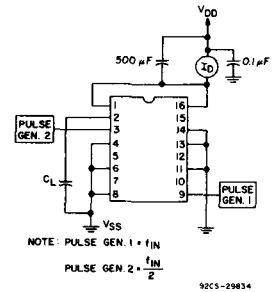


Fig. 9—Dynamic power dissipation test circuit.

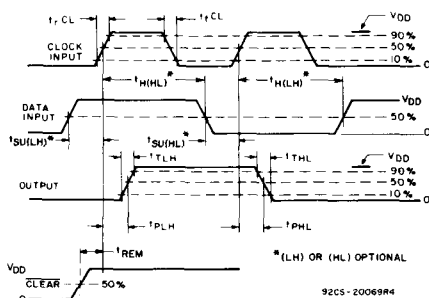


Fig. 10—Definition of setup, hold, propagation delay, and removal times.

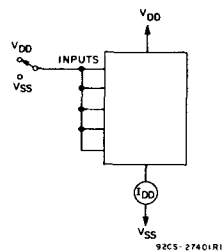


Fig. 11—Quiescent device current test circuit.

CD40174B Types

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$;
 Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$, $R_L \approx 200\text{ k}\Omega$

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS			UNITS
		Min.	Typ.	Max.	
Propagation Delay Time Clock to Output, t_{PHL}, t_{PLH}	5	—	150	300	ns
	10	—	70	140	
	15	—	50	100	
Clear to Output, t_{PHL}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Transition Time, t_{THL}, t_{TLH}	5	—	100	200	ns
	10	—	50	100	
	15	—	40	80	
Minimum Pulse Width, Clock, t_{WL}, t_{WH}	5	—	65	130	ns
	10	—	30	60	
	15	—	20	40	
Clear, t_{WL}	5	—	50	100	ns
	10	—	25	50	
	15	—	20	40	
Minimum Data Setup Time, t_{SU}	5	—	20	40	ns
	10	—	10	20	
	15	—	0	10	
Minimum Data Hold Time, t_H	5	—	40	80	ns
	10	—	20	40	
	15	—	15	30	
Maximum Clock Frequency, f_{CL}	5	3.5	7	—	MHz
	10	6	12	—	
	15	8	16	—	
Maximum Clock Rise or Fall Time, t_{rCL}, t_{fCL}	5	15	—	—	μs
	10	15	—	—	
	15	15	—	—	
Input Capacitance, C_{iN}	Clear	—	25	40	pF
	All other	—	5	7.5	
Minimum Clear Removal Time, t_{REM}	5	—	-40	0	ns
	10	—	-15	0	
	15	—	-10	0	

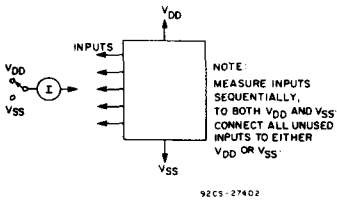


Fig. 12 — Input current test circuit.

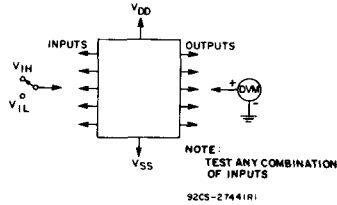
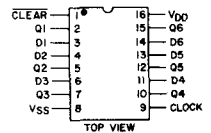


Fig. 13 — Input voltage test circuit.

TERMINAL ASSIGNMENT



92CS-29232