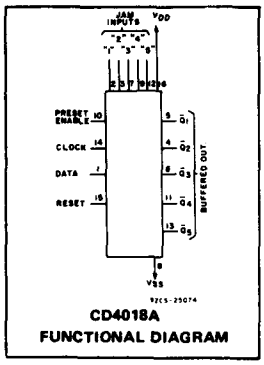
CMOS Presettable Divide-By-'N' Counter

The RCA-CD4018A types consist of 5 Johnson-Counter stages, buffered $\overline{Q}$ outputs from each stage, and counter preset control gating. CLOCK, RESET, DATA, PRESET ENABLE, and 5 individual JAM inputs are provided. Divide by 10, 8, 6, 4, or 2 counter configurations can be implemented by feeding the $\overline{Q}5$, $\overline{Q}4$, $\overline{Q}3$, $\overline{Q}2$, $\overline{Q}1$ signals, respectively, back to the DATA input. Divide-by-9, 7, 5, or 3 counter configurations can be implemented by the use of a CD4011A gate package to properly gate the feedback connection to the DATA input. Divide-by functions greater than 10 can be achieved by use of multiple CD4018A units. The counter is advanced one count at the positive clock-signal transition. A high RESET signal clears the counter to an all-zero condition. A high PRESET-ENABLE signal allows information on the JAM inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4018A
FUNCTIONAL DIAGRAM

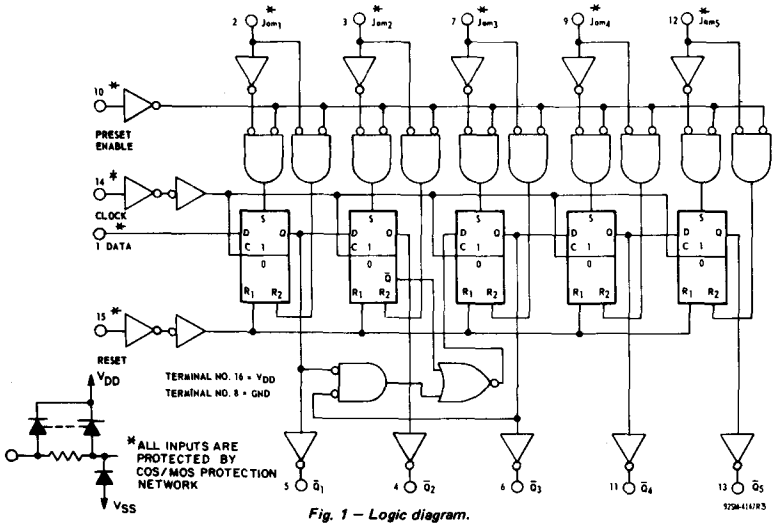


Fig. 1 – Logic diagram.

("DATA" INPUT TIED TO $\overline{Q}_5$ FOR DECADE COUNTER CONFIGURATION)

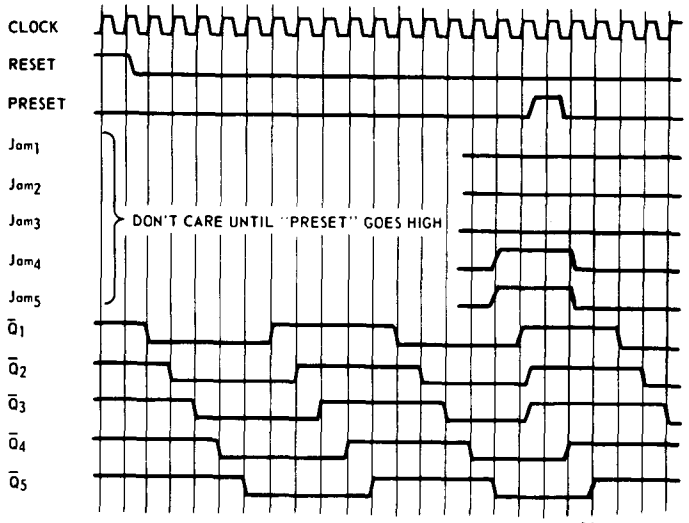


Fig. 2 – Timing diagram. 92SS-4148R2

Features:

- Medium speed operation . . . . 5 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V
- Fully static operation
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2 counters
- Fixed and programmable counters *greater than* 10
- Programmable decade counters
- Divide-by-"N" counters/frequency synthesizers
- Frequency division
- Counter control/timers

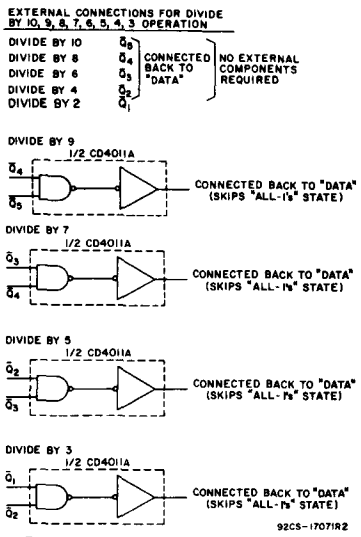


Fig. 3 – External connections for divide by 10, 9, 8, 7, 6, 5, 4, 3, 2 operation.

CD4018A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
PACKAGE TYPE E . . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D, F, K, H Packages			*E Package*			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLOCKED OPERATION									
Propagation Delay Time; t_{PLH}, t_{PHL} To $\overline{Q}_5$ Output		5	–	350	1000	–	350	1300	ns
		10	–	125	250	–	125	300	
To Other Outputs		5	–	500	1200	–	500	1600	
		10	–	200	400	–	200	500	
Transition Time; t_{THL}, t_{TLH} To $\overline{Q}_5$ Output		5	–	100	300	–	100	350	ns
		10	–	50	150	–	50	200	
To Other Outputs		5	–	300	900	–	300	1200	ns
		10	–	125	350	–	125	450	
Maximum Clock Input Frequency, f_{CL}		5	1	2.5	–	0.6	2.5	–	MHz
		10	3	5	–	2	5	–	
Min. Clock Pulse Width, t_W		5	–	200	500	–	200	830	ns
		10	–	100	170	–	100	250	
Clock Rise & Fall Time; t_rCL, t_fCL		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Min. Data Input Set-Up Time, t_S		5	–	175	500	–	175	700	ns
		10	–	75	200	–	75	300	
Average Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
PRESET* OR RESET OPERATION									
Propagation Delay Time: t_{PLH}, t_{PHL} To $\overline{Q}_5$ Output		5	–	350	1000	–	350	1300	ns
		10	–	125	250	–	125	300	
To Other Outputs		5	–	500	1200	–	500	1600	
		10	–	200	400	–	200	500	
Min. Preset or Reset Pulse Width t_W		5	–	200	500	–	200	830	ns
		10	–	100	165	–	100	250	
Min. Preset or Reset Removal Time		5	–	300	750	–	300	1000	
		10	–	100	225	–	100	275	

* At PRESET ENABLE OR JAM Inputs.

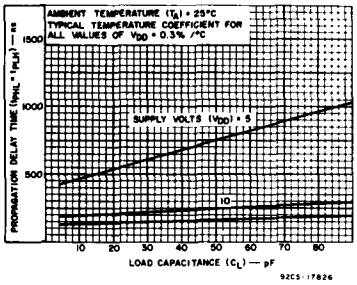


Fig. 4 – Typical propagation delay time vs. load capacitance for decoded outputs.

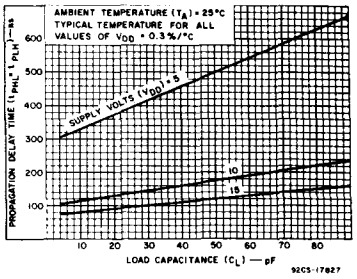


Fig. 5 – Typical propagation delay time vs. load capacitance for $\overline{Q}_5$ output.

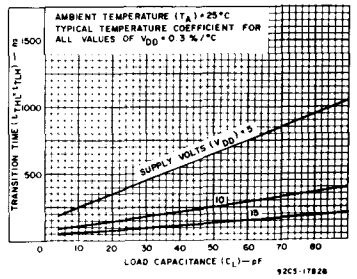


Fig. 6 – Typical transition time vs. load capacitance for decoded outputs.

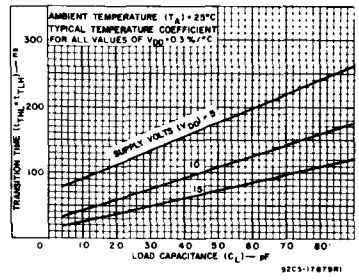


Fig. 7 – Typical transition time vs. load capacitance for $\overline{Q}_5$ output.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5	500	–	700	–	ns
	10	200	–	300	–	
Clock Pulse Width, t_W	5	500	–	830	–	ns
	10	170	–	250	–	
Clock Input Frequency, f_{CL}	5	dc	1	dc	0.6	MHz
	10	dc	3	dc	2	
Clock Rise and Fall Time, t_rCL, t_fCL	5	–	15	–	15	μs
	10	–	15	–	15	
Preset or Reset Pulse Width, t_W	5	500	–	830	–	ns
	10	165	–	250	–	
Preset or Reset Removal Time	5	750	–	1000	–	ns
	10	225	–	275	–	

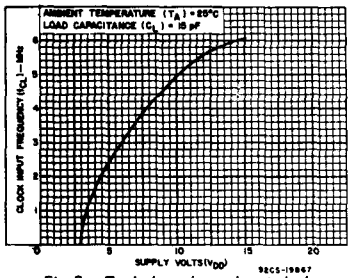


Fig. 8 – Typical maximum input clock frequency vs. supply voltage.

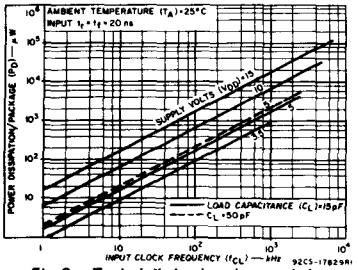


Fig. 9 – Typical dissipation characteristics

STATIC ELECTRICAL CHARACTERISTICS

Characteristic		Conditions			Limits at Indicated Temperatures (°C)								Units
					D, F, K, H Packages				*E Package*				
		V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	+25 Typ.	+25 Limit	+125	–40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.		–	–	5	5	0.3	5	300	50	0.5	50	700	μA
		–	–	10	10	0.5	10	600	100	1	100	1400	
		–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}		–	5	5	0 Typ.; 0.05 Max.								V
		–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}		–	0	5	4.95 Min.; 5 Typ.								
		–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.								V
		9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.								
		1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.								V
		9	–	10	1 Min.								
Inputs High, V_{NMH}		0.5	–	5	1 Min.								
		1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_DN Min.	$\bar{Q}_5$	0.5	–	5	0.18	0.4	0.15	0.105	0.095	0.4	0.08	0.065	mA
		0.5	–	10	0.45	1	0.35	0.25	0.3	1	0.25	0.2	
	$\bar{Q}_1,\bar{Q}_2$	0.5	–	5	0.06	0.1	0.05	0.035	0.03	0.1	0.025	0.02	
	$\bar{Q}_3,\bar{Q}_4$	0.5	–	10	0.25	0.4	0.2	0.14	0.18	0.4	0.15	0.12	
p-Channel (Source) I_DP Min.	$\bar{Q}_5$	4.5	–	5	-0.185	-0.4	-0.15	-0.105	-0.095	-0.4	-0.08	-0.065	
		9.5	–	10	-0.45	-1	-0.35	-0.25	-0.3	-1	-0.25	-0.2	
	$\bar{Q}_1,\bar{Q}_2$	4.5	–	5	-0.075	-0.15	-0.06	-0.04	-0.035	-0.15	-0.03	-0.024	
	$\bar{Q}_3,\bar{Q}_4$	9.5	–	10	-0.25	-0.4	-0.2	-0.14	-0.18	-0.4	-0.15	-0.12	
Input Leakage Current, I_{IL}, I_{IH} Max.		Any Input	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

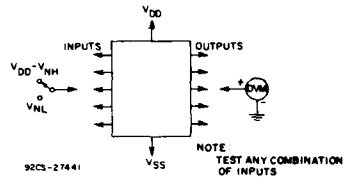
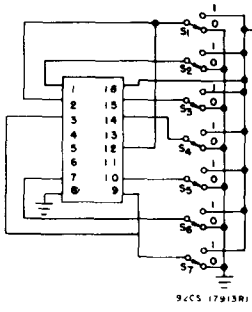


Fig. 10 – Noise-immunity test circuit



Test performed with the following sequence of "1's" and "0's" at each switch.

S_1	S_2	S_3	S_4	S_5	S_6	S_7
0	1	1	0	0	0	0
1	1	1	0	0	1	1
1	0	1	0	1	1	1
0	1	0	0	1	0	0
0	1	0	0	1	0	1
1	0	0	1	1	1	0
0	0	0	1	0	0	0
0	0	0	0	0	0	0
1	0	0	0	1	0	0
0	0	0	0	0	1	0
0	0	0	0	0	0	0

Fig. 11 – Quiescent-device-current test circuit.

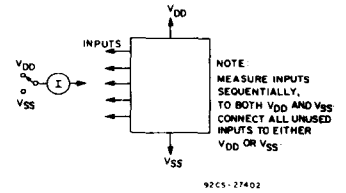


Fig. 12 – Input-leakage-current test circuit.