CMOS 4 x 4 Multiport Register

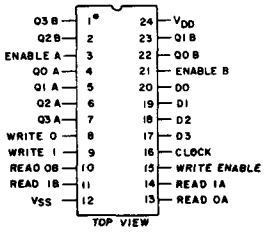
High-Voltage Types (20-Volt Rating)

The RCA-CD40208B is a 4 x 4 multiport register containing four 4-bit registers, write address decoder, two separate read address decoders, and two 3-state output buses.

When the ENABLE input is low, the corresponding output bus is switched, independently of the clock, to a high-impedance state. The high-impedance third state provides the outputs with the capability of being connected to the bus lines in a bus-organized system without the need for interface or pull-up components.

When the WRITE ENABLE input is high, all data input lines are latched on the positive transition of the CLOCK and the data is entered into the word selected by the write address lines. When WRITE ENABLE is low, the CLOCK is inhibited and no new data is entered. In either case, the contents of any word may be accessed via the read address lines independent of the state of the CLOCK input.

The CD40208B types are supplied in hermetic 24-lead dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).



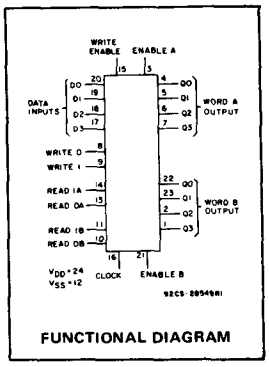
TERMINAL ASSIGNMENT

Features:

- Four 4-bit registers
- One input and two output buses
- Unlimited expansion in bit and word directions
- Data lines have latched inputs
- 3-state outputs
- Separate control of each bus, allowing simultaneous independent reading of any of four registers on Bus A and Bus B and independent writing into any of the four registers
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package-temperature range):
  1 V at V_{DD} = 5 V
  2 V at V_{DD} = 10 V
  2.5 V at V_{DD} = 15 V
- 5-V, 10-V, and 15-V parametric ratings
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Scratch-pad memories
- Arithmetic units
- Data storage



FUNCTIONAL DIAGRAM

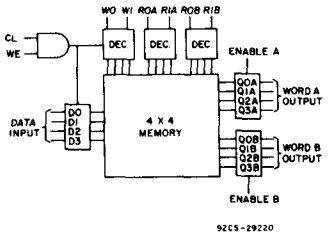


Fig. 1 – Block diagram.

TRUTH TABLE

CLOCK	WRITE ENABLE	WRITE 1	WRITE 0	READ 1A	READ 0A	READ 1B	READ 0B	ENABLE A	ENABLE B	D_n	Q_{nA}	Q_{nB}
⌐¯	1	S1	S2	S1	S2	S1	S2	1	1	1	1	1
⌐¯	1	S1	S2	S1	S2	S1	S2	1	1	0	0	0
X	X	X	X	X	X	X	X	0	0	X	Z	Z
⌐¯	1	0	0	0	1	1	0	1	1	D_n to word 0	Word 1 out	Word 2 out
⌐¯	0	0	0	0	1	1	0	1	1	Word 0 not altered	Word 1 out	Word 2 out
X	X	X	X	1	0	0	1	1	1	X	Word 2 out	Word 1 out
¯⌐	X	X	X	X	X	X	X	1	1	X	NC	NC

1 = HIGH LEVEL; 0 = LOW LEVEL; X = DON'T CARE; Z = HIGH IMPEDANCE
S1 and S2 refer to input states of either 1 or 0

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR:
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

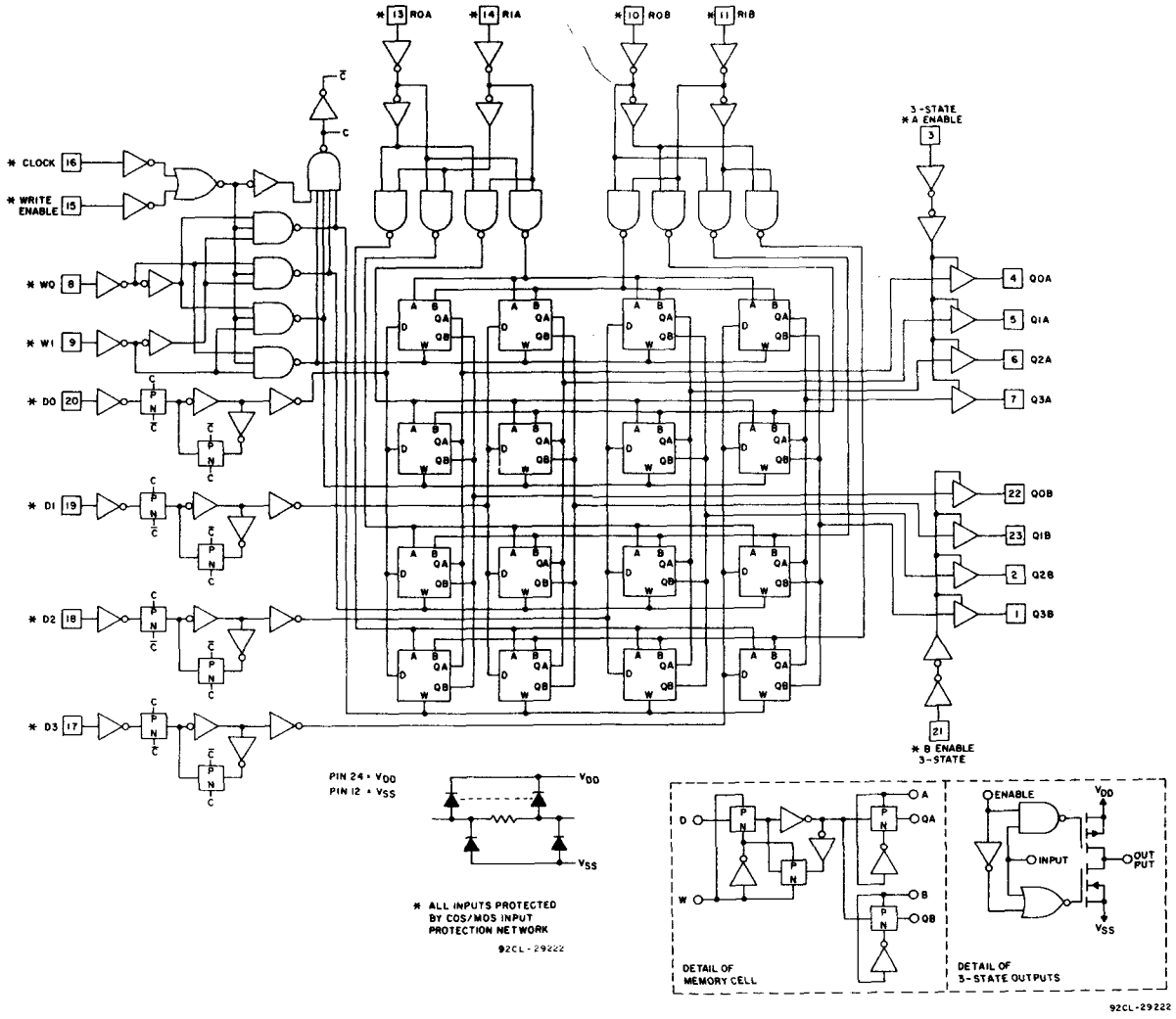


Fig. 2 – Logic diagram.

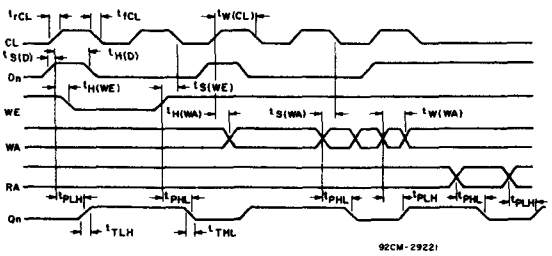


Fig. 3 – Timing diagram.

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS		UNITS
		MIN.	MAX.	
Supply Voltage Range (For T_A = Full Package Temperature Range)	–	3	18	V
Set-Up Time: Data to Clock, $t_{S(D)}$	5	0	–	ns
	10	0	–	
	15	0	–	
Write Enable to $\overline{Clock}$, $t_{S(WE)}$	5	250	–	ns
	10	100	–	
	15	70	–	
Write Address to $\overline{Clock}$, $t_{S(WA)}$	5	250	–	ns
	10	100	–	
	15	70	–	
Hold Time: Data to Clock, $t_{H(D)}$	5	220	–	ns
	10	100	–	
	15	80	–	
Write Enable to Clock, $t_{H(WE)}$	5	270	–	ns
	10	130	–	
	15	80	–	
Write Address to Clock, $t_{H(WA)}$	5	330	–	ns
	10	140	–	
	15	90	–	
Clock Input Frequency, f_{CL}	5	–	1.5	MHz
	10	–	3.5	
	15	–	4.5	
Clock Pulse Width, CL or WE t_W	5	350	–	ns
	10	130	–	
	15	90	–	
Clock Rise or Fall Time, t_rCL or t_fCL	5	–	15	μs
	10	–	5	
	15	–	5	

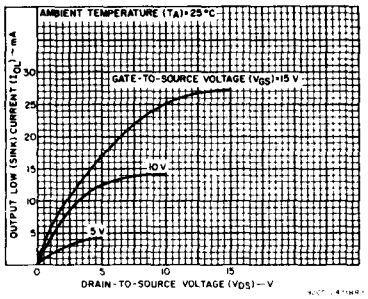


Fig. 4 – Typical output low (sink) current characteristics.

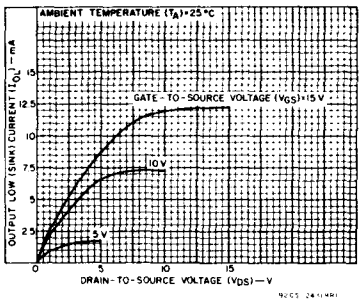


Fig. 5 – Minimum output low (sink) current characteristics.

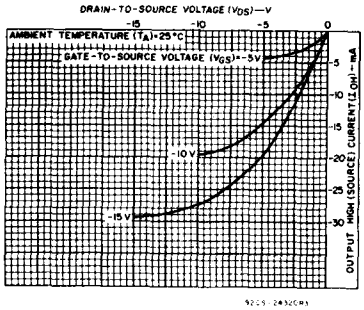


Fig. 6 – Typical output high (source) current characteristics.

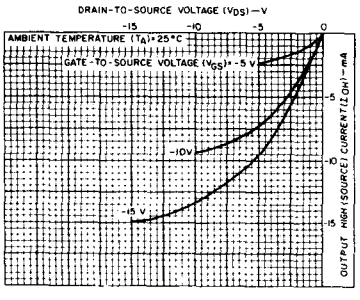


Fig. 7 – Minimum output high (source) current characteristics.

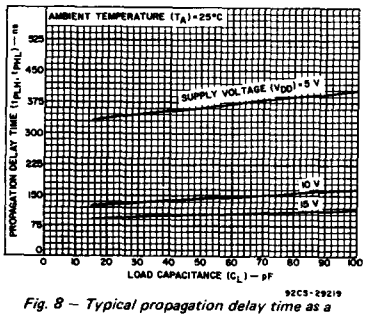


Fig. 8 – Typical propagation delay time as a function of load capacitance (CL or WE to Q).

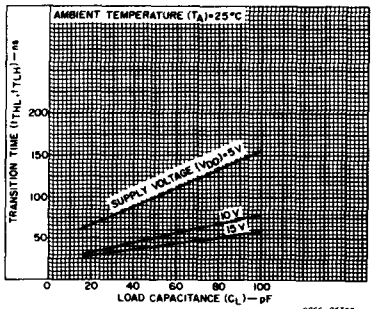
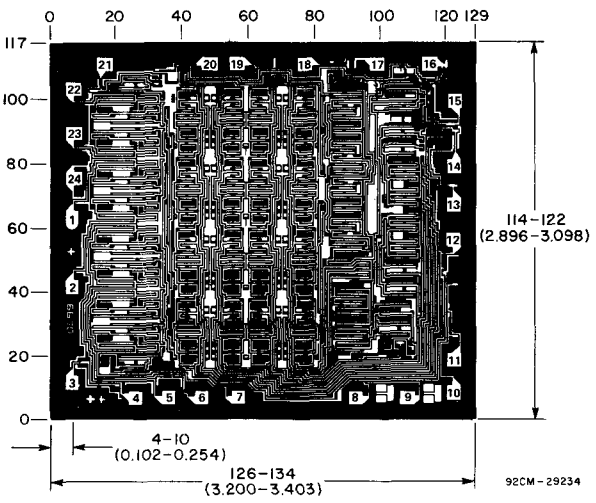


Fig. 9 – Typical transition time as a function of load capacitance.

CD40208B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D,K,F,H Packages Values at −40, +25, +85 Apply to E Package							UNITS
									+25		
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	–	5	1.5				—	—	1.5	V
	1, 9	–	10	3				—	—	3	
	15, 13.5	–	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	–	5	3.5				3.5	—	—	
	1, 9	–	10	7				7	—	—	
	1.5,13.5	–	15	11				11	—	—	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA
3-State Output Leakage Current I_{OUT} Max.	0,18	0,18	18	±0.4	±0.4	±12	±12	–	$\pm 10^{-4}$	±0.4	μA



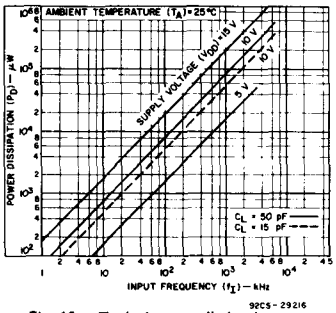


Fig. 10 – Typical power dissipation as a function of input frequency.

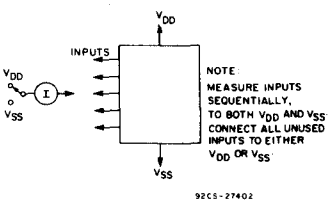


Fig. 11 – Input leakage current test circuit.

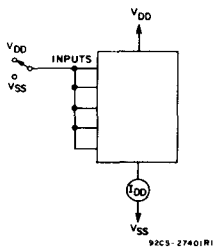


Fig. 12 – Quiescent-device-current test circuit.

Dimensions and Pad Layout for CD40208BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r,t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: t_{PHL}, t_{PLH} Clock or Write Enable to Q	5	–	360	720	ns
	10	–	140	280	
	15	–	100	200	
Read or Write Address to Q	5	–	300	600	ns
	10	–	120	240	
	15	–	85	170	
3-State Disable Delay Time:	5	–	100	200	ns
	10	–	50	100	
t_{PZH}, t_{PHZ}	15	–	40	80	
t_{PZL}, t_{PLZ}	5	–	130	260	ns
	10	–	60	120	
	15	–	50	100	
Output Transition Time: t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Setup Time: Data to Clock $t_{S(D)}$	5	–	−95	0	ns
	10	–	−35	0	
	15	–	−20	0	
Write Enable to $\overline{Clock}$ $t_{S(WE)}$	5	–	125	250	ns
	10	–	50	100	
	15	–	35	70	
Write Address to $\overline{Clock}$ $t_{S(WA)}$	5	–	125	250	ns
	10	–	50	100	
	15	–	35	70	
Clock Rise and Fall Time: t_rCL, t_fCL	5	–	–	15	μs
	10	–	–	5	
	15	–	–	5	
Minimum Hold Time: Data to Clock $t_{H(D)}$	5	–	110	220	ns
	10	–	50	100	
	15	–	40	80	
Write Enable to Clock $t_{H(WE)}$	5	–	135	270	ns
	10	–	65	130	
	15	–	40	80	
Write Address to $\overline{Clock}$ $t_{H(WA)}$	5	–	165	330	ns
	10	–	70	140	
	15	–	45	90	
Maximum Clock Input Frequency, f_{CL}	5	1.5	3	–	MHz
	10	3.5	7	–	
	15	4.5	9	–	
Minimum Clock Pulse Width, Clock or Write Enable $t_{W(CL)}$	5	–	175	350	ns
	10	–	65	130	
	15	–	45	90	
Write Address $t_{W(WA)}$	5	–	150	300	ns
	10	–	75	150	
	15	–	45	90	
Average Input Capacitance, (Any Input) C_I	–	–	5	7.5	pF

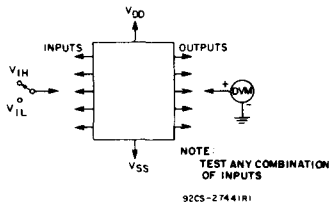
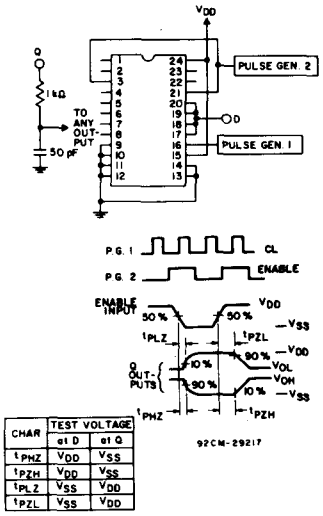


Fig. 13 – Input-voltage test circuit.



CHAR	TEST VOLTAGE at D	at Q
t_{PHZ}	V_{DD}	V_{SS}
t_{PZH}	V_{DD}	V_{SS}
t_{PLZ}	V_{SS}	V_{DD}
t_{PZL}	V_{SS}	V_{DD}

Fig. 14 – Output-enable-delay-times test circuit and waveforms.

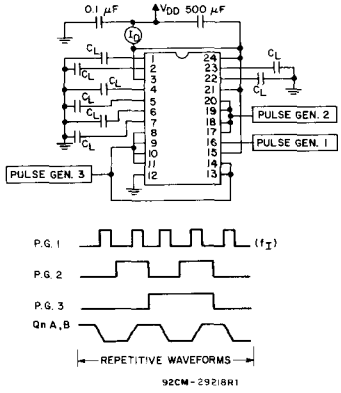


Fig. 15 – Power-dissipation test circuit and waveforms.