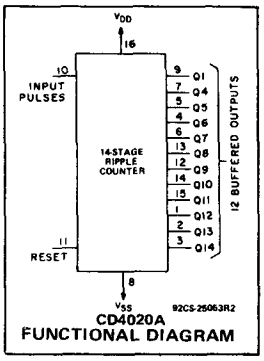
CMOS 14-Stage Ripple-Carry Binary Counter/Divider

The RCA-CD4020 consists of a PULSE INPUT shaping circuit, RESET line driver circuitry, and 14 ripple-carry binary counter stages. Buffered outputs are externally available from stages 1 and 4 through 14. The counter is reset to its all-zeroes state by a high level on the RESET inverter input line. Each counter stage is a static master-slave flip-flop. The counter is advanced one count on the negative-going transition of each INPUT PULSE.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4020A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPE E ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) .... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input Pulse Width, t_W	5	335	–	500	–	ns
	10	125	–	165	–	
Input Pulse Frequency, f_ϕ	5	dc	1.5	dc	1.5	MHz
	10	dc	4	dc	4	
Input Pulse Rise or Fall Time, $t_{r\phi}$, $t_{f\phi}$	5	–	15	–	15	μs
	10	–	15	–	15	
Reset Pulse Width, t_W	5	2500	–	3000	–	ns
	10	475	–	550	–	

Features:

- Medium speed operation . . . 7 MHz (typ.) at V_{DD}−V_{SS} = 10 V
- Low output impedance
- Common reset
- Fully static operation
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Frequency-dividing circuits
- Time-delay circuits
- Counter control
- Counting functions

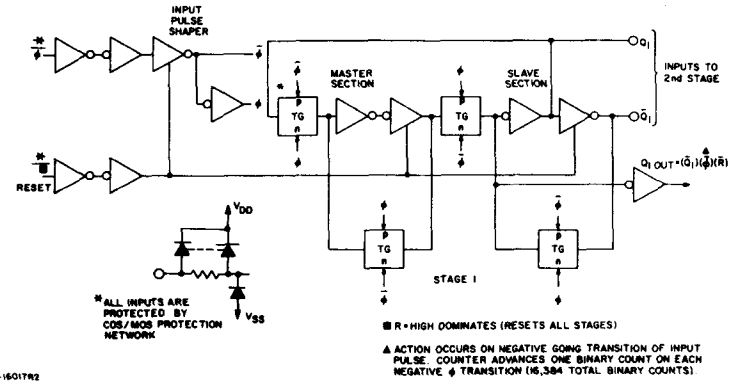


Fig. 1—Logic diagram for 1 of 14 binary stages.

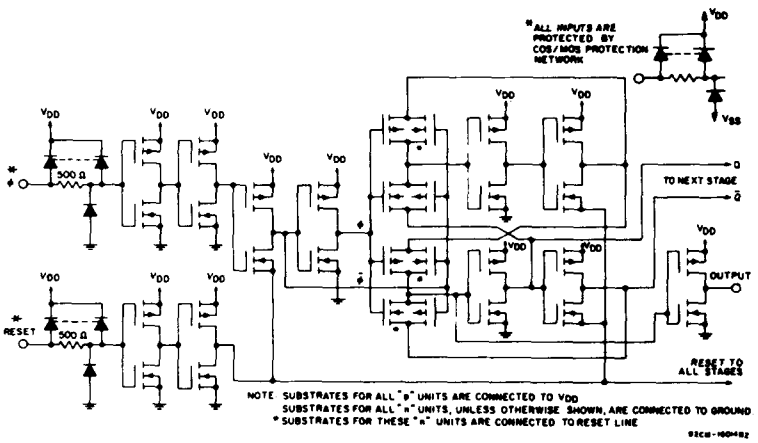


Fig. 2 – Schematic diagram of pulse shapers and 1 of 14 binary stages.

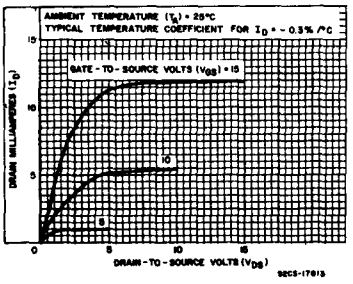


Fig. 3—Typical output n-channel drain characteristics.

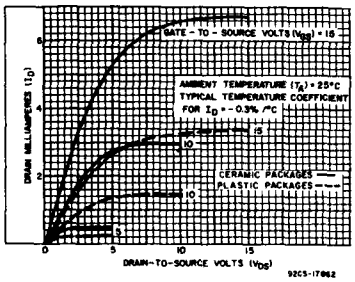


Fig. 4—Minimum output n-channel drain characteristics.

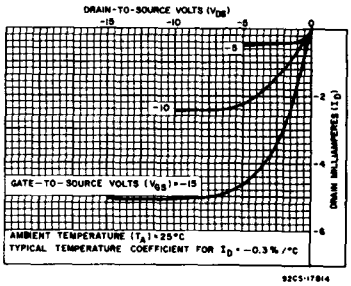


Fig. 5—Typical output p-channel drain characteristics.

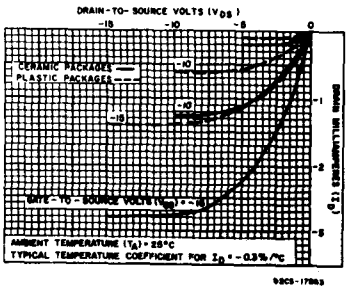


Fig. 6—Minimum output p-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				*E Package*				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.5	–	5	0.09	0.2	0.075	0.05	0.09	0.33	0.08	0.065	mA
	0.5	–	10	0.185	0.4	0.15	0.105	0.16	0.5	0.10	0.10	
P-Channel (Source) I_DP Min.	4.5	–	5	−0.11	−0.25	−0.09	−0.065	−0.09	−0.25	−0.06	−0.05	
	9.5	–	10	−0.25	−0.5	−0.20	−0.14	−0.18	−0.5	−0.15	−0.12	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											μA
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r,t_f = 20 ns, C_L = 15 pF, R_L 200 kΩ

CHARACTERISTIC	TEST CONDITIONS V_{DD} (V)	LIMITS D, F, K, H Packages Min.	Typ.	Max.	LIMITS E Package Min.	Typ.	Max.	UNITS
Clocked Operation								
Propagation Delay Time,* t_{PLH}, t_{PHL}	5	–	450	600	–	450	650	ns
	10	–	150	225	–	150	250	
Transition Time, t_{THL}, t_{TLH}	5	–	450	600	–	450	650	ns
	10	–	200	300	–	200	350	
Maximum Input Pulse Frequency, f_ϕ	5	1.5	2.5	–	1.5	2.5	–	MHz
	10	4	6	–	4	6	–	
Minimum Input Pulse Width, t_W	5	–	200	335	–	200	500	ns
	10	–	70	125	–	70	165	
Input Pulse Rise & Fall Time, $t_{r\phi}$,$t_{f\phi}$	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Average Input Capacitance, C_I	Any Input	–	–	5	–	–	5	pF
Reset Operation								
Propagation Delay Time,* t_{PHL}	5	–	2000	3000	–	2000	3500	ns
	10	–	500	775	–	500	300	
Minimum Reset Pulse Width, t_W	5	–	1800	2500	–	1800	3000	ns
	10	–	300	475	–	300	550	

* Propagation delay is from input pulse to Q_1 output.

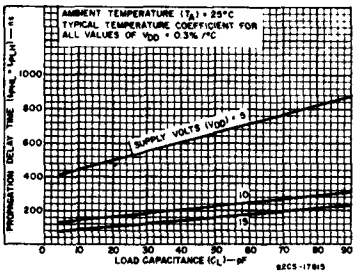


Fig. 7—Typical propagation delay time vs. C_L.

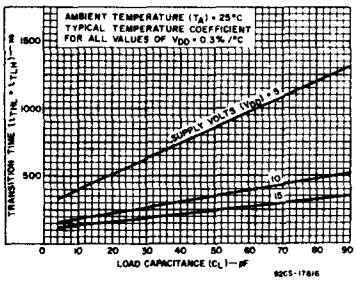


Fig. 8—Typical transition time vs. C_L.

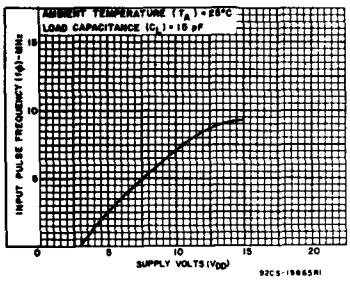


Fig. 9—Typical clock input frequency vs. V_{DD}.

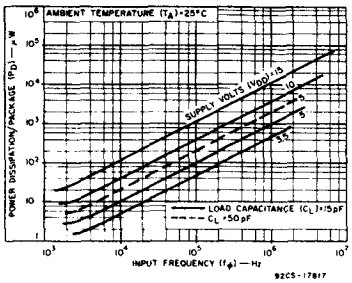


Fig. 10—Typical dissipation characteristics.

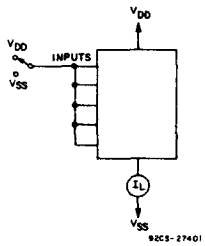


Fig. 11—Quiescent-device-current test circuit.

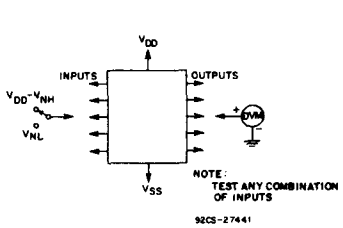


Fig. 12—Noise-immunity test circuit.

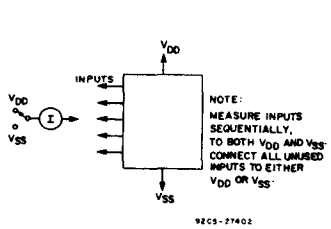


Fig. 13—Input-leakage-current test circuit.