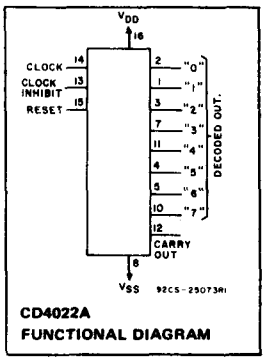
CMOS Divide-By-8 Counter/Divider With 8 Decoded Outputs

The RCA-CD4022A types consist of a 4-stage divide-by-8 Johnson counter, associate decode output gating and a CARRY-OUT BIT. The counter is cleared to its zero count by a high RESET signal. The counter is advanced on the positive CLOCK-signal transition provided the CLOCK INHIBIT signal is low.

Use of the Johnson divide-by-8 counter configuration permits high-speed operation, 2-input decode gating, and spike-free decoder outputs. Anti-lock gating is provided, thus assuring proper counting sequence. The 8 decode gating outputs are normally low and go high only at their respective decoded time slot. Each decode gate output remains high for one full clock cycle. The CARRY-OUT signal completes one cycle every 8 CLOCK-INPUT cycles and is used as a ripple-carry signal to directly clock a succeeding counter package in a multi-package counting system.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4022A
FUNCTIONAL DIAGRAM

Features:

- **Medium speed operation . . . . 5 MHz (typ.) at $V_{DD} - V_{SS} = 10$ V**
- **Divide by N counting; N = 2 to 8 with one CD4022A plus one CD4001A package**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Binary counting/decoding**
- **Binary frequency division**
- **Binary counter control/timers**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
  PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C
  PACKAGE TYPE E . . . . . −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
  (Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
  FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
  FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
  FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
  FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
  At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Clock Inhibit Setup Time, t_S	5 10	175 75	– –	175 75	– –	ns
Clock Pulse Width, t_W	5 10	500 170	– –	830 250	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1 3	dc dc	0.6 2	MHz
Clock Rise and Fall Time, t_rCL, t_fCL	5 10	– –	15 15	– –	15 15	μs
Reset Pulse Width	5 10	300 150	– –	600 300	–	ns
Reset Removal Time	5 10	752 225	– –	1000 275	– –	ns

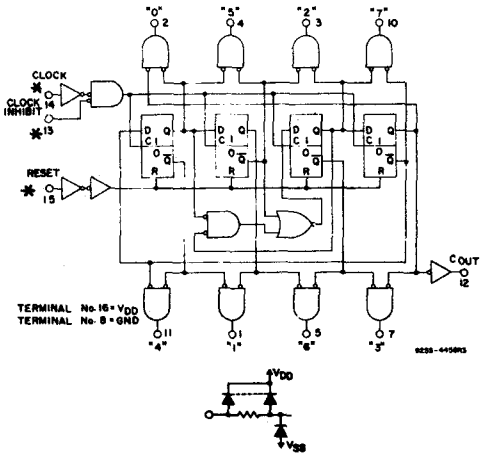


Fig. 1 – Logic diagram.

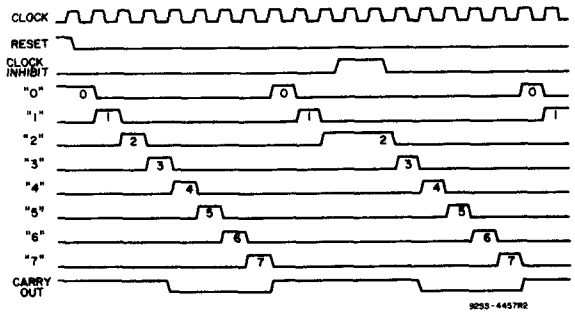


Fig. 2 – Timing diagram.

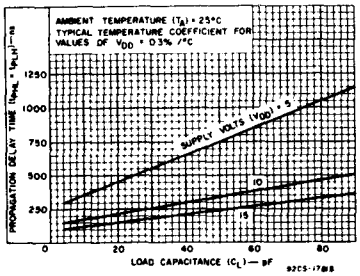


Fig. 3 – Typical propagation delay time vs. load capacitance for decoded outputs.

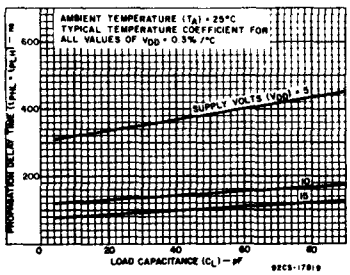


Fig. 4 – Typical propagation delay time vs. load capacitance for carry output.

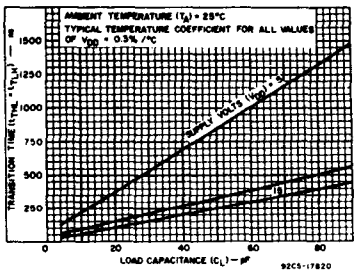


Fig. 5 – Typical transition time vs. load capacitance for decoded outputs.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic		Conditions			Limits at Indicated Temperatures (°C)								Units
					D, F, K, H Packages				E Package				
		V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.		–	–	5	5	0.3	5	300	50	0.5	50	700	μA
		–	–	10	10	0.5	10	600	100	1	100	1400	
		–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level V_{OL}		–	5	5	0 Typ.; 0.05 Max.								V
		–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}		–	0	5	4.95 Min.; 5 Typ.								
		–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.								V
		9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.								
		1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.								V
		9	–	10	1 Min.								
Inputs High, V_{NMH}		0.5	–	5	1 Min.								
		1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_{DN} Min.	Decoded Outputs	0.5	–	5	0.062	0.15	0.05	0.035	0.03	0.15	0.025	0.02	mA
		0.5	–	10	0.12	0.3	0.1	0.07	0.06	0.3	0.05	0.04	
	Carry Output	0.5	–	5	0.185	0.5	0.15	0.105	0.095	0.5	0.08	0.065	
		0.5	–	10	0.375	1	0.3	0.21	0.155	1	0.13	0.105	
p-Channel (Source): I_{DP} Min.	Decoded Outputs	4.5	–	5	-0.038	-0.075	-0.03	-0.021	-0.018	-0.075	-0.015	-0.012	
		9.5	–	10	-0.12	-0.15	-0.1	-0.07	-0.06	-0.15	-0.05	-0.04	
	Carry Output	4.5	–	5	-0.185	-0.4	-0.15	-0.105	-0.095	-0.4	-0.08	-0.065	
		9.5	–	10	-0.375	-0.8	-0.3	-0.21	-0.155	-0.8	-0.13	-0.105	
Input Leakage Current, I_{IL}, I_{IH}		Any Input	–	15	±10⁻⁵ Typ., ±1 Max.								μA

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			D, F, K, H Packages			E Package			
		V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
CLOCKED OPERATION									
Propagation Delay Time: t_{PHL}, t_{PLH} Carry-Out Line		5	–	325	1000	–	325	1300	ns
		10	–	125	250	–	125	500	
Decode Out Lines		5	–	400	1200	–	400	1600	ns
		10	–	200	400	–	200	800	
Transition Time: t_{THL}, t_{TLH} Carry-Out Line		5	–	85	300	–	85	340	ns
		10	–	50	100	–	50	200	
Decode-Out Lines		5	–	300	900	–	300	1200	ns
		10	–	125	250	–	125	500	
Min. Clock Pulse Width, t_W		5	–	250	500	–	250	830	ns
		10	–	86	170	–	85	250	
Clock Rise and Fall Time, t_{rCL}, t_{fCL}		5	–	–	15	–	–	15	μs
		10	–	–	15	–	–	15	
Min. Clock Inhibit Set-Up Time, t_S		5		175	350		175	700	ns
		10		75	150		75	300	
Max. Clock Input Frequency, f_{CL}*		5	1	2.5	–	0.6	2.5	–	MHz
		10	3	5	–	2	5	–	
Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
RESET OPERATION									
Propagation Delay Time: t_{PHL}, t_{PLH} Carry-Out Line		5	–	300	900	–	300	1200	ns
		10	–	125	250	–	125	500	
Decode-Out Line		5	–	500	1250	–	500	2500	ns
		10	–	200	400	–	200	800	
Min. Reset Pulse Width, t_W		5	–	150	300	–	150	600	ns
		10	–	75	150	–	75	300	
Min. Reset Removal Time		5	–	300	752	–	300	1000	ns
		10	–	100	225	–	100	275	

* Measured with respect to carry output line

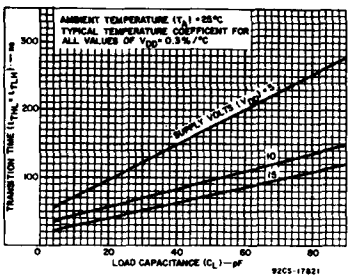


Fig. 6 – Typical transition time vs. load capacitance for carry output.

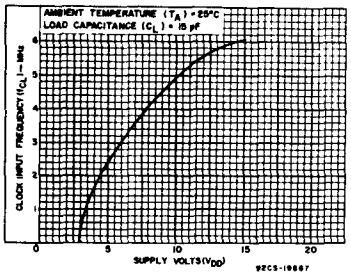


Fig. 7 – Typical clock input frequency vs. supply voltage.

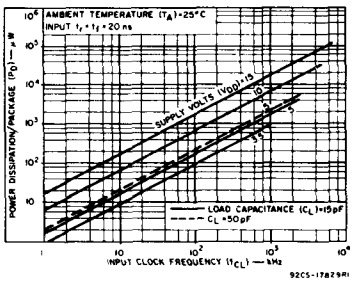


Fig. 8 – Typical dissipation characteristics.

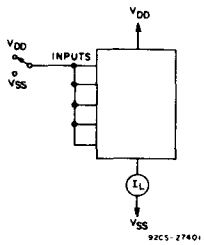


Fig. 9 – Quiescent-device-current test circuit.

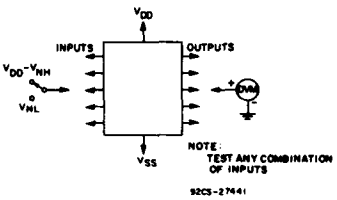


Fig. 10 – Noise-immunity test circuit.

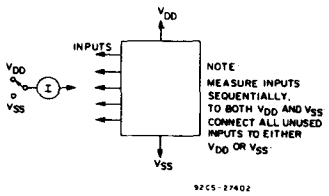


Fig. 11 – Input-leakage-current test circuit.