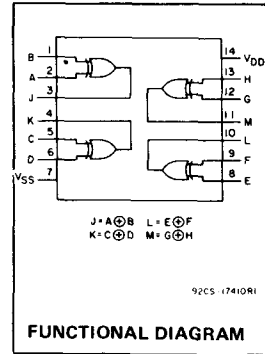


CMOS Quad Exclusive-OR Gate

The RCA-CD4030A types consist of four independent Exclusive-OR gates integrated on a single monolithic silicon chip. Each Exclusive-OR gate consists of four n-channel and four p-channel enhancement-type transistors. All inputs and outputs are protected against electrostatic effects.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).



MAXIMUM RATINGS, Absolute-Maximum Values

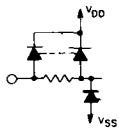
STORAGE TEMPERATURE RANGE (T_{stg})	-65 to +150°C
OPERATING TEMPERATURE RANGE (T_A)	
PACKAGE TYPES D, F, K, H	-55 to +125°C
PACKAGE TYPE E	-40 to +85°C
DC SUPPLY VOLTAGE RANGE (V_{DD})	
(Voltages referenced to V_{SS} Terminal)	-0.5 to +15V
POWER DISSIPATION PER PACKAGE (P_D)	
FOR $T_A = -40$ to +60°C (PACKAGE TYPE E)	500 mW
FOR $T_A = +60$ to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR $T_A = -55$ to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR $T_A = +100$ to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5 to $V_{DD} + 0.5$
LEAD TEMPERATURE (DURING SOLDERING)	
At distance 1/16 ± 1/32 inch (159 ± 0.79 mm) from case for 10s max.	+265°C

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$,

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS				UNITS
	D, F, K, H Packages		E Package		
	Min.	Max.	Min.	Max.	
Supply Voltage Range (For $T_A =$ Full Package Temperature Range)	3	12	3	12	V

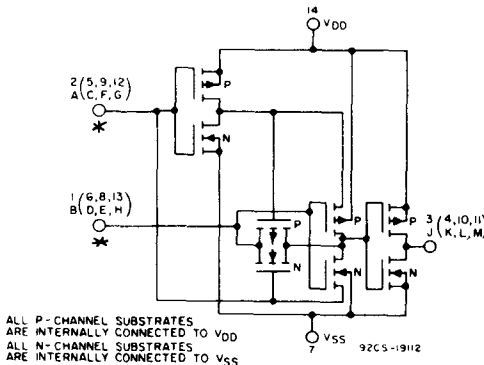
* ALL INPUTS ARE PROTECTED BY COS/MOS PROTECTION NETWORK



TRUTH TABLE FOR ONE OF FOUR IDENTICAL GATES

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

WHERE "1" = HIGH LEVEL
"0" = LOW LEVEL



ALL P-CHANNEL SUBSTRATES ARE INTERNALLY CONNECTED TO V_{DD}
ALL N-CHANNEL SUBSTRATES ARE INTERNALLY CONNECTED TO V_{SS}

Fig. 1 - Schematic diagram for 1 of 4 identical exclusive-OR gates.

For quiescent device current, noise immunity, and input leakage current test circuits see "Rating and Characteristics" at the beginning of the CMOS section.

Features:

- Medium speed operation. $t_{PHL} = t_{PLH} = 40$ ns (typ.) @ $C_L = 15$ pF and $V_{DD} - V_{SS} = 10$ V
- Low output impedance. 500Ω (typ.) @ $V_{DD} - V_{SS} = 10$ V
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (Full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Even and odd-parity generators and checkers
- Logical comparators
- Adders/subtractors
- General logic functions

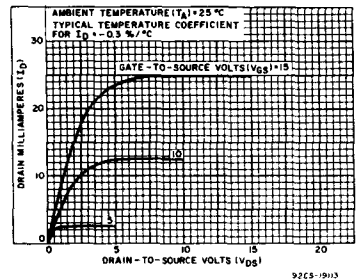


Fig. 2 - Typical output n-channel drain characteristics.

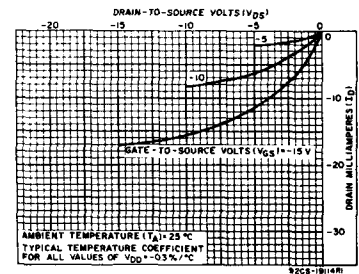


Fig. 3 - Typical output p-channel drain characteristics.

CD4030A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)									Units
				D, F, K, H Packages						E Package			
	V _O (V)	V _{IN} (V)	V _{DD} (V)	-55	+25		+125	-40	+25		+85		
Quiescent Device Current I _L Max.	-	-	5	0.5	0.005	0.5	30	5	0.05	5	70	μA	
	-	-	10	1	0.01	1	60	10	0.1	10	140		
	-	-	15	25	0.5	25	1000	250	2.5	250	2500		
Output Voltage: Low Level, V _{OL}	-	5	5	0 Typ.; 0.05 Max.									V
	-	10	10	0 Typ.; 0.05 Max.									
High Level V _{OH}	-	0	5	4.95 Min.; 5 Typ.									V
	-	0	10	9.95 Min.; 10 Typ.									
Noise Immunity: Inputs Low, V _{NL}	3.6	-	5	1.5 Min.; 2.25 Typ.									V
	7.2	-	10	3 Min.; 4.5 Typ.									
Inputs High V _{NH}	1.4	-	5	1.5 Min.; 2.25 Typ.									V
	2.8	-	10	3 Min.; 4.5 Typ.									
Noise Margin: Inputs Low, V _{NML}	4.5	-	5	1 Min.									V
	9	-	10	1 Min.									
	0.5	-	5	1 Min.									
Inputs High, V _{NMH}	1	-	10	1 Min.									V
Output Drive Current: N Channel (Sink) I _{DN} Min.	0.5	-	5	0.75	1.2	0.6	0.45	0.35	1.2	0.3	0.25	mA	
	0.5	-	10	1.5	2.4	1.2	0.9	0.7	2.4	0.6	0.5		
P Channel (Source): I _{DP} Min.	4.5	-	5	-0.45	-0.6	-0.3	-0.21	-0.21	-0.6	-0.15	-0.12	mA	
	9.5	-	10	-0.95	-1.3	-0.65	-0.45	-0.45	-1.3	-0.32	-0.25		
Input Leakage Current I _{IL} , I _{IH}	Any Input			± 10 ⁻⁵ Typ., ± 1 Max.									μA
	-	-	15										

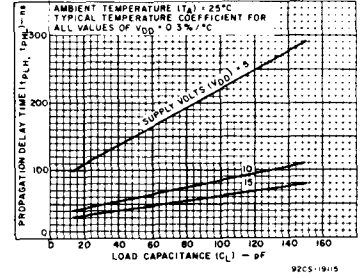


Fig. 4 - Typical propagation-delay time vs. load capacitance.

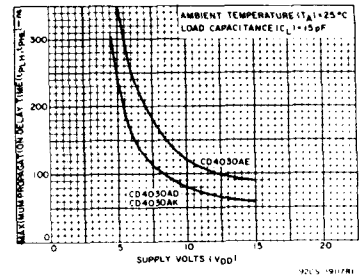


Fig. 5 - Maximum propagation-delay time vs. supply voltage.

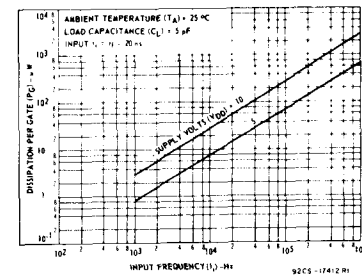


Fig. 6 - Typical dynamic power dissipation characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

Characteristic	Test Conditions	LIMITS						Units	
		V _{DD} (V)	D, F, K, H Packages			E Package			
			Min.	Typ.	Max.	Min.	Typ.		Max.
Propagation Delay Time: t _{PLH} , t _{PHL}		5	-	100	200	-	100	300	ns
		10	-	40	100	-	40	150	
Transition Time: High-to-Low Level, t _T HL		5	-	70	150	-	70	300	ns
		10	-	25	75	-	25	150	
	Low-to-High Level, t _T LH	5	-	80	150	-	80	300	
		10	-	30	75	-	30	150	
Average Input Capacitance, C _i	Any Input	-	5	-	-	5	-	pF	

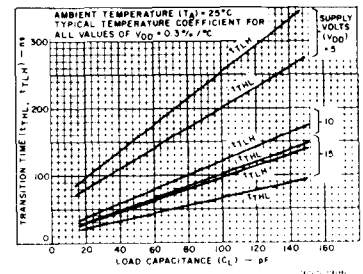


Fig. 7 - Typical transition time vs. load capacitance.