CMOS 8-Stage Static Bidirectional Parallel/Serial Input/Output Bus Register

The RCA-CD4034A is a static eight-stage parallel-or serial-input parallel-output register. It can be used to:

1) bidirectionally transfer parallel information between two buses, 2) convert serial data to parallel form and direct the parallel data to either of two buses, 3) store (recirculate) parallel data, or 4) accept parallel data from either of two buses and convert that data to serial form. Inputs that control the operations include a single-phase CLOCK (CL), A DATA ENABLE (AE), ASYNCHRONOUS/SYNCHRONOUS (A/S), A-BUS-TO-B-BUS/2B-BUS-TO-A-BUS (A/B), and PARALLEL/SERIAL (P/S).

Data inputs include 16 bidirectional parallel data lines of which the eight A data lines are inputs (outputs) and the B data lines are outputs (inputs) depending on the signal level on the A/B input. In addition, an input for SERIAL DATA is also provided.

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave. Isolation from external noise and the effects of loading is provided by output buffering.

PARALLEL OPERATION

A high P/S input signal allows data transfer into the register via the parallel data lines synchronously with the positive transition of the clock provided the A/S input is low. If the A/S input is high the transfer is independent of the clock. The direction of data flow is controlled by the A/B input. When this signal is high the A data lines are inputs (and B data lines are outputs); a low A/B signal reverses the direction of data flow.

The AE input is an additional feature which allows many registers to feed data to a common bus. The A DATA lines are enabled only when this signal is high.

Data storage through recirculation of data in each register stage is accomplished by making the A/B signal high and the AE signal low.

SERIAL OPERATION

A low P/S signal allows serial data to transfer into the register synchronously with the positive transition of the clock. The A/S input is internally disabled when the register is in the serial mode (asynchronous serial operation is not allowed).

The serial data appears as output data on either the B lines (when A/B is high) or the A lines (when A/B is low and the AE signal is high).

Register expansion can be accomplished by simply cascading CD4034A packages.

The CD4034A-Series types are supplied in 24-lead hermetic dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), 24-lead ceramic flat packages (K suffix), and in chip form (H suffix).

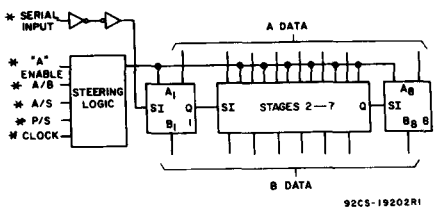
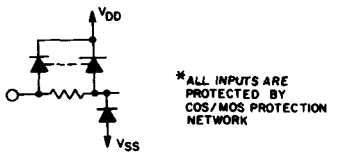


Fig. 1 – Functional diagram.



MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to + 150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . -55 to +125°C

PACKAGE TYPE E. . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) . . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = -40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:*

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5 10	500 200	– –	500 200	– –	ns
Clock Pulse Width, t_W	5 10	400 175	– –	400 175	– –	ns
Clock Input Frequency, f_{CL}	5 10	dc dc	1.5 3	dc dc	1.5 3	MHz
Clock Rise and Fall Time, t_rCL, t_fCL*	5,10	–	15	–	15	μs

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

CD4034A Types

Table I — Truth Table for Register Input-Levels and the Resulting Register Operation (L = Low Level, H = High Level, X = Don't Care)

"A" Enable	P/S	A/B	A/S	Operation*
L	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Outputs Disabled
L	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
L	H	L	L	Parallel Mode; "B" Synch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Inputs, "A" Parallel Data Outputs Disabled
L	H	H	L	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Synch. Data Recirculation
L	H	H	H	Parallel Mode; "A" Parallel Data Inputs Disabled, "B" Parallel Data Outputs, Asynch. Data Recirculation
H	L	L	X	Serial Mode; Synch. Serial Data Input, "A" Parallel Data Output
H	L	H	X	Serial Mode; Synch. Serial Data Input, "B" Parallel Data Output
H	H	L	L	Parallel Mode; "B" Synch. Parallel Data Input, "A" Parallel Data Output
H	H	L	H	Parallel Mode; "B" Asynch. Parallel Data Input, "A" Parallel Data Output
H	H	H	L	Parallel Mode; "A" Synch. Parallel Data Input, "B" Parallel Data Output
H	H	H	H	Parallel Mode; "A" Asynch. Parallel Data Input, "B" Parallel Data Output

*Outputs change at positive transition of clock in the serial mode and when the A/S control input is "low" in the parallel mode.

Features:

- Bidirectional parallel data input
- Parallel or serial inputs/parallel outputs
- Asynchronous or synchronous parallel data loading
- Parallel data-input enable on "A" data lines
- Data recirculation for register expansion
- Multipackage register expansion
- Fully static operation DC-to-5 MHz (typ.) At $V_{DD}-V_{SS}$ = 10 V
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Parallel Input/Parallel Output, Parallel Input/Serial Output, Serial Input/Parallel Output, Serial Input/Serial Output Register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-Down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

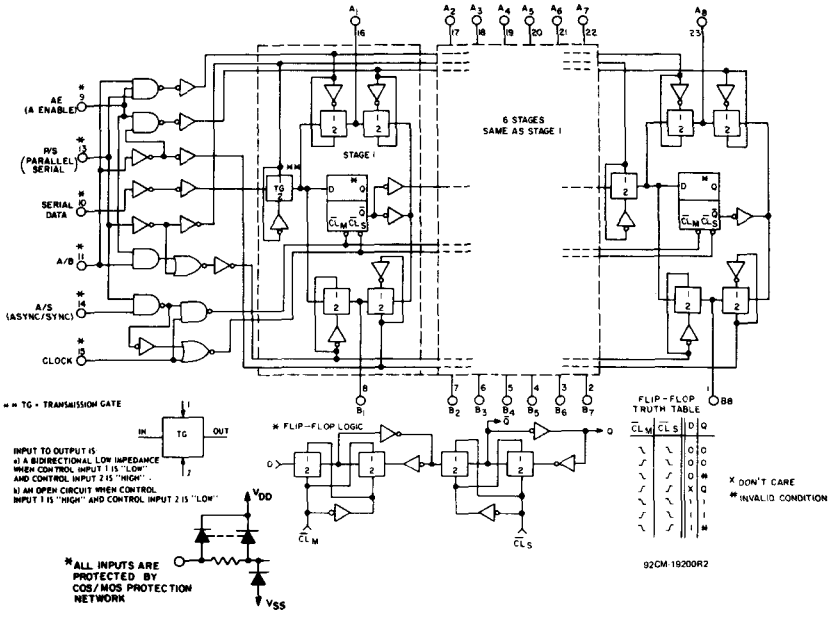


Fig. 2 — Logic diagram.

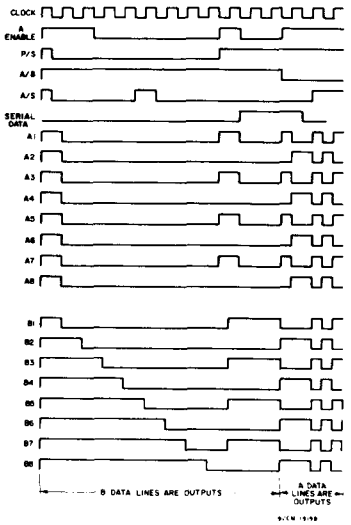


Fig. 3 — Timing diagram.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)								UNITS
				D, F, K, H PACKAGES				E PACKAGE				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	+25 TYP.	+25 LIMIT	+125	-40	+25 TYP.	+25 LIMIT	+85	
Quiescent Device Current, I_L Max.	–	–	5	5	0.3	5	300	50	0.5	50	700	μA
	–	–	10	10	0.5	10	600	100	1	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max								V
	–	10	10	0 Typ.; 0.05 Max								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink),	0.5	–	5	0.124	0.2	0.1	0.07	0.124	0.2	0.1	0.07	mA
I_DN Min.	0.5	–	10	0.31	0.5	0.25	0.175	0.31	0.5	0.25	0.175	
P-Channel (Source):	4.5	–	5	-0.075	-0.1	-0.05	-0.035	-0.075	-0.1	-0.05	-0.035	
I_DP Min.	9.5	–	10	-0.188	-0.25	-0.125	-0.088	-0.188	-0.25	-0.125	-0.088	
Input Leakage Current, I_{IL}, I_{IH}	Any Input	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

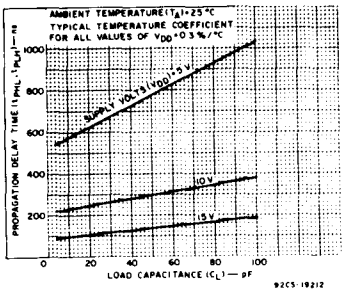


Fig. 4 – Typical propagation delay time vs. load capacitance.

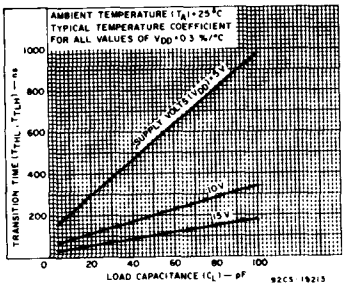


Fig. 5 – Typical transition time vs. load capacitance.

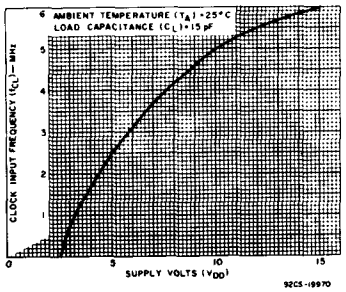


Fig. 6 – Typical clock input frequency vs. supply voltage.

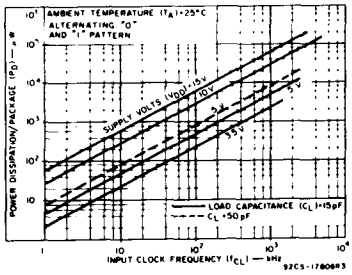


Fig. 7 – Typical dissipation characteristics.

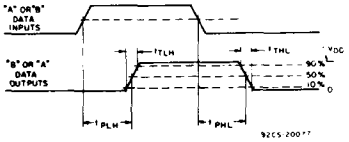


Fig. 8 – Asynchronous operation propagation delay time and transition time.

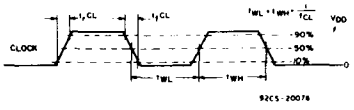


Fig. 9 – Clock pulse rise and fall times.

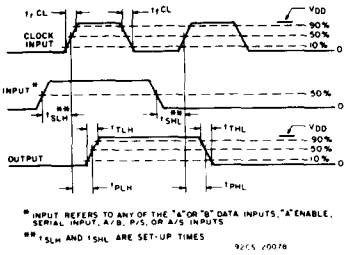


Fig. 10 – Synchronous operation propagation delay times, transition times, and set-up times.

CD4034A Types

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20ns, C_L = 15 pF, RL = 200kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNIT
		D, F, K, H PACKAGES			E PACKAGE			
	V_{DD} (V)	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time; t_{PLH}, t_{PHL}	5	–	600	1200	–	600	1200	ns
	10	–	240	480	–	240	480	
Transition Time; t_{THL}, t_{TLH}	5	–	250	750	–	250	750	ns
	10	–	100	300	–	100	300	
Maximum Clock Input Frequency, f_{CL}	5	1.5	2.5	–	1.5	2.5	–	MHz
	10	3	5	–	3	5	–	
Clock Pulse Width, t_W	5	–	200	400	–	200	400	ns
	10	–	100	175	–	100	175	
Min. High-Level AE, P/S, A/S Pulse Width	5	–	240	480	–	240	480	ns
	10	–	85	195	–	85	195	
Clock Rise & Fall Time t_rCL, t_fCL*	5	–	–	15	–	–	15	μs
	10	–	–	15	–	–	15	
Data Set-Up Time, t_S	5	–	250	500	–	250	500	ns
	10	–	100	200	–	100	200	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

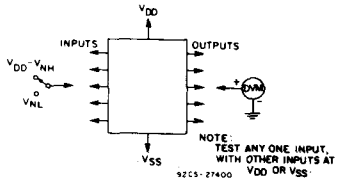


Fig. 11 – Noise-immunity test circuit.

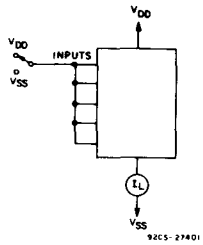


Fig. 12 – Quiescent-device-current test circuit.

APPLICATIONS

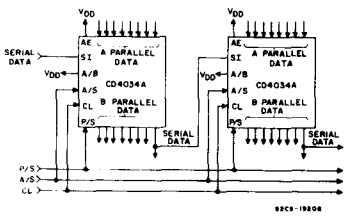


Fig. 14 – 16-Bit parallel in/parallel out, parallel in/serial out, serial in/parallel out, serial in/serial out register.

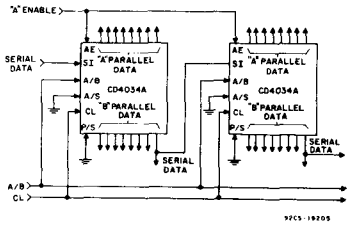


Fig. 15 – 16-Bit serial in/gated parallel out register.

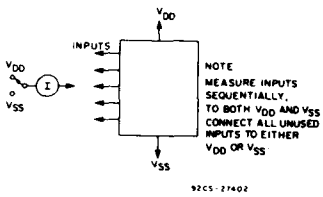


Fig. 13 – Input-leakage-current test circuit.