CD4035B Types

CMOS 4-Stage Parallel In/Parallel Out Shift Register

with J-$\overline{K}$ Serial Inputs and True/Complement Outputs

High-Voltage Types (20-Volt Rating)

The RCA-CD4035B is a four-stage clocked signal serial register with provision for synchronous PARALLEL inputs to each stage and SERIAL inputs to the first stage via J$\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial D flip-flop configuration when the register is in the serial mode (PARALLEL/SERIAL control low).

Parallel entry into each register stage is permitted when the PARALLEL/SERIAL control is high.

In the parallel or serial mode information is transferred on positive clock transitions.

When the TRUE/COMPLEMENT control is high, the true contents of the register are available at the output terminals. When the TRUE/COMPLEMENT control is low, the outputs are the complements of the data in the register. The TRUE/COMPLEMENT control functions asynchronously with respect to the CLOCK signal.

J$\overline{K}$ input logic is provided on the first stage SERIAL input to minimize logic requirements particularly in counting and sequence-generation applications. With J$\overline{K}$ inputs connected together, the first stage becomes a D flip-flop. An asynchronous common RESET is also provided.

The CD4035B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

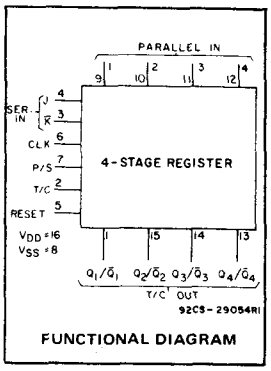
- **4-Stage clocked shift operation**
- **Synchronous parallel entry on all 4 stages**
- **J$\overline{K}$ inputs on first stage**
- **Asynchronous True/Complement control on all outputs**
- **Static flip-flop operation; Master-slave configuration**
- **Buffered inputs and outputs**
- **High speed – 12 MHz (typ.) at V_{DD} = 10 V**
- **100% tested for quiescent current at 20 V**
- **Standardized, symmetrical output characteristics**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of "B" Series CMOS Devices"**

Applications:

- **Counters, Registers**
  Arithmetic-unit registers
  Shift-left – shift right registers
  Serial-to-parallel/parallel-to-serial conversions
- **Sequence generation**
- **Control circuits**
- **Code conversion**

FIRST STAGE TRUTH TABLE

	t_{n-1} (INPUTS)				t_n (OUTPUTS)
CL	J	$\overline{K}$	R	Q_{n-1}	Q_n
↑	0	X	0	0	0
↑	1	X	0	0	1
↑	X	0	0	1	0
↑	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
↑	X	1	0	1	1
↓	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0



FUNCTIONAL DIAGRAM

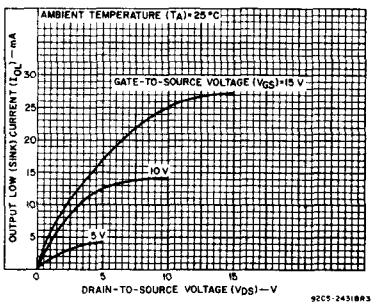


Fig. 1 – Typical output low (sink) current characteristics.

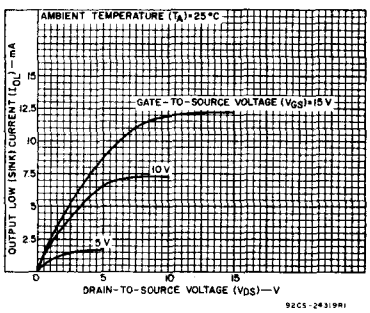


Fig. 2 – Minimum output low (sink) current characteristics.

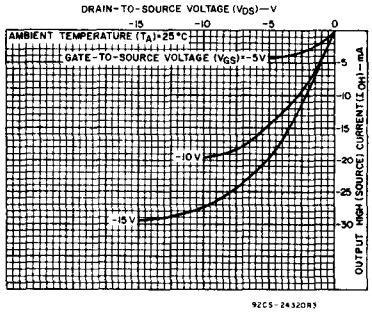


Fig. 3 – Typical output high (source) current characteristics.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

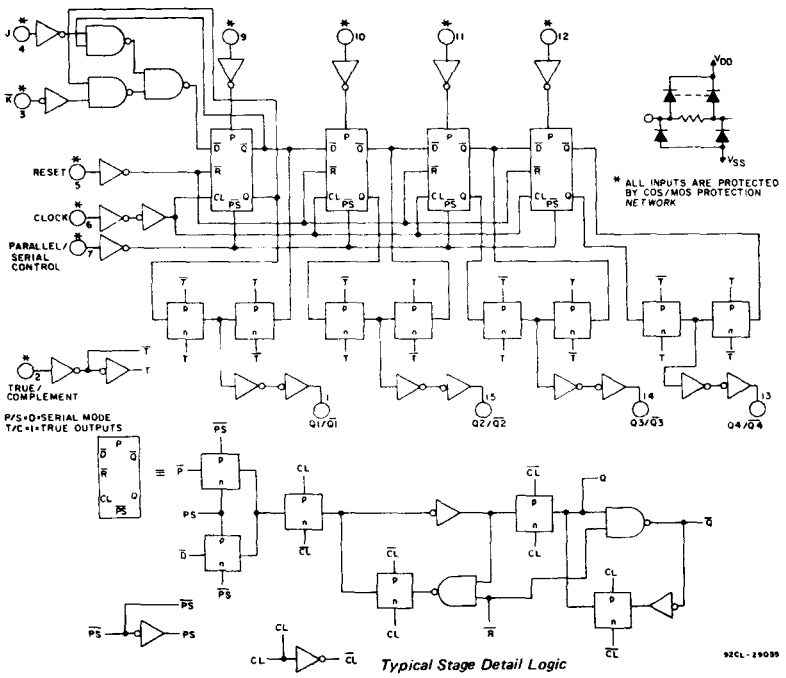


Fig. 4 – Logic diagram.

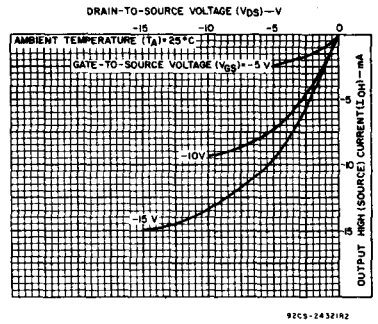


Fig. 5 – Minimum output high (source) current characteristics.

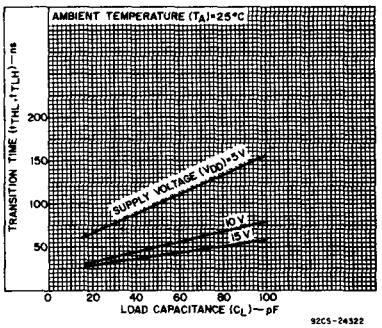


Fig. 6 – Typical transition time as a function of load capacitance.

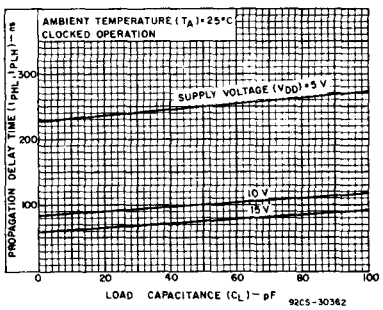


Fig. 7 – Typical propagation delay times as a function of load capacitance (Q output).

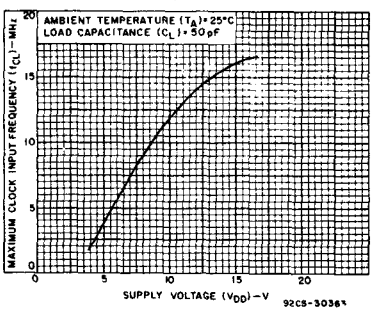


Fig. 8 – Typical maximum clock input frequency as a function of supply voltage.

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	18	V
Data Setup Time, t_S: J/$\overline{K}$ Lines	5	220	–	ns
	10	80	–	
	15	60	–	
Parallel-In Lines	5	140	–	ns
	10	50	–	
	15	40	–	
Clock Pulse Width, t_W	5	200	–	ns
	10	90	–	
	15	60	–	
Clock Input Frequency, f_{CL}	5	dc	2	MHz
	10		6	
	15		8	
Clock Rise or Fall Time, t_rCL, t_fCL:	5	–	15	μs
	10	–	15	
	15	–	15	
Reset Pulse Width, t_W	5	250	–	ns
	10	110	–	
	15	80	–	

CD4035B Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, K, H, Packages Values at −40, +25, +85 Apply to E Package							UNITS
								+25			
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	Min.	Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	–	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	–	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−0.64	−0.61	−0.42	−0.36	−0.51	−1	–	
	2.5	0,5	5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	9.5	0,10	10	−1.6	−1.5	−1.1	−0.9	−1.3	−2.6	–	
	13.5	0,15	15	−4.2	−4	−2.8	−2.4	−3.4	−6.8	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	0	0.05	V
	–	0,10	10	0.05				–	0	0.05	
	–	0,15	15	0.05				–	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5		5	1.5				–	–	1.5	V
	1,9		10	3				–	–	3	
	1.5,13.5		15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5		5	3.5				3.5	–	–	
	1,9		10	7				7	–	–	
	1.5,13.5		15	11				11	–	–	
Input Current I_{IN} Max.		0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

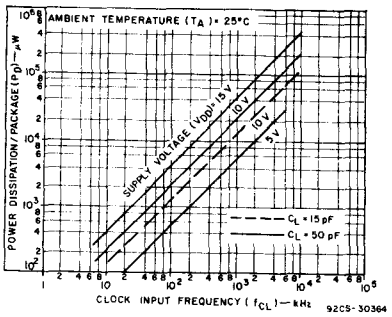


Fig. 9 – Typical dynamic power dissipation as a function of clock input frequency.

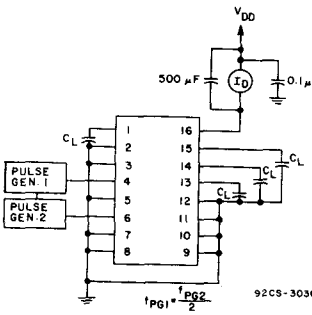


Fig. 10 – Dynamic power dissipation test circuit.

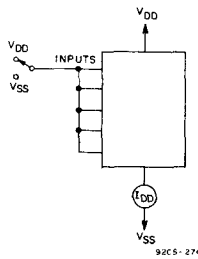


Fig. 11 – Quiescent-device current test circuit.

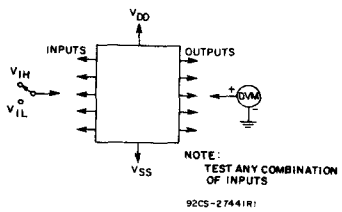


Fig. 12 – Input-voltage test circuit.

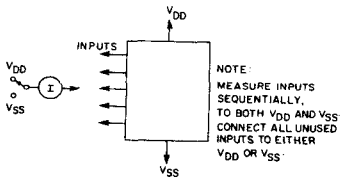


Fig. 13 – Input-current test circuit.

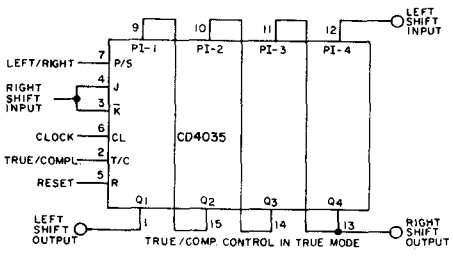
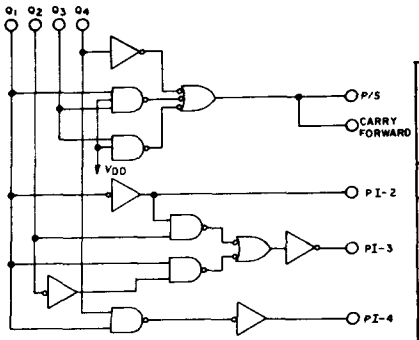


Fig. 14 – Shift left/shift right register.



Using Couleur's Technique (BIDEC)▲, a binary number (most significant bit, MSB) first is shifted and processed, such that the BCD equivalent is obtained when the last binary bit is clocked into the register. The CD4035B, with the correct conversion logic, can also be used as a BCD-to-binary converter.

▲*The basic rule is: If a 4 or less is in a decade, shift with the next clock pulse; if a 5 or greater is in a decade, add 3 and then shift at the next clock pulse. For more information refer to "IRE TRANSACTIONS ON ELECTRONIC COMPUTERS", Dec. 1958, Pages 313–316.*

Fig. 15 – BIDEC logic.

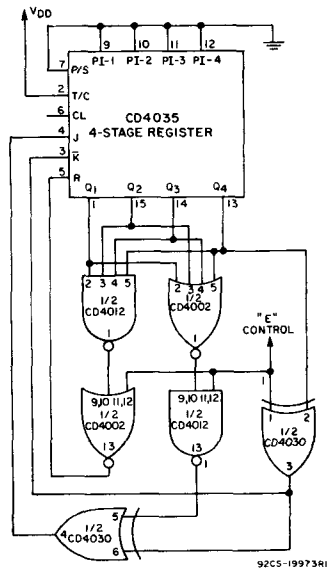


Fig. 16(a) – Double sequence generator.

DYNAMIC ELECTRICAL CHARACTERISTICS

At T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTICS	TEST CONDITIONS V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
CLOCKED OPERATION					
Propagation Delay Time: t_{PHL}, t_{PLH}	5	–	250	500	ns
	10	–	100	200	
	15	–	75	150	
Transition Time: t_{THL}, t_{TLH}	5	–	100	200	ns
	10	–	50	100	
	15	–	40	80	
Minimum Clock Pulse Width, t_W	5	–	100	200	ns
	10	–	45	90	
	15	–	30	60	
Clock Rise or Fall Time, t_rCL, t_fCL*	5,10, 15	–	–	15	μs
Minimum Setup Time: J/$\overline{K}$ Lines	5	–	110	220	ns
	10	–	40	80	
	15	–	30	60	
Parallel-In-Lines	5	–	70	140	ns
	10	–	25	50	
	15	–	20	40	
Maximum Clock Frequency, f_{CL}	5	2	4	–	MHz
	10	6	12	–	
	15	8	16	–	
Input Capacitance, C_{IN}	Any Input	–	5	7.5	pF
RESET OPERATION					
Propagation Delay Time: t_{PHL}, t_{PLH}	5	–	230	460	ns
	10	–	100	200	
	15	–	80	160	
Minimum Reset Pulse Width, t_W	5	–	125	250	ns
	10	–	55	110	
	15	–	40	40	

*If more than one unit is cascaded t_rCL should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Control = E =	0				1			
	Q_1	Q_2	Q_3	Q_4	Q_1	Q_2	Q_3	Q_4
	A	B	C	D	A	B	C	D
0	0	0	0	0	15	1	1	1
1	1	0	0	0	14	0	1	1
2	0	1	0	0	13	1	0	1
5	1	0	1	0	10	0	1	0
10	0	1	0	1	5	1	0	1
4	0	0	1	0	11	1	1	0
9	1	0	0	1	6	0	1	1
3	1	1	0	0	12	0	0	1
6	0	1	1	0	9	1	0	0
13	1	0	1	1	2	0	1	0
11	1	1	0	1	4	0	0	1
7	1	1	1	0	8	0	0	0
14	0	1	1	1	1	1	0	0
12	0	0	1	1	3	1	1	0
8	0	0	0	1	7	1	1	1

Using a control line (E) two different state sequences can be generated. For example, suppose the following two sequences are desired on command (control line E)

Fig. 16(b) – State sequences.

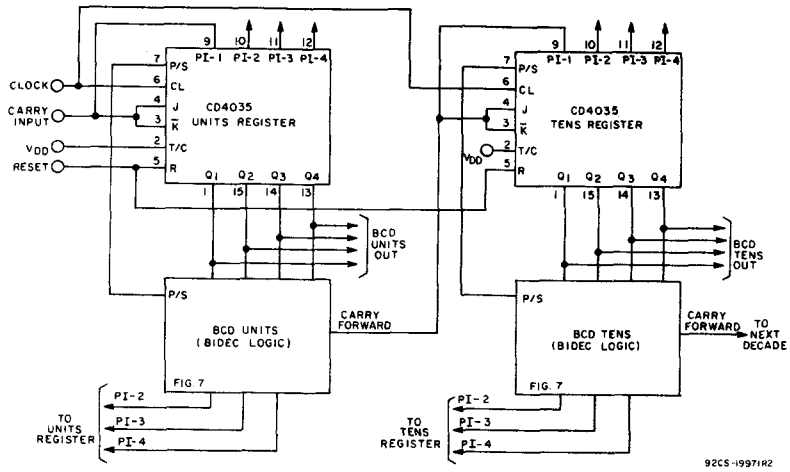
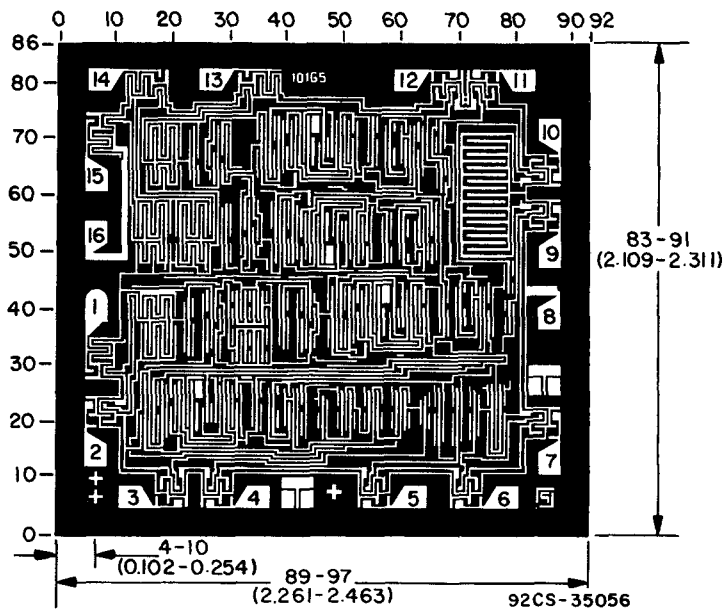


Fig. 17 – Binary-to-BCD converter.



Dimensions and pad layout for CD4035BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

TERMINAL DIAGRAM
Top View