

CD4042B Types

CMOS

Quad Clocked "D" Latch

High-Voltage Types (20-Volt Rating)

The RCA-CD4042B types contain four latch circuits, each strobed by a common clock. Complementary buffered outputs are available from each circuit. The impedance of the n- and p-channel output devices is balanced and all outputs are electrically identical. Information present at the data input is transferred to outputs Q and \bar{Q} during the CLOCK level which is programmed by the POLARITY input. For POLARITY = 0 the transfer occurs during the 0 CLOCK level and for POLARITY = 1 the transfer occurs during the 1 CLOCK level. The outputs follow the data input providing the CLOCK and POLARITY levels defined above are present. When a CLOCK transition occurs (positive for POLARITY = 0 and negative for POLARITY = 1) the information present at the input during the CLOCK transition is retained at the outputs until an opposite CLOCK transition occurs.

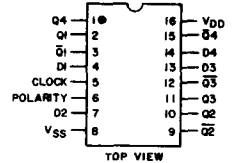
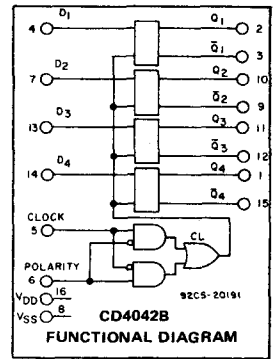
The GD4042B types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Clock polarity control
- Q and \bar{Q} outputs
- Common clock
- Low power TTL compatible
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μ A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin (over full package temperature range):
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- Meets all requirements of JEDEC Tentative Standard No. 13A, "Standard Specifications for Description of 'B' Series CMOS Devices"

Applications:

- Buffer storage
- Holding register
- General digital logic



TERMINAL ASSIGNMENT

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	Values at -55, +25, +125 Apply to D, F, K, H Pkgs.				Values at -40, +25, +85 Apply to E Pkgs.			
				-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current I_{DD} Max.	—	0.5	5	1	1	30	30	—	0.02	1	μ A
	—	0.10	10	2	2	60	60	—	0.02	2	
	—	0.15	15	4	4	120	120	—	0.02	4	
Output Low (Sink) Current I_{OL} Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current I_{OH} Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0.5	5	0.05				—	0	0.05	V
	—	0.10	10	0.05				—	0	0.05	
	—	0.15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0.5	5	4.95				4.95	5	—	V
	—	0.10	10	9.95				9.95	10	—	
	—	0.15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5, 4.5	—	5	1.5				—	—	1.5	V
	1.9	—	10	3				—	—	3	
	1.5, 13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5, 4.5	—	5	3.5				3.5	—	—	V
	1.9	—	10	7				7	—	—	
	1.5, 13.5	—	15	11				11	—	—	
Input Current, I_{IN} Max.	—	0.18	18	± 0.1	± 0.1	± 1	± 1	—	$\pm 10^{-5}$	± 0.1	μ A

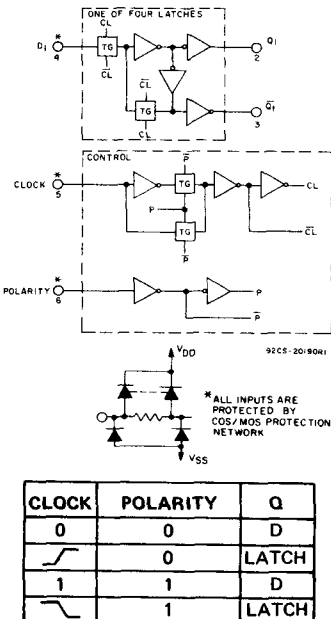


Fig. 1 — Logic block diagram and truth table.

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MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})	(Voltages referenced to V_{SS} Terminal)	-0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS		-0.5 to $V_{DD} + 0.5$ V
DC INPUT CURRENT, ANY ONE INPUT		± 10 mA
POWER DISSIPATION PER PACKAGE (P_D):		
For $T_A = -40$ to $+60^\circ\text{C}$ (PACKAGE TYPE E)		500 mW
For $T_A = +60$ to $+85^\circ\text{C}$ (PACKAGE TYPE E)	Derate Linearly at $12\text{ mW}/^\circ\text{C}$	to 200 mW
For $T_A = -55$ to $+100^\circ\text{C}$ (PACKAGE TYPES D, F, K)		500 mW
For $T_A = +100$ to $+125^\circ\text{C}$ (PACKAGE TYPES D, F, K)	Derate Linearly at $12\text{ mW}/^\circ\text{C}$	to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
For $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE}$ (All Package Types)		100 mW
OPERATING-TEMPERATURE RANGE (T_A):		
PACKAGE TYPES D, F, K, H		-55 to $+125^\circ\text{C}$
PACKAGE TYPE E		-40 to $+85^\circ\text{C}$
STORAGE TEMPERATURE RANGE (T_{stg})		-65 to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ inch (1.59 ± 0.79 mm) from case for 10 s max.		$+265^\circ\text{C}$

RECOMMENDED OPERATING CONDITIONS at $T_A = 25^\circ\text{C}$, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS ALL TYPES		UNITS
		Min.	Max.	
Supply-Voltage Range (For $T_A = \text{Full Package Temperature Range}$)	—	3	18	V
Clock Pulse Width, t_{W}	5	200	—	ns
	10	100	—	
	15	60	—	
Setup Time, t_s	5	50	—	ns
	10	30	—	
	15	25	—	
Hold Time, t_H	5	120	—	ns
	10	60	—	
	15	50	—	
Clock Rise or Fall Time: t_r, t_f	5, 10	Not rise or fall time sensitive.		μs
	15			

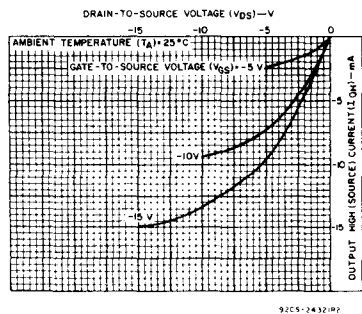


Fig. 5 - Minimum output high (source) current characteristics.

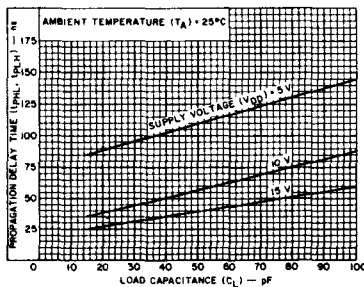


Fig. 6 - Typical propagation delay time vs. load capacitance—data to Q .

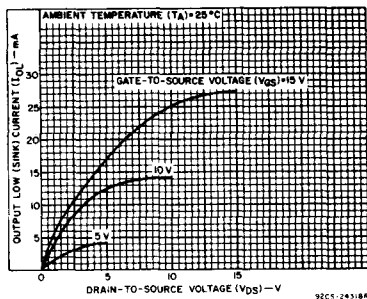


Fig. 2 - Typical output low (sink) current characteristics.

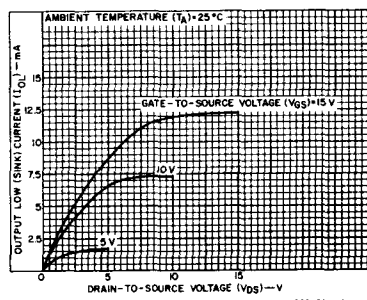


Fig. 3 - Minimum output low (sink) current characteristics.

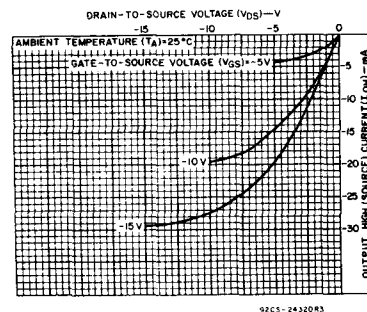


Fig. 4 - Typical output high (source) current characteristics.

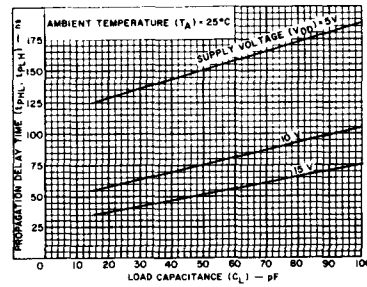


Fig. 7 - Typical propagation delay time vs. load capacitance—data to \bar{Q} .

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DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$; Input $t_r, t_f = 20\text{ ns}$, $C_L = 50\text{ pF}$,
 $R_L = 200\text{ k}\Omega$

CHARACTERISTIC	VDD (V)	LIMITS ALL TYPES		UNITS
		Typ.	Max.	
Propagation Delay Time: t_{PHL}, t_{PLH} Data In to Q	5	110	220	ns
	10	55	110	
	15	40	80	
Data In to \bar{Q}	5	150	300	ns
	10	75	150	
	15	50	100	
Clock to Q	5	225	450	ns
	10	100	200	
	15	80	160	
Clock to \bar{Q}	5	250	500	ns
	10	115	230	
	15	90	180	
Transition Time: t_{THL}, t_{TLH}	5	100	200	ns
	10	50	100	
	15	40	80	
Minimum Clock Pulse Width, t_W	5	100	200	ns
	10	50	100	
	15	30	60	
Minimum Hold Time, t_H	5	60	120	ns
	10	30	60	
	15	25	50	
Minimum Setup Time, t_S	5	0	50	ns
	10	0	30	
	15	0	25	
Clock Input Rise or Fall Time: t_r, t_f	5, 10, 15	Not rise or fall time sensitive.		μs
Input Capacitance, C_{IN} (Any Input)	—	5	7.5	pF

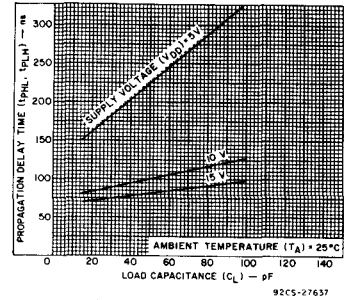


Fig. 8 - Typical propagation delay time vs. load capacitance—clock to Q

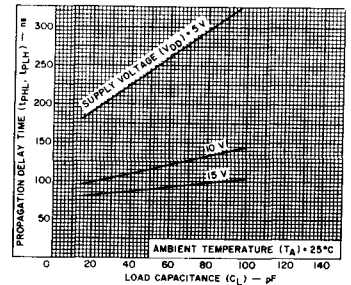


Fig. 9 - Typical propagation delay time vs. load capacitance—clock to \bar{Q} .

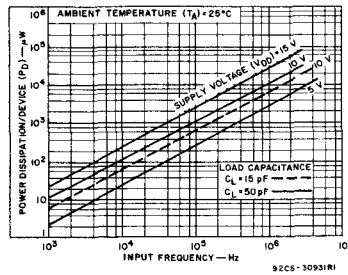


Fig. 10 - Typical power dissipation vs. frequency.

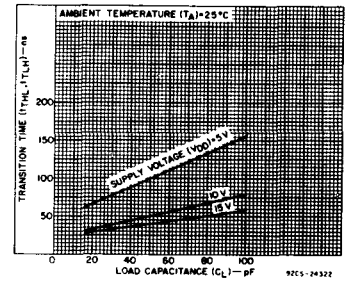
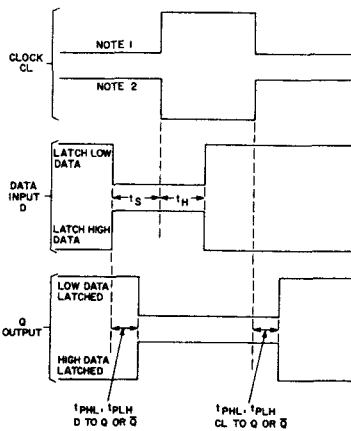


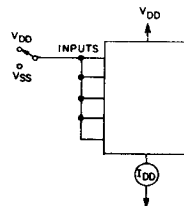
Fig. 11 - Typical transition time vs. load capacitance.



NOTES:
 1. FOR POSITIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS LOW.
 2. FOR NEGATIVE CLOCK EDGE, INPUT DATA IS LATCHED WHEN POLARITY IS HIGH.

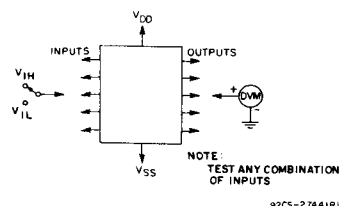
92CS-27630

Fig. 12 - Dynamic test parameters.



92CS-27401R1

Fig. 13 - Quiescent device current test circuit.



92CS-27441R1

Fig. 14 - Input voltage test circuit.

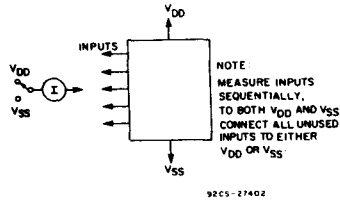
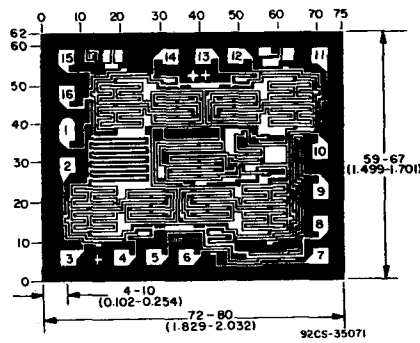


Fig. 15 - Input current test circuit.

Chip Photograph, Dimensions, and Pad Layout



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to $+16$ mils applicable to the nominal dimensions shown.