CMOS 21-Stage Counter

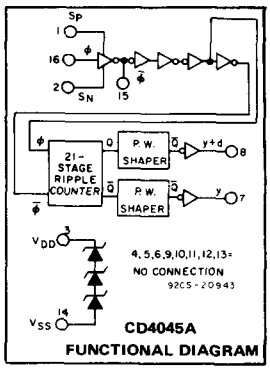
The RCA-CD4045A is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, three 5.5-V zener diodes (providing transient protection at 16.5 V), and input inverters for use in a crystal oscillator. The CD4045A configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers.

The first inverter is intended for use as a crystal oscillator/amplifier. However, it may be used as a normal logic inverter if desired. A crystal oscillator circuit can be made less sensitive to voltage-supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_p to V_{DD}, S_n to V_{SS}). See Fig. 3.

These types are supplied in 16-lead hermetic *dual-in-line ceramic packages (D and F* suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- **Digital equipment in which ultra-low dissipation and/or operation using a battery source are primary design requirements.**
- **Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.**
- **Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.**



FUNCTIONAL DIAGRAM

Features:

- **Microwatt quiescent dissipation . . . . . 2.5 μW (typ.) @ V_{DD} = 5 V; 10 μW (typ.) @ V_{DD} = 10 V**
- **Very low operating dissipation . . . . . 1 mW (typ.); @ V_{DD} = 5 V, $f\phi$ = 1 MHz**
- **Output drivers with sink or source capability . . . . . 7 mA (typ.) @ V_O = 0.5 V, V_{DD} = 5 V (sink) 5 mA (typ.) @ V_O = 4.5 V, V_{DD} = 5 V (source)**
- **Medium speed (typ.) . . . . . $f\phi$ = 5 MHz @ V_{DD} = 5 V $f\phi$ = 10 MHz @ V_{DD} = 10 V**
- **16.5 V zener diode transient protection on chip for automotive use**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C

PACKAGE TYPE E . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		3	12	3	12	V
Input-Pulse Width, t_W	5 10	115 60	– –	140 75	– –	ns
Input-Pulse Frequency, $f\phi$	5 10	dc dc	4.4 8.5	dc dc	3.5 6.5	MHz
Input-Pulse Rise or Fall Time, $t_r\phi$, $t_f\phi$	5 10	– –	15 10	– –	15 10	μs

NOTE 1: To minimize power dissipation in the zener diodes, and to ensure device dissipation less than 200 mW, a 150 Ω current-limiting resistor must be placed in series with the power supply for V_{DD} > 13 V.

NOTE 2: Observe power-supply terminal connections, V_{DD} is terminal No. 3 and V_{SS} is *terminal No. 14 (not 16 and 8 respectively, as in all other CD4000A Series* 16-lead devices).

CD4045A Types

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, H Packages			*E Package*			
	V_{DD} (V)	Min.	Typ.	Max.	Min.	Typ.	Max.	
Propagation Delay Time: ϕ to y or y+d out t_{PLH}, t_{PHL}	5	–	2.2	4.4	–	2.2	5.5	μs
	10	–	1.2	2.4	–	1.2	3.3	
Transition Time: t_{THL}, t_{TLH}	5	–	450	800	–	450	900	ns
	10	–	375	650	–	375	750	
Maximum Input-Pulse Frequency, $f_{m\phi}$	5	4.4	5	–	3.5	5	–	MHz
	10	8.5	10	–	6.5	10	–	
Minimum Input-Pulse Width, t_W	5	–	100	115	–	100	140	ns
	10	–	50	60	–	50	75	
Input-Pulse Rise & Fall Time; $t_r\phi$, $t_f\phi$	5	–	–	15	–	–	15	μs
	10	–	–	10	–	–	10	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

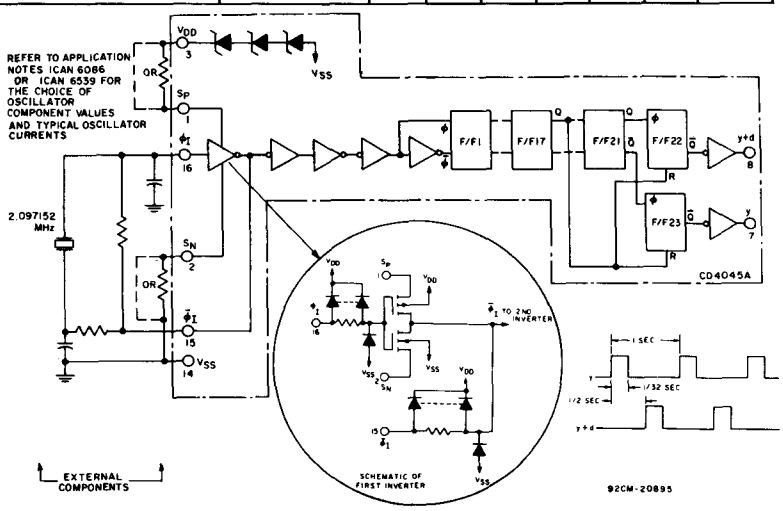


Fig. 3 – CD4045A and outboard components in a typical 21-stage counter application.

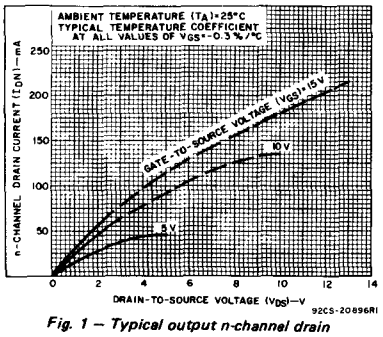


Fig. 1 – Typical output n-channel drain characteristics.

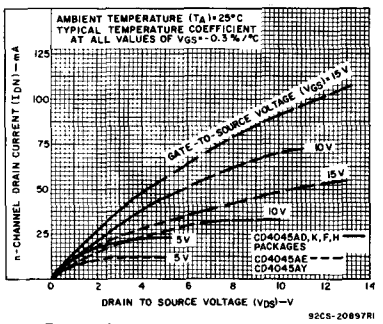


Fig. 2 – Minimum output n-channel drain characteristcs.

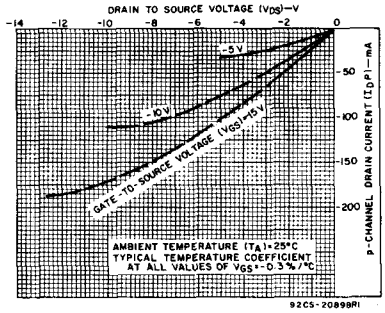


Fig. 4 – Typical output p-channel drain characteristics.

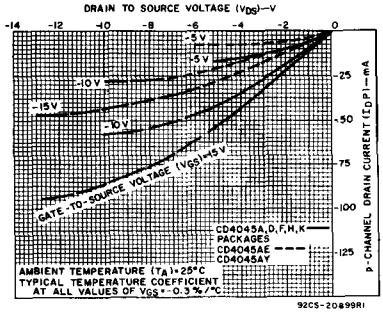


Fig. 5 – Minimum output p-channel drain characteristics.

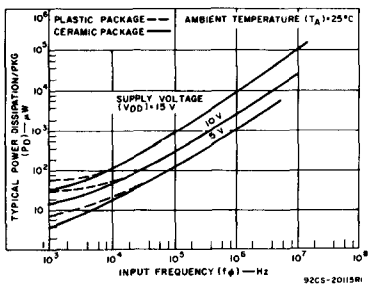


Fig. 6 – Typical dissipation vs input frequency (21 counting stages).

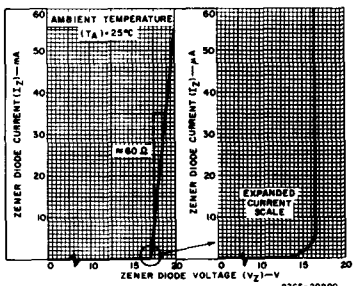


Fig. 7 – Typical zener diode characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_DN Min.	0.5	–	5	4.4	7	3.5	2.5	2.2	7	1.8	1.3	mA
	0.5	–	10	6.9	11	5.5	3.9	3.5	11	2.8	2	
p-Channel (Source): I_DP Min.	4.5	–	5	−3.1	−5	−2.5	−1.8	−1.6	−5	−1.3	−0.9	
	9.5	–	10	−5.6	−9	−4.5	−3.2	−2.8	−9	−2.3	−1.6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA
Zener Breakdown Voltage, $V_{(BR)Z}$	1–100 μA		Min.	13.3	–	13.5	13.7	13.3	–	13.5	13.6	V
			Typ.	–	16.5	–	–	–	16.5	–	–	
			Max.	17.8	–	18	18.2	17.8	–	18	18.1	

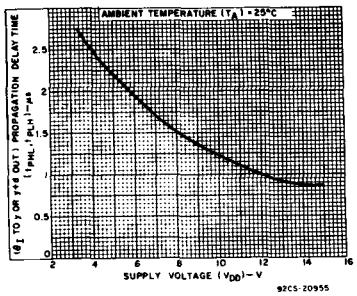


Fig. 8 – Typical propagation delay (ϕ_1 to y or y+d out) vs V_{DD}.

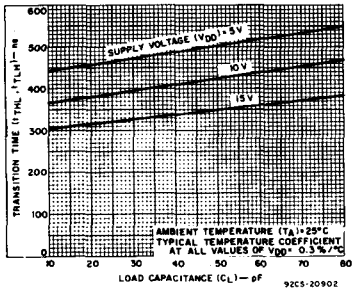


Fig. 9 – Typical transition time vs C_L.

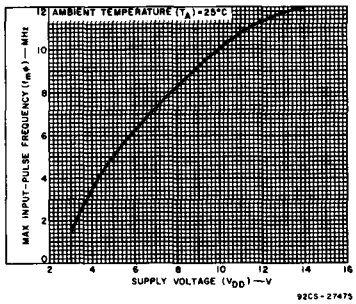


Fig. 10 – Typical maximum input-pulse frequency.

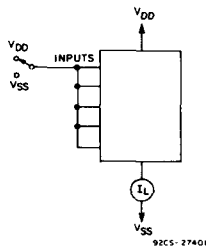


Fig. 11 – Quiescent-device-current test circuit.

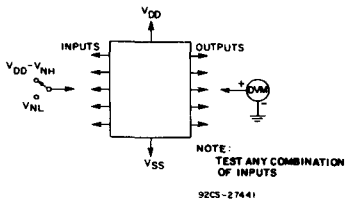


Fig. 12 – Noise-immunity test circuit.

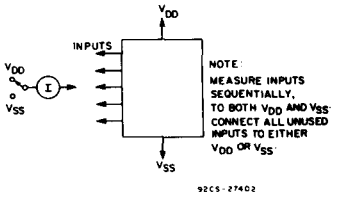


Fig. 13 – Input-leakage-current test circuit.

CMOS Micropower Phase-Locked Loop

The RCA-CD4046A CMOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the RCA-CD4024, CD4018, CD4020, CD4022, CD4029, and CD4059. One or more CD4018 (Preset-table Divide-by-N Counter) or CD4029 (Presettable Up/Down Counter), or CD4059A (Programmable Divide-by-"N" Counter), together with the CD4046A (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0" ≤30% (V_{DD}–V_{SS}), logic "1" ≥ 70% (V_{DD}–V_{SS})]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analagously to an overdriven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_0).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_C$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is ≤ the lock range.

With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 2 shows the typical, triangular, phase-to-output response characteristic

Features:

- **Very low power consumption: 70 μW (typ.) at VCO f_0 = 10 kHz, V_{DD} = 5 V**
- **Operating frequency range up to 1.2 MHz (typ.) at V_{DD} = 10 V**
- **Wide supply-voltage range: $V_{DD} - V_{SS}$ = 5 to 15 V**
- **Low frequency drift: 0.06%/°C (typ.) at V_{DD} = 10 V**
- **Choice of two phase comparators:**
  1. **Exclusive-OR network**
  2. **Edge-controlled memory network with phase-pulse output for lock indication**
- **High VCO linearity: 1% (typ.)**
- **VCO inhibit control for ON-OFF keying and ultra-low standby power consumption**
- **Source-follower output of VCO control input (Demod. output)**
- **Zener diode to assist supply regulation**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**

Applications:

- **FM demodulator and modulator**
- **Frequency synthesis and multiplication**
- **Frequency discriminator**
- **Data synchronization**
- **Voltage-to-frequency conversion**
- **Tone decoding**
- **FSK – Modems**
- **Signal conditioning**
- **(See ICAN-6101) "RCA CMOS Phase-Locked Loop – A Versatile Building Block for Micropower Digital and Analog Applications"**

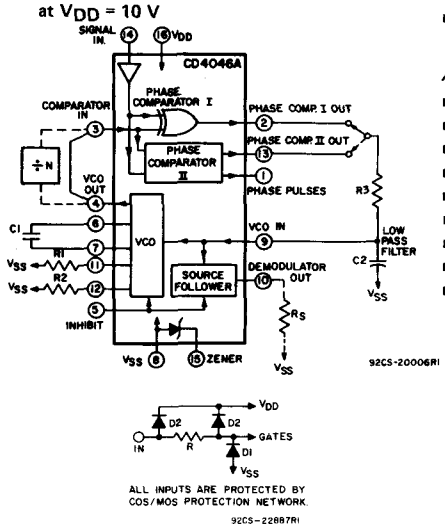


Fig. 1 – COS/MOS phase-locked loop block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

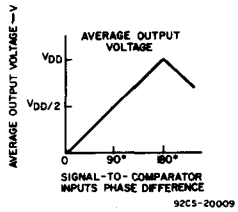


Fig.2 – Phase-comparator I characteristics at low-pass filter output.

of phase-comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition of f_o is shown in Fig. 3.

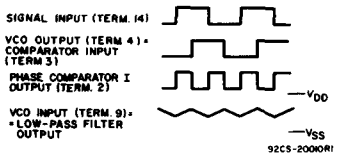


Fig.3 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator I in locked condition of f_o.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range	3	12	V

ELECTRICAL CHARACTERISTICS at $T_A = 25^oC$

Characteristic	Test Conditions	V_O Volts	V_{DD} Volts	Limits All Package Types Min.	Typ.	Max.	Units
Phase Comparator Section							
Operating Supply Voltage, $V_{DD}-V_{SS}$	VCO Operation		–	5	–	15	V
	Comparators only		–	3	–	15	
Total Quiescent Device Current, I_L: Term. 14 Open	Term. 15 open, Term. 5 at V_{DD}, Terms. 3 & 9 at V_{SS}		5	–	25	–	μA
			10	–	200	–	
Term. 14 at V_{SS} or V_{DD}			5	–	5	15	
			10	–	25	60	
			15	–	50	500	
Term. 14 (SIGNAL IN) Input Impedance, Z_{14}			5	1	2	–	MΩ
			10	0.2	0.4	–	
			15	–	0.2	–	
AC-Coupled Signal Input Voltage Sensitivity* (peak-to-peak)	See Fig.7		5	–	200	400	mV
			10	–	400	800	
			15	–	700	–	
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity Low Level			5	1.5	2.25	–	V
			10	3	4.5	–	
			15	4.5	6.75	–	
High Level		V_O Volts	5	–	2.75	3.5	
			10	–	5.5	7	
			15	–	8.25	–	
Output Drive Current: n-Channel (Sink), I_{DN}	Phase Comparator I & II Term. 2 & 13	0.5	5	0.43	0.86	–	mA
		0.5	10	1.3	2.5	–	
	Phase Pulses	0.5	5	0.23	0.47	–	
		0.5	10	0.7	1.4	–	
p-Channel (Source), I_{DP}	Phase Comparator I & II Term. 2 & 13	4.5	5	–0.3	–0.6	–	
		9.5	10	–0.9	–1.8	–	
	Phase Pulses	4.5	5	–0.08	–0.16	–	
		9.5	10	–0.25	–0.5	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	–	$\pm 10^{-5}$	±1	μA

* For sine wave, the frequency must be greater than 1 kHz for Phase Comparator II.

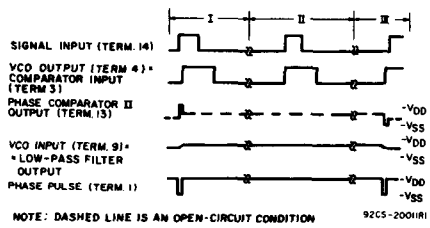


Fig.4 – Typical waveforms for CMOS phase-locked loop employing phase comparator II in locked condition.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic	Test Conditions		V_O Volts	V_{DD} Volts	Limits (All Package Types) Min.	Typ.	Max.	Units
VCO Section								
Operating Supply Voltage $V_{DD}-V_{SS}$	As fixed oscillator only				3	–	15	V
	Phase-lock-loop operation				5	–	15	
Operating Power Dissipation, P_D	f_o = 10 kHz, R_1 = 1 MΩ, R_2 = ∞, $VCO_{IN} = \frac{V_{DD}}{2}$			5	–	70	–	μW
				10	–	600	–	
				15	–	2400	–	
Maximum Operating Frequency, f_{max}	R1 = 10 kΩ, R_2 = ∞, $VCO_{IN} = V_{DD}$	C1 = 100 pF		5	0.25	0.5	–	MHz
		C1 = 50 pF		10	0.6	1.2	–	
				15	–	1.5	–	
Center Frequency (f_o) and Frequency Range, $f_{max}-f_{min}$	Programmable with external components R1, R2, and C1 *See Design Information*							
Linearity	VCO_{IN} = 2.5 V ± 0.3 V, R1 > 10 kΩ			5	–	1	–	%
	= 5 V ± 2.5 V, R1 > 400 kΩ			10	–	1	–	
	= 7.5 V ± 5 V, R1 = 1 MΩ			15	–	1	–	
Temperature-Frequency Stability•: No Frequency Offset f_{MIN} = 0	%/°C ∝ $\frac{1}{f \cdot V_{DD}}$, R2 = ∞			5	–	0.12–0.24	–	%/°C
				10	–	0.04–0.08	–	
				15	–	0.015–0.03	–	
Frequency Offset $f_{MIN} \neq 0$	%/°C ∝ $\frac{1}{f \cdot V_{DD}}$			5	–	0.06–0.12	–	
				10	–	0.05–0.1	–	
				15	–	0.03–0.06	–	
Input Resistance of VCO_{IN} (Term 9), R_I				5,10,15	–	10^{12}	–	Ω
VCO Output Voltage (Term 4) Low Level, V_{OL}	Driving CMOS-Type Load (e.g. Term 3 Phase Comparator Input)			5,10,15	–	–	0.01	V
High Level, V_{OH}				5	4.99	–	–	
				10	9.99	–	–	
				15	14.99	–	–	
VCO Output Duty Cycle				5,10,15	–	50	–	%
VCO Output Transition Times, t_{THL}, t_{TLH}			V_O Volts	5	–	75	150	ns
				10	–	50	100	
				15	–	40	–	
VCO Output Drive Current: n-Channel (Sink), I_{DN}			0.5	5	0.43	0.86	–	mA
			0.5	10	1.3	2.6	–	
p-Channel (Source), I_{DP}			4.5	5	–0.3	–0.6	–	
			9.5	10	–0.9	–1.8	–	
Source-Follower Output (Demodulated Output): Offset Voltage ($VCO_{IN}-V_{DEM}$)	R_S > 10 kΩ			5,10	–	1.5	2.2	V
				15	–	1.5	–	
Linearity	R_S>50kΩ	VCO_{IN} = 2.5±0.3 V		5	–	0.1	–	%
		= 5±2.5 V		10	–	0.6	–	
		= 7.5±5 V		15	–	0.8	–	
Zener Diode Voltage (V_Z)	I_Z = 50 μA				4.5	5.2	6.1	V
Zener Dynamic Resistance, R_Z	I_Z = 1 mA				–	100	–	Ω

• Positive coefficient.

Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 4 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

DESIGN INFORMATION

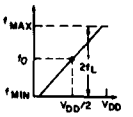
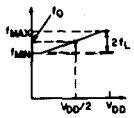
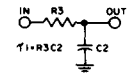
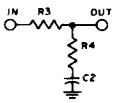
This information is a guide for approximating the values of external components for the CD4046A in a Phase-Locked-Loop system. The selected external components must be within the following ranges:

$10\ k\Omega \leqslant R1, R2, R_S \leqslant 1\ M\Omega$

$C1 \geqslant 100\ pF$ at $V_{DD} \geqslant 5\ V$;

$C1 \geqslant 50\ pF$ at $V_{DD} \geqslant 10\ V$

In addition to the given design information refer to Fig.5 for R1, R2, and C1 component selections.

Characteristics	Phase Comparator Used	Design Information	
VCO Frequency	1	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
		 VCO INPUT VOLTAGE	 VCO INPUT VOLTAGE 92CS-20012R
	2	Same as for No.1	
For No Signal Input	1	VCO will adjust to center frequency, f_o	
	2	VCO will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2f_L$	1	$2f_L$ = full VCO frequency range	
		$2f_L = f_{max} - f_{min}$	
	2	Same as for No.1	
Frequency Capture Range, $2f_C$	1	 $\tau 1 = R3C2$	(1), (2) $2f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$
Loop Filter Component Selection		 92CS-21901	For $2f_C$, see Ref. (2)
	2	$f_C = f_L$	
Phase Angle Between Signal and Comparator	1	90^o at center frequency (f_o) approximating 0^o and 180^o at ends of lock range ($2f_L$)	
	2	Always 0^o in lock	

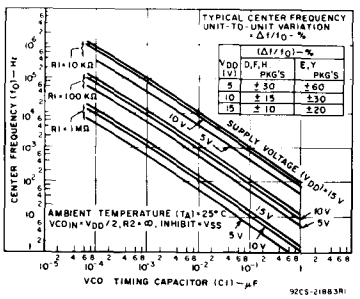


Fig.5(a) — Typical center frequency vs C1 for R1 = 10 kΩ, and 1 MΩ and $f_o \sim 1/R1\ C1$.

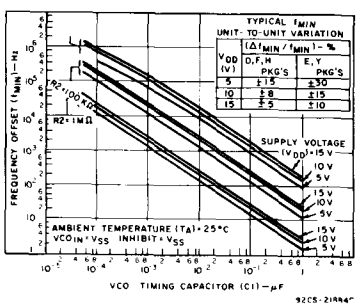


Fig.5(b) — Typical frequency offset vs C1 for R2 = 10 kΩ, 100 kΩ, and 1 MΩ.

NOTE: Lower frequency values are obtainable if larger values of C1 than shown in Figs. 5(a) and 5(b) are used.

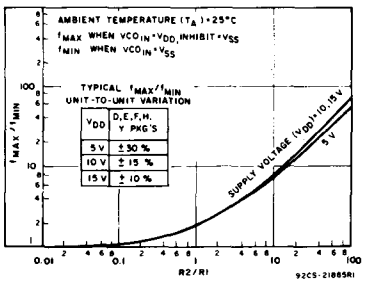


Fig.5(c) — Typical f_{max}/f_{min} vs R2/R1.

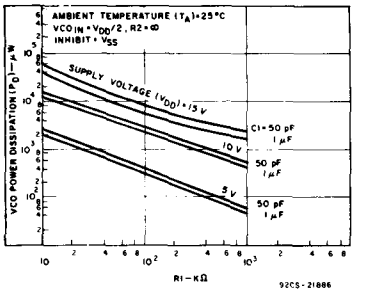


Fig.6(a) — Typical VCO power dissipation at center frequency vs R1.

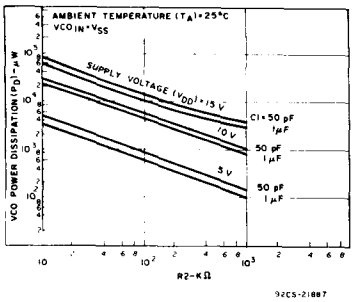


Fig.6(b) — Typical VCO power dissipation at f_{min} vs R2.

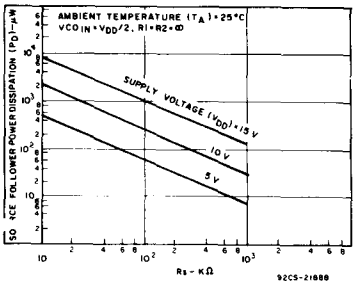


Fig.6(c) — Typical source follower power dissipation vs R_S.

NOTE: To obtain approximate total power dissipation of PLL system for no-signal input

P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S) — Phase Comparator I

P_D (Total) = P_D (f_{MIN}) — Phase Comparator II

DESIGN INFORMATION (Cont'd):

Characteristics	Phase Comparator Used	Design Information	
Locks On Harmonic of Center Frequency	1	Yes	
	2	No	
Signal Input Noise Rejection	1	High	
	2	Low	
VCO Component Selection	1	**VCO WITHOUT OFFSET** $R_2 = \infty$ – Given: f_o – Use f_o with Fig.5a to determine R1 and C1	**VCO WITH OFFSET** – Given: f_o and f_L – Calculate f_{min} from the equation $f_{min} = f_o - f_L$ – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1
	2	– Given: f_{max} – Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$ –Use f_o with Fig.5a to determine R1 and C1	– Given: f_{min} & f_{max} – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1

For further information, see

(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966

(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

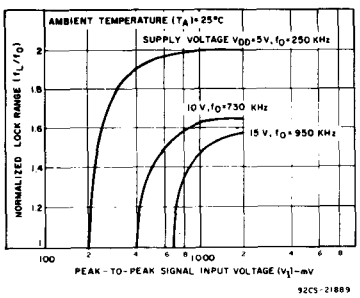
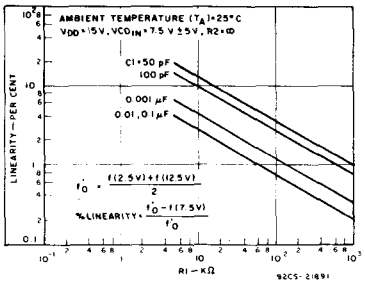


Fig.7 – Typical lock range vs signal input amplitude.



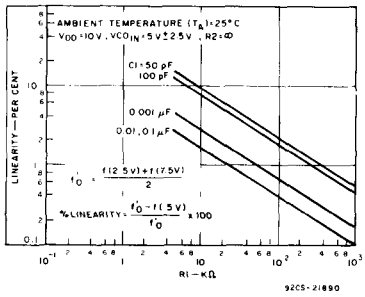


Fig.8(a) and (b) – Typical VCO linearity vs R1 and C1.

CMOS Low-Power Monostable/Astable Multivibrator

The RCA-CD4047A consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, −TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, $\overline{Q}$, and OSCILLATOR. In all modes of operation an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the ASTABLE input. The period of the square wave at the Q and $\overline{Q}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{\text{ASTABLE}}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output.

In the monostable mode, positive-edge triggering is accomplished by application of a leading-edge pulse to the +TRIGGER input and a low level to the −TRIGGER input. For negative-edge triggering, a trailing-edge pulse is applied to the −TRIGGER and a high level is applied to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode the output pulse remains high as long as the RETRIGGER input is high, with or without transitions.

An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator.

A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a high-level or power-on reset pulse, must be applied to the EXTERNAL RESET whenever V_{DD} is applied.

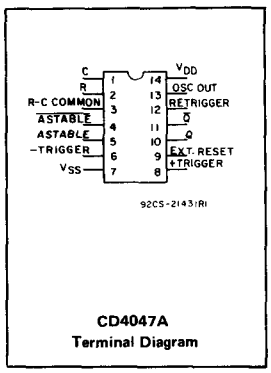
These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and F suffixes), 14-lead dual-in-line plastic packages (E suffix), 14-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Low power consumption: special COS/MOS oscillator configuration**
- **Monostable (one-shot) or astable (free-running) operation**
- **True and complemented buffered outputs**
- **Only one external R and C required**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Monostable Multivibrator Features:

- **Positive- or negative-edge trigger**
- **Output pulse width independent of trigger pulse duration**
- **Retriggerable option for pulse width expansion**
- **Long pulse widths possible using small RC components by means of external counter provision**
- **Fast recovery time essentially independent of pulse width**
- **Pulse-width accuracy maintained at duty cycles approaching 100%**



CD4047A Terminal Diagram

Astable Multivibrator Features:

- **Free-running or gatable operating modes**
- **50% duty cycle**
- **Oscillator output available**
- **Good astable frequency stability:**
  Frequency deviation:
  =±2% + 0.03%/°C @ 100 kHz
  =±0.5% + 0.015%/°C @ 10 kHz
  (circuits "trimmed" to frequency V_{DD} = 10 V ± 10%)

Applications :

Digital equipment where low-power dissipation and/or high noise immunity are primary design requirements:

- **Envelope detection**
- **Frequency multiplication**
- **Frequency division**
- **Frequency discriminators**
- **Timing circuits**
- **Time-delay applications**

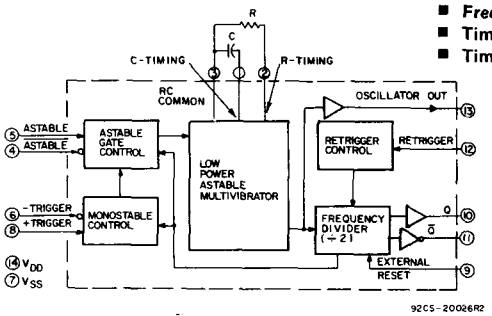


Fig. 1 – CD4047A logic block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . −55 to +125°C

PACKAGE TYPE E . . . . . −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D)

FOR T_A = −40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

CD4047A Types

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD}	LIMITS				UNITS
		D, F, K, H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A=Full Package- Temperature Range)		3	12	3	12	V
Input Pulse Width, t_W (Any Input)	5	1000	–	1300	–	ns
	10	400	–	600	–	
Trigger, Retrigger Rise or Fall Time, t_r, t_f	5	–	15	–	15	μs
	10	–	5	–	5	

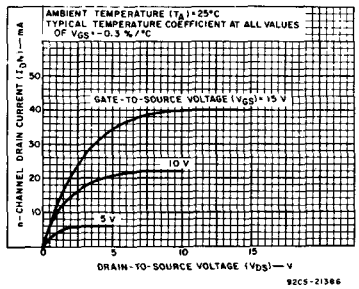


Fig. 2 – Typical output n-channel drain characteristics for Q and $\overline{Q}$ buffers.

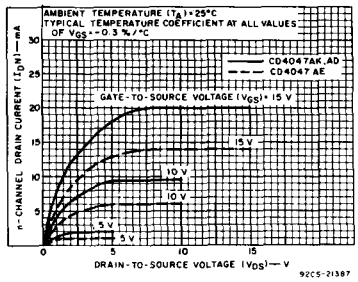


Fig. 3 – Minimum output n-channel drain characteristics for Q and $\overline{Q}$ buffers.

STATIC ELECTRICAL CHARACTERISTICS

Characteristics	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				*E Package*				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	–55	+25 Typ.	+25 Limit	+125	– 40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	5	0.03	5	300	50	0.1	50	700	μA
	–	–	10	10	0.05	10	600	100	0.2	100	1400	
	–	–	15	50	1	50	2000	500	5	500	5000	
Output Voltage: Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min., 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min., 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5		5	1 Min.								V
	9		10	1 Min.								
Inputs High, V_{NMH}	0.5		5	1 Min.								
	1		10	1 Min.								
Output Drive Current: (Q,$\overline{Q}$ Outputs) n-channel (Sink), I_{DN} Min.	0.5	–	5	0.5	0.8	0.4	0.28	0.34	0.8	0.28	0.23	mA
	0.5	–	10	1.25	2	1	0.7	0.85	2	0.7	0.6	
p-Channel (Source): I_{DP} Min.	4.5	–	5	-0.5	-0.8	-0.4	-0.28	-0.34	-0.8	-0.28	-0.23	
	9.5	–	10	-1.25	-2	-1	-0.7	-0.85	-2	-0.7	-0.6	
Input Leakage Current, I_{IL},I_{IH}	Any Input											μA
	–	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								

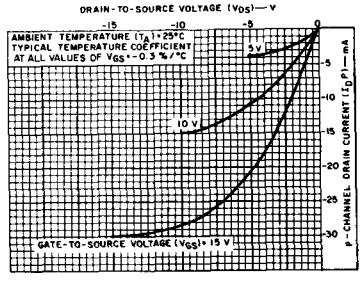


Fig. 4. – Typical output p-channel drain characteristics for Q and $\overline{Q}$ buffers.

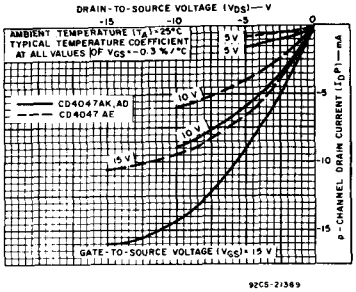


Fig. 5 – Minimum output p-channel drain characteristics for Q and $\overline{Q}$ buffers.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTICS	TEST CONDITIONS	LIMITS						UNITS
		D, F, K, H Packages			*E Package*			
	V_{DD} (Volts)	Min.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time: t_{PHL}, t_{PLH} Astable, Astable to Osc. Out	5	–	200	400	–	200	550	ns
	10	–	100	200	–	100	275	
Astable, Astable to Q, $\overline{Q}$	5	–	550	900	–	550	1200	
	10	–	250	500	–	250	650	
+Trigger, –Trigger to Q, $\overline{Q}$	5	–	700	1200	–	700	1600	
	10	–	300	600	–	300	800	
+Trigger, Retrigger to Q, $\overline{Q}$	5	–	300	600	–	300	800	
	10	–	175	300	–	175	400	
External Reset to Q, $\overline{Q}$	5	–	300	600	–	300	800	
	10	–	125	250	–	125	350	
Transition Time: t_{THL}, t_{TLH} Q, $\overline{Q}$	5	–	75	125	–	75	150	ns
	10	–	45	75	–	45	100	
Osc. Out	5	–	75	150	–	75	180	
	10	–	45	100	–	45	130	
Minimum Input Pulse Width (any input), t_W*	5	–	500	1000	–	500	1300	ns
	10	–	200	400	–	200	600	
+Trigger, Retrigger Rise & Fall Time, t_r, t_f	5	–	–	15	–	–	15	μs
	10	–	–	5	–	–	5	
Average Input Capacitance, C_I	Any Input	–	–	5	–	–	5	pF

* Input pulse widths below the minimum specified may cause malfunction of the unit. See Application Note ICAN - 6230

CD4047A FUNCTIONAL TERMINAL CONNECTIONS
NOTE: IN ALL CASES EXTERNAL RESISTOR BETWEEN TERMINALS 2 AND 3▲
EXTERNAL CAPACITOR BETWEEN TERMINALS 1 AND 3▲

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT PULSE TO		
Astable Multivibrator:					
Free Running	4,5,6,14	7,8,9,12	–	10,11,13	t_A(10,11)=4.40 RC
True Gating	4,6,14	7,8,9,12	5	10,11,13	t_A(13)=2.20 RC
Complement Gating	6,14	5,7,8,9,12	4	10,11,13	
Monostable Multivibrator:					
Positive-Edge Trigger	4,14	5,6,7,9,12	8	10,11	t_M(10,11)=2.48 RC
Negative-Edge Trigger	4,8,14	5,7,9,12	6	10,11	
Retriggerable	4,14	5,6,7,9	8,12	10,11	
External Countdown*	14	5,6,7,8,9,12	–	10,11	

* Input Pulse to Reset of External Counting Chip External Counting Chip Output To Terminal 4 ▲ See Text.

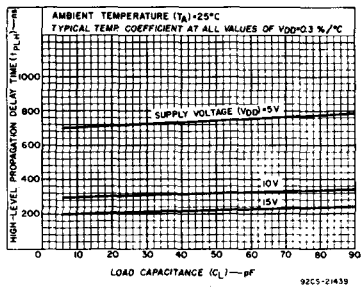


Fig. 6 – Typical low-to-high level propagation delay time vs load capacitance for Q and $\overline{Q}$ buffers.

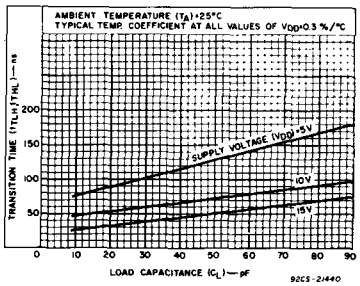


Fig. 7 – Typical transition time vs load capacitance for Q and $\overline{Q}$ buffers.

I. Astable Mode Design Information

A. Unit-to-Unit Transfer-Voltage Variations.

The following analysis presents worst-case variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33%–67% V_{DD}) for free-running (astable) operation.

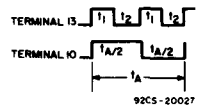


Fig. 8 – Astable mode waveforms.

$$t_1 = -RC \ln \frac{V_{TR}}{V_{DD} + V_{TR}}$$

$$t_2 = -RC \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}}$$

$$t_A = 2(t_1 + t_2)$$

$$= -2\,RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})}$$

Typ: $V_{TR} = 0.5\,V_{DD}$ $t_A = 4.40\,RC$
Min: $V_{TR} = 0.33\,V_{DD}$ $t_A = 4.62\,RC$
Max: $V_{TR} = 0.67\,V_{DD}$ $t_A = 4.62\,RC$

thus if $\boxed{t_A = 4.40\,RC}$ is used, the maximum variation will be (+5.0%,–0.0%).

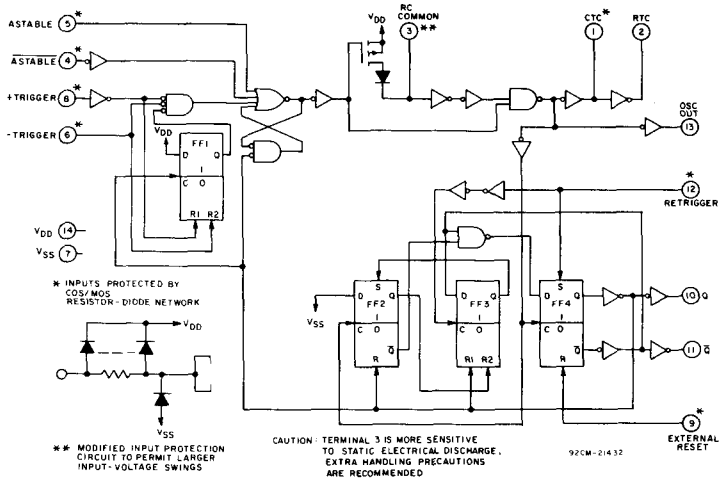


Fig. 9 – CD4047A logic diagram.

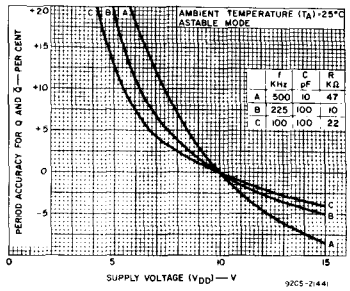


Fig. 10 – Typical Q-and-Q̄-period accuracy vs supply voltage (high frequency).

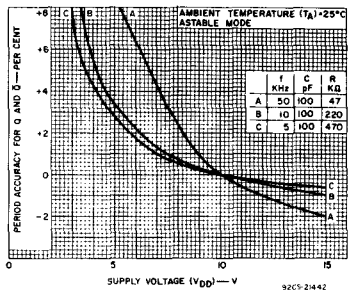


Fig. 11 – Typical Q-and-Q̄-period accuracy vs supply voltage (medium frequency)

B. Variations Due to V_{DD} and Temperature Changes

In addition to variations from unit to unit, the astable period may vary as a function of frequency with respect to V_{DD} and temperature. Typical variations are presented in graphical form in Figs. 10 to 20 with 10 V as reference for voltage variation curves and 25°C as reference for temperature variation curves.

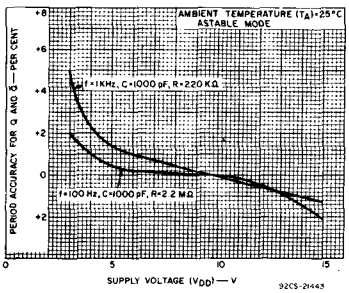


Fig. 12 – Typical Q-and-Q̄-period accuracy vs supply voltage (low frequency).

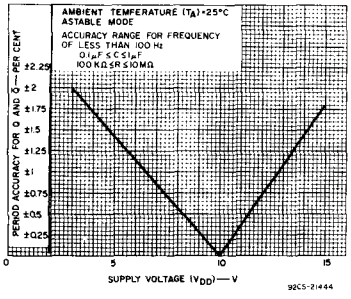


Fig. 13 – Typical Q-and-Q̄- period accuracy vs supply voltage (very low frequency).

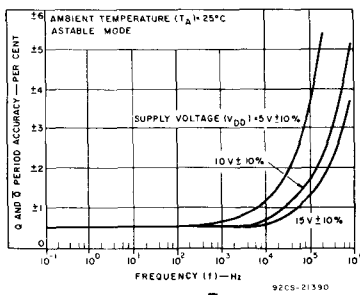


Fig. 14 – Typical Q-and Q̄-period accuracy vs frequency for V_{DD} variation of ±10% from value indicated.

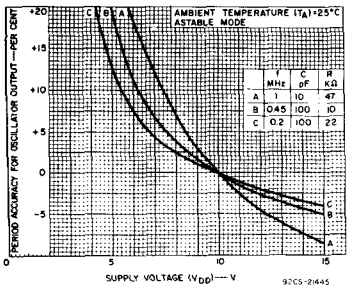


Fig. 15 – Typical oscillator-output-period accuracy vs supply voltage (high frequency).

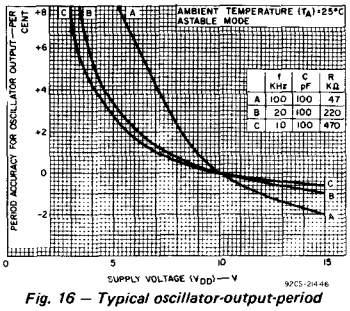


Fig. 16 – Typical oscillator-output-period accuracy vs supply voltage (medium frequency).

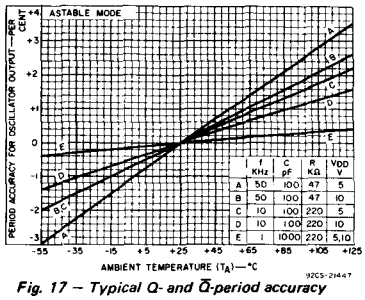


Fig. 17 – Typical Q- and Q̄-period accuracy vs temperature (medium frequency).

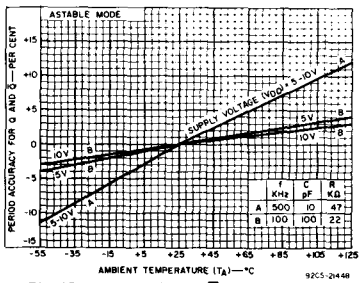


Fig. 18 – Typical Q- and Q̄-period accuracy vs temperature (high frequency).

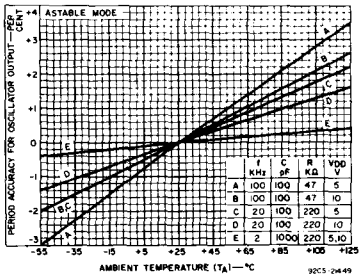


Fig. 19 – Typical oscillator-period accuracy vs temperature (medium frequency).

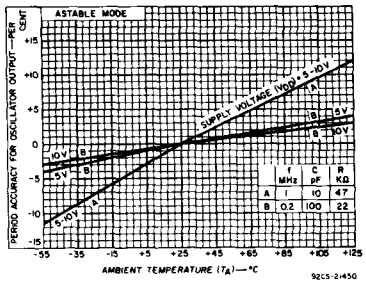


Fig. 20 – Typical oscillator-period accuracy vs temperature (high frequency).

II. Monostable Mode Design Information

The following analysis presents worst-case variations from unit to unit as a function of transfer-voltage (V_{TR}) shift (33% – 67% V_{DD}) for one-shot (monostable) operation.

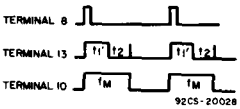


Fig. 21 – Monostable waveforms.

$$t_1' = -RC \ln \frac{V_{TR}}{2V_{DD}}$$

$$t_M = (t_1' + t_2)$$

$$t_M = -RC \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})}$$

where t_M = Monostable mode pulse width. Values for t_M are as follows:

Typ: $V_{TR} = 0.5\ V_{DD}$ $t_M = 2.48\ RC$
Min: $V_{TR} = 0.33\ V_{DD}$ $t_M = 2.71\ RC$
Max. $V_{TR} = 0.67\ V_{DD}$ $t_M = 2.48\ RC$

Thus if $\boxed{t_M = 2.48\ RC}$ is used, the maximum variation will be (+9.3%, –0.0%).

Note:

In the astable mode, the first positive half cycle has a duration of T_M; succeeding durations are $t_A/2$.

In addition to variations from unit to unit, the monostable pulse width may vary as a function of frequency with respect to V_{DD} and temperature. These variations are presented in graphical form in Fig. 22 to 27 with 10 V as reference for voltage-variation curves and 25°C as reference for temperature-variation curves.

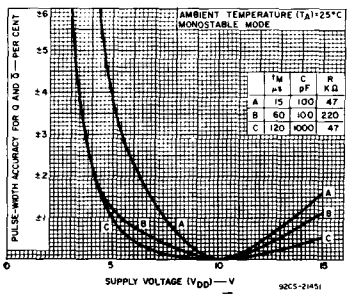


Fig. 22 – Typical Q- and Q̄-pulse-width accuracy vs supply voltage (t_M = 15, 60, 120 µs).

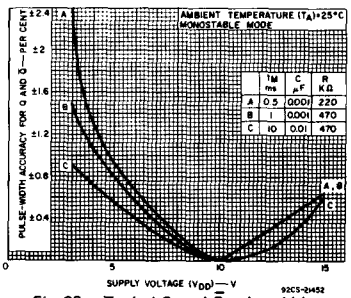


Fig. 23 – Typical Q- and Q̄-pulse-width accuracy vs supply voltage (t_M = 0.5, 1, 10 ms).

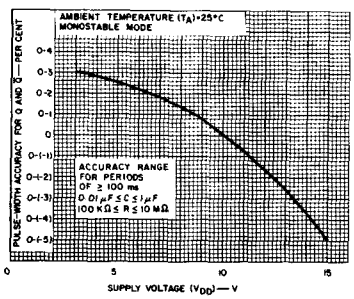


Fig. 24 – Typical Q- and Q̄-pulse-width accuracy vs supply voltage ($t_M \geq 100$ ms).

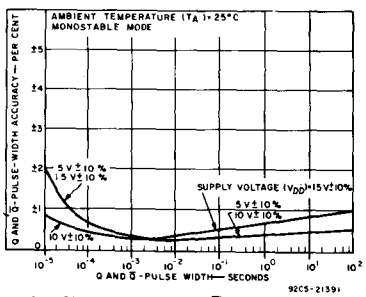


Fig. 25 – Typical Q- and Q̄ pulse-width accuracy vs Q and Q̄ pulse width for a variation of ± 10% from value indicated.

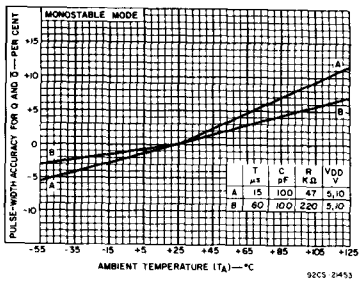


Fig. 26 – Typical Q and Q̄ pulse-width accuracy vs temperature (high frequency).

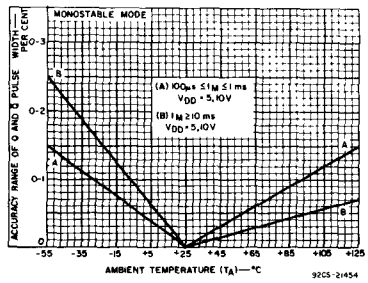


Fig. 27 – Typical Q and Q̄ pulse-width accuracy range vs temperature.

III. Retrigger Mode Operation

The CD4047A can be used in the retrigger mode to extend the output-pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminals 8 and 12, and the output is taken from terminal 10 or 11. As shown in Fig. 28, normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied. For two input pulses, $t_{RE}=t_1' + t_1 + 2t_2$. For more than two pulses, t_{RE} (Q OUTPUT), terminates at some variable time, t_D, after the termination of the last retrigger pulse, t_D is variable because t_{RE} (Q OUTPUT) terminates after the second positive edge of the oscillator output appears at flip-flop 4 (see Fig. 8).

IV. External Counter Option

Time t_M can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Fig. 29. The pulse duration at the output is

$$t_{ext} = (N-1)(t_A) + (t_M + t_A/2)$$

where t_{ext}= pulse duration of the circuitry, and N is the number of counts used.

V. Timing-Component Limitations

The capacitor used in the circuit should be non-polarized and have low leakage(i.e. the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the CMOS "ON" resistance in series with it, which typically is hundreds of ohms. In addition, with very large values of R, some short-term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

$C \geqslant 100$ pF, up to any practical value, for astable modes;

$C \geqslant 1000$ pF, up to any practical value for monostable modes.

$10\ k\Omega \leqslant R \leqslant 1\ M\Omega$

VI. Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formulae:

Astable Mode: $P = 2CV^2f$. (Output at terminal No. 13)
$P = 4CV^2f$. (Output at terminal Nos. 10 and 11)

Monostable Mode:

$$P = \frac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$$

(Output at terminal Nos. 10 and 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above). See Figs. 30–32 for typical power consumption in astable mode.

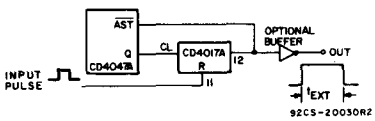


Fig. 28 – Implementation of external counter option.

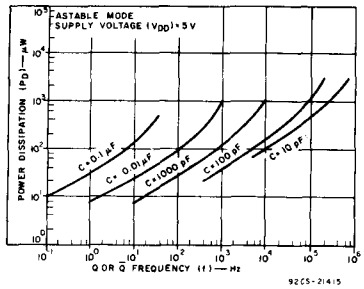


Fig. 30 – Power dissipation vs output frequency (V_{DD} = 5 V).

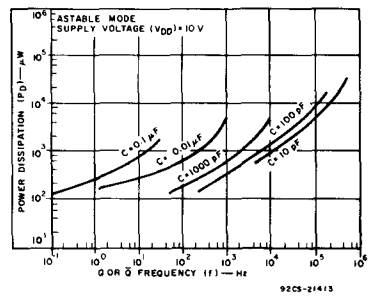


Fig. 31 – Power dissipation vs output frequency (V_{DD} = 10 V).

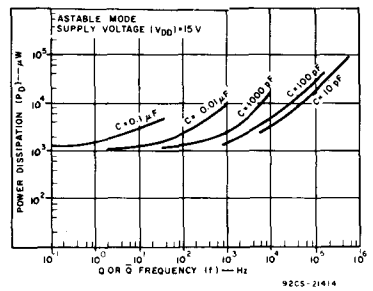


Fig. 32 – Power dissipation vs output frequency (V_{DD} = 15 V).

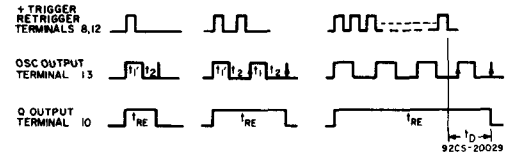


Fig. 29 – Retrigger-mode waveforms.

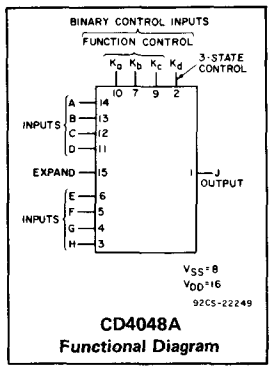
CMOS Multi-Function Expandable 8-Input Gate

The RCA-CD4048A is an 8-input gate having four control inputs. Three binary control inputs – Ka, Kb, and Kc – provide the implementation of eight different logic functions. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR, and AND/NOR.

A fourth control input –Kd – provides the user with 3-state outputs. When control input Kd is high the output is either a logic 1 or a logic 0 depending on the input states. When control input Kd is low, the output is an open circuit. This feature enables the user to connect this device to a common bus line.

In addition to the eight input lines, an EXPAND input is provided that permits the user to increase the number of inputs to one CD4048A, (see Fig. 6). For example, two CD4048A's can be cascaded to provide a 16-input multifunction gate. When the EXPAND input is not used, it should be connected to V_{SS}.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).



CD4048A
Functional Diagram

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . –65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H . . . . . –55 to +125°C
PACKAGE TYPE E . . . . . –40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal): . . . . . –0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = –40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) . . . . Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS . . . . . –0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ±1/32 inch (1.59 ±0.79 mm) from case for 10 s max . . . . . +265°C

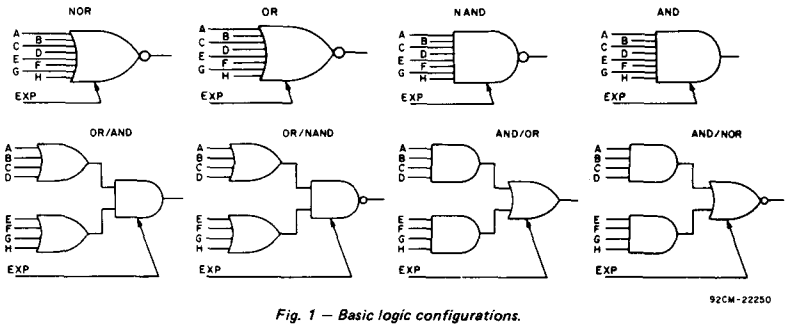


Fig. 1 – Basic logic configurations.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		E Package		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V

Features:

- **Medium-power TTL drive capability**
- **Three-state output**
- **High current source and sink capability 9 mA (typ.) @ V_{DS} = 0.5 V, V_{DD} = 10 V**
- ***Many logic functions available in one package***
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Applications:

- **Selection of up to 8 logic functions**
- **Digital control of logic**
- **General-purpose gating logic**
  - ***Decoding***
  - **Encoding**

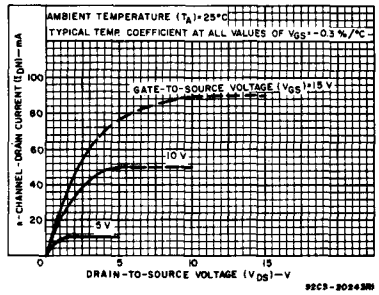


Fig. 2– Typical output n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	1	0.005	1	60	10	0.01	10	140	μA
	–	–	10	2	0.01	2	120	20	0.02	20	280	
	–	–	15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	1	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: n-Channel (Sink) I_DN Min.	0.4	–	4.5	2	3.2	1.6	1.1	1.9	3.2	1.6	1.3	mA
	0.5	–	10	5.6	9	4.5	3.1	5.4	9	4.5	3.7	
p-channel (Source), I_DP Min.	4.6	–	5	−2	−3.2	−1.6	−1.1	−1.9	−3.2	−1.6	−1.3	
	9.5	–	10	−5.6	−9	−4.5	−3.1	−3.8	−9	−3.15	−2.6	
Input Leakage Current, I_{IL}, I_{IH}	Any Input											μA
	–	–	15	$\pm 10^{-5}$ Typ., ± 1 Max.								
3-State Output Leakage Current I_{OL}, I_{OH}	Forced (Output Disabled)											μA
	–	–	15	$\pm 10^{-4}$ Typ., ±2 Max.								

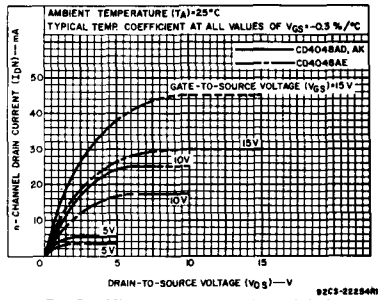


Fig. 3— Minimum output n-channel drain characteristics

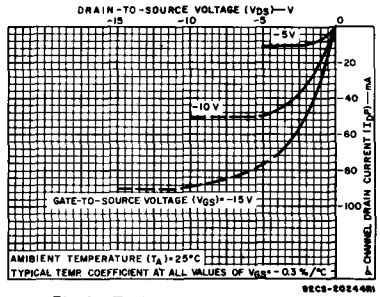


Fig. 4— Typical output p-channel drain characteristics.

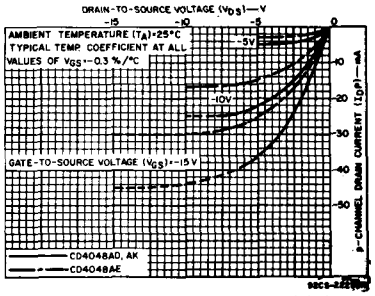


Fig. 5— Minimum output p-channel drain characteristics.

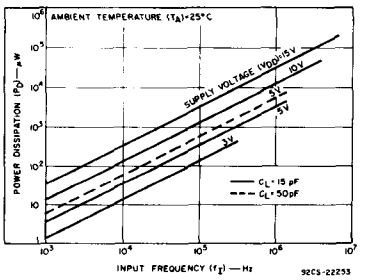


Fig. 6— Typical power dissipation as a function of input frequency.

DYNAMIC ELECTRICAL CHARACTERISTCS at T_A = 25°C and C_L = 15 pF and 50 pF,
Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C R_L = 200 kΩ

C_L = 15 pF

CHARACTERISTIC	TEST CONDITIONS		LIMITS				UNITS
			D, F, K, H Packages		*E Package*		
		V_{DD} (Volts)	TYP.	MAX.*	TYP.	MAX.*	
Propagation Delay Time t_{PHL}		5	750	1300	750	1600	ns
		10	225	400	225	500	
Transition Time: High-to-Low Level t_{THL}		5	90	140	90	170	ns
		10	30	50	30	65	
Low-to-High Level t_{TLH}		5	130	250	130	300	ns
		10	40	60	40	75	
Input Capacitance C_I	Any Input		5	–	5	–	pF
C_L = 50 pF							
Propagation Delay Time t_{PLH}, t_{PHL}		5	775	1350	775	1650	ns
		10	240	430	240	530	
Transition Time: High-to-Low Level t_{THL}		5	105	170	105	200	ns
		10	40	70	40	85	
Low-to-High Level t_{TLH}		5	145	280	145	330	ns
		10	50	80	50	95	
Input Capacitance C_I	Any Input		5	–	5	–	pF

* Max. Limits represent worst-case limits for worst-case modes of operation shown in Figs. 15, 16, and 17.

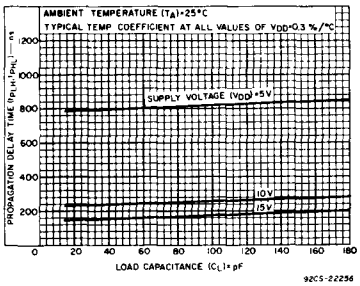


Fig. 7— Typical propagation delay time as a function of load capacitance.

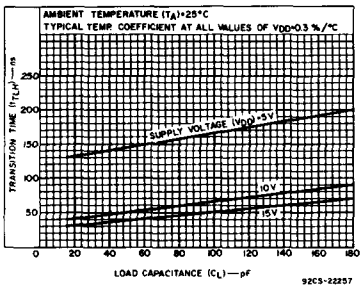


Fig. 8— Typical low-to-high level transition time as a function of load capacitance.

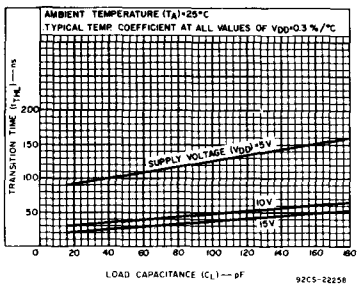


Fig. 9— Typical high-to-low level transition time as a function of load capacitance.

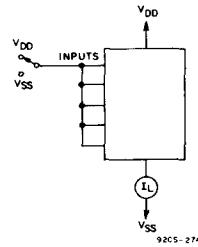


Fig. 10— Quiescent-device-current test circuit.

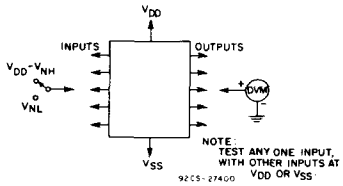


Fig. 11— Noise-immunity test circuit.

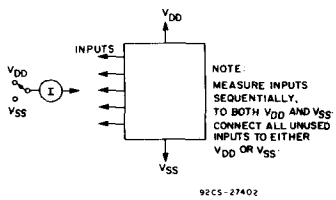
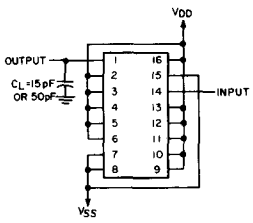


Fig. 12— Input-leakage-current test circuit.



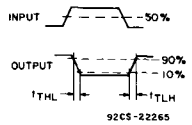
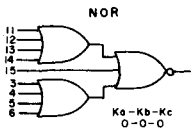


Fig. 13— t_{THL}, t_{TLH} — AND/NOR.



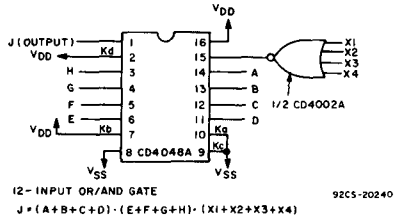
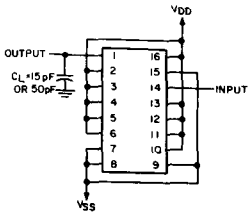


Fig. 14(a) - 12-input OR/AND gate.



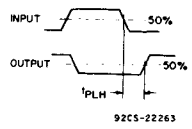
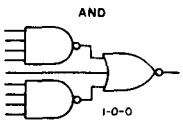
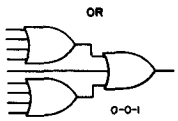


Fig. 15- t_{PLH} - NAND.





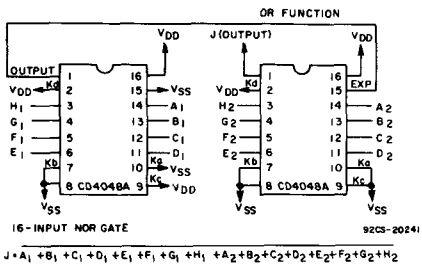
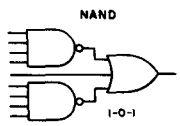


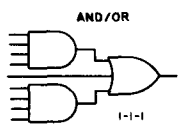
Fig. 14(b) 16-input NOR gate.
Applications of Expand Input

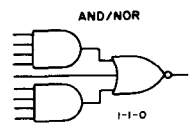


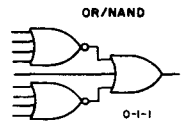
IMPLEMENTATION OF EXPAND INPUT FOR 9 OR MORE INPUTS

OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J=\overline{(A+B+C+D+E+F+G+H)+(EXP)}$
OR	OR	$J=(A+B+C+D+E+F+G+H)+(EXP)$
AND	NAND	$J=(ABCDEFGH)\cdot\overline{(EXP)}$
NAND	NAND	$J=\overline{(ABCDEFGH)\cdot\overline{(EXP)}}$
OR/AND	NOR	$J=(A+B+C+D)\cdot(E+F+G+H)\cdot\overline{(EXP)}$
OR/NAND	NOR	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)\cdot\overline{(EXP)}}$
AND/NOR	AND	$J=\overline{(ABCD)+(EFGH)+(EXP)}$
AND/OR	AND	$J=(ABCD)+(EFGH)+(EXP)$

Note: (EXP) designates the EXPAND function (i.e., $X_1+X_2+\ldots X_N$).







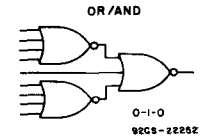
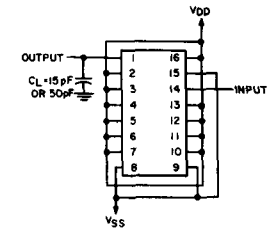


Fig. 14(c) Actual-circuit logic configurations.

Fig. 14- Expansion logic and truth table.



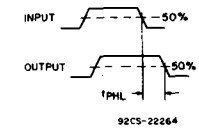
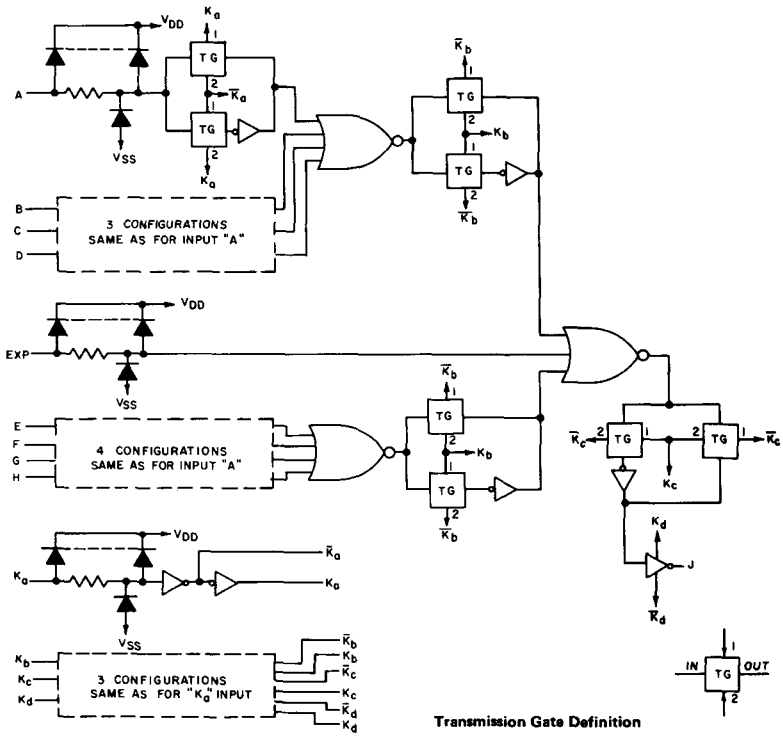


Fig. 16- t_{PHL} - AND.



Transmission Gate Definition

TG = Transmission Gate
Input to Output is:

a) A bidirectional low impedance when control input 1 is low and control 2 is high.

b) An open circuit when control input 1 is high and control input 2 is low.

92CM-22251RI

FUNCTION TRUTH TABLE

OUTPUT FUNCTION	BOOLEAN EXPRESSION	K_a	K_b	K_c	UNUSED INPUT*
NOR	$J=\overline{A+B+C+D+E+F+G+H}$	0	0	0	V_{SS}
OR	$J=A+B+C+D+E+F+G+H$	0	0	1	V_{SS}
OR/AND	$J=(A+B+C+D)\cdot(E+F+G+H)$	0	1	0	V_{SS}
OR/NAND	$J=\overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	V_{SS}
AND	$J=ABCDEFGH$	1	0	0	V_{DD}
NAND	$J=\overline{ABCDEFGH}$	1	0	1	V_{DD}
AND/NOR	$J=\overline{ABCD+EFGH}$	1	1	0	V_{DD}
AND/OR	$J=ABCD+EFGH$	1	1	1	V_{DD}
K_d=1 Normal Inverter Action					
K_d=0 High Impedance Output					

EXPAND Input=0

*See Figs. 1 and 7.

Fig. 17– Logic diagram and truth table.

CD4049A, CD4050A Types

CMOS Hex Buffer/Converters

CD4049A—Inverting Type
CD4050A—Non-Inverting Type

The CD4049A and CD4050A are inverting and non-inverting hex buffers, respectively, and feature logic-level conversion using only one supply voltage (V_{CC}). The input-signal high level (V_{IH}) can exceed the V_{CC} supply voltage when these devices are used for logic-level conversions. These devices are intended for use as CMOS to DTL/TTL converters and can drive directly two DTL/TTL loads. (V_{CC}=5 V, $V_{OL} \geqslant$0.4 V, and $I_DN \geqslant$3.2 mA.)

The CD4049A and CD4050A are designated as replacements for CD4009A and CD4010A, respectively. Because the CD4049A and CD4050A require only one power supply, they are preferred over the CD4009A and CD4010A and should be used in place of the CD4009A and CD4010A in all inverter, current driver, or logic-level conversion applications. In these applications the CD4049A and CD4050A are pin compatible with the CD4009A and CD4010A respectively, and can be substituted for these devices in existing as well as in new designs. Terminal No. 16 is not connected internally on the CD4049A or CD4050A, therefore, connection to this terminal is of no consequence to circuit operation. For applications not requiring high sink-current or voltage conversion, the CD4069 Hex Inverter is recommended.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **High sink current for driving 2 TTL loads**
- **High-to-low level logic conversion**
- **Quiescent current specified to 15 V**
- **Maximum input leakage of 1 μA at 15 V (full package-temperature range)**

Applications:

- **CMOS to DTL/TTL hex converter**
- **CMOS current "sink" or "source" driver**
- **CMOS high-to-low logic-level converter**

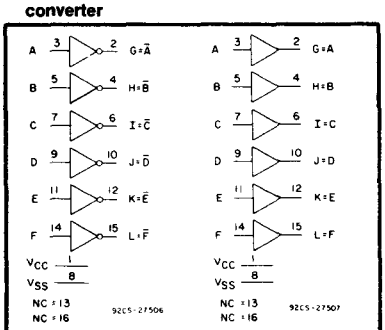


Fig. 1 — Functional diagrams.

RECOMMENDED OPERATING CONDITIONS at T_A=25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (V_{CC}) (For T_A=Full Package-Temperature Range)	3	12	V
Input Voltage Range (V_I)	V_{CC}*	12	V

*The CD4049 and CD4050 have high-to-low-level voltage conversion capability but not low-to-high-level; therefore it is recommended that $V_I \geqslant V_{CC}$.

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				*E Package*				
	V_O (V)	V_{IN} (V)	V_{CC} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current, I_L Max.	–	–	5	0.3	0.01	0.3	20	3	0.03	3	42	μA
	–	–	10	0.5	0.01	0.5	30	5	0.05	5	70	
	–	–	15	10	0.02	10	100	50	0.05	50	500	
Output Voltage: Low-Level, V_{OL}	–	0, 5	5	0 Typ.; 0.05 Max.								V
	–	0, 10	10	0 Typ.; 0.05 Max.								
High-Level, V_{OH}	–	0, 5	5	4.95 Min.; 5 Typ.								
	–	0, 10	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL} CD4050A	3.6	–	5	1.5 Min.; 2.25 Typ.								V
	7.2	–	10	3 Min.; 4.5 Typ.								
Inputs High, V_{NH} All Types	1.4	–	5	1.5 Min.; 2.25 Typ.								
	2.8	–	10	3 Min.; 4.5 Typ.								
Inputs Low, V_{NL} CD4049A	3.6	–	5	1 Min.; 1.5 Typ.								
	7.2	–	10	2 Min.; 3 Typ.								
Noise Margin: Inputs Low, V_{NML} Min. CD4050A	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH} Min. CD4050A	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current: N-Channel (Sink), I_DN Min.	0.4	–	4.5	3.3	5.2	2.6	1.8	3.1	5.2	2.6	2.1	mA
	0.4	–	5	3.75	6	3	2.1	3.6	6	3	2.5	
	0.5	–	10	10	16	8	5.6	9.6	16	8	6.6	
P-Channel (Source), I_DP Min.	4.5	–	5	−0.62	−1	−0.5	−0.35	−0.6	−1	−0.5	−0.4	
	2.5	–	5	−1.85	−2.5	−1.25	−0.9	−1.5	−2.5	−1.25	−1	
	9.5	–	10	−1.85	−2.5	−1.25	−0.9	−1.5	−2.5	−1.25	−1	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H ..... −55 to +125°C

PACKAGE TYPE E ..... −40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{CC})

(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

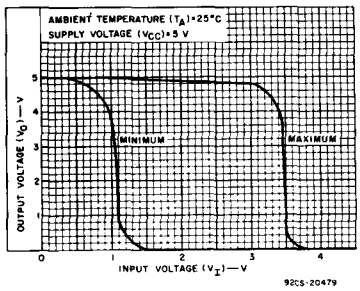


Fig. 2—Minimum and maximum voltage transfer characteristics for CD4049A.

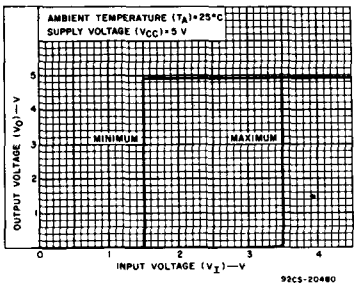


Fig. 3—Minimum and maximum voltage transfer characteristics for CD4050A.

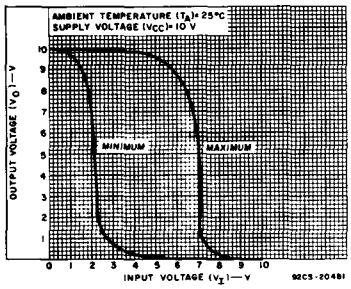


Fig. 4—Minimum and maximum voltage transfer characteristics for CD4049A.

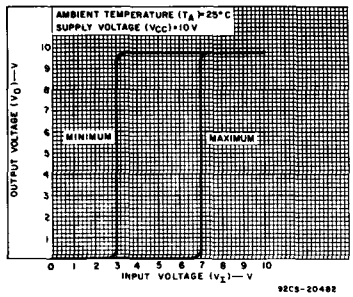


Fig. 5—Minimum and maximum voltage transfer characteristics for CD4050A.

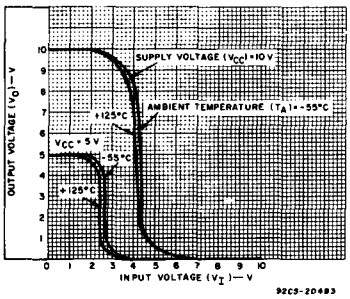


Fig. 6—Typical voltage transfer characteristics as a function of temperature for CD4049A.

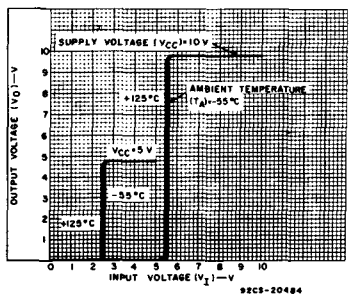


Fig. 7—Typical voltage transfer characteristics as a function of temperature for CD4050A.

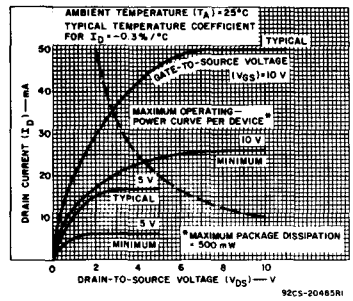


Fig. 8—Typical and minimum n-channel drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

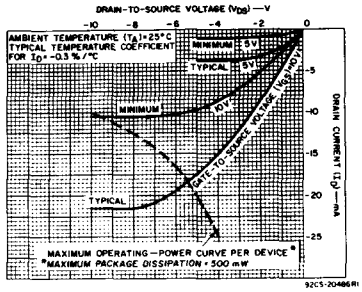


Fig. 9—Typical and minimum p-channel drain characteristics as a function of gate-to-source voltage (V_{GS}) for CD4049A, CD4050A.

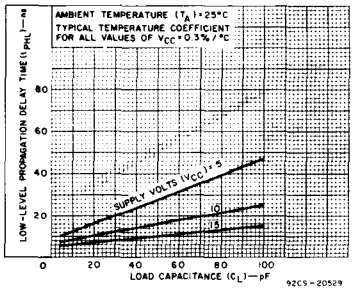


Fig. 10—Typical high-to-low level propagation delay time vs. C_L for CD4049A.

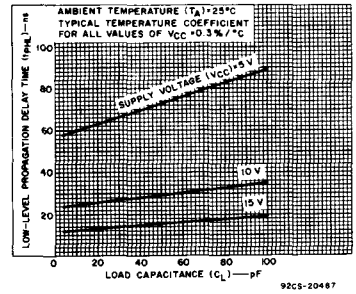


Fig. 11—Typical high-to-low level propagation delay time vs. C_L for CD4050A.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A=25°C; Input t_r,t_f=20 ns, C_L=15 pF, R_L=200 kΩ

CHARACTERISTIC	CONDITIONS		LIMITS ALL PKGS.		UNITS
	V_I	V_{CC}	Typ.	Max.	
Propagation Delay Time:					
Low-to-High, t_{PLH}					
CD4049A	5	5	50	80	ns
	10	10	25	55	
CD4050A	5	5	75	140	
	10	10	35	85	
High-to-Low, t_{PHL}					
CD4049A	5	5	15	55	ns
	10	10	10	30	
CD4050A	5	5	55	110	
	10	10	25	55	
Transition Time:					
Low-to-High, t_{TLH}	5	5	50	100	ns
	10	10	30	60	
High-to-Low, t_{THL}	5	5	20	45	
	10	10	16	40	
Input Capacitance, C_I					
CD4049A	–	–	15	–	pF
CD4050A	–	–	5	–	

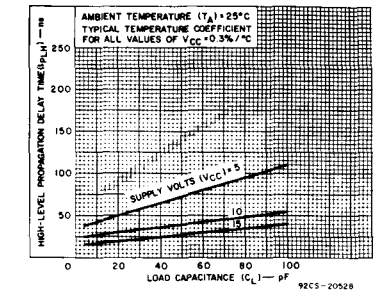


Fig. 12—Typical low-to-high level propagation delay time vs. C_L for CD4049A.

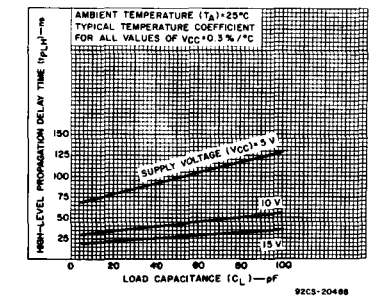


Fig. 13—Typical low-to-high level propagation delay time vs. C_L for CD4050A.

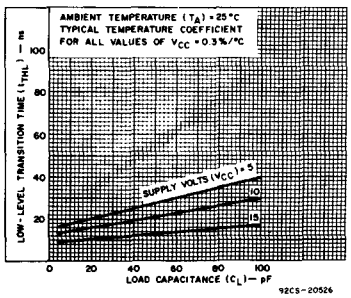


Fig. 14—Typical high-to-low level transition time vs. C_L for CD4049A, CD4050A.

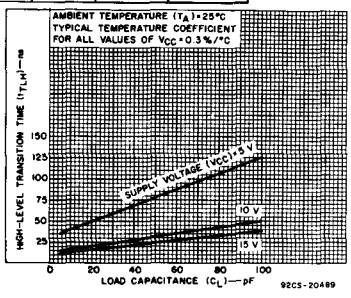


Fig. 15—Typical low-to-high level transition time vs. C_L for CD4049A, CD4050A.

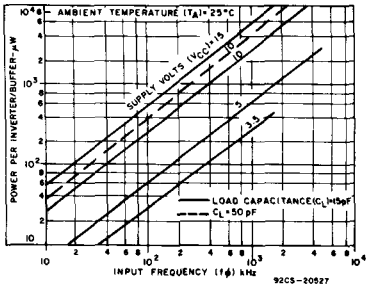


Fig. 16—Typical dissipation characteristics for CD4049A, CD4050A.

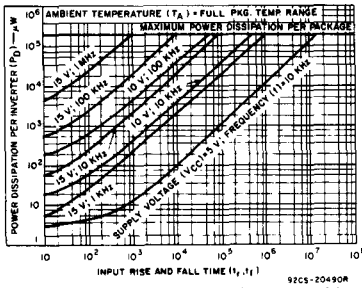


Fig. 17—Typical power dissipation vs. transition time per inverter CD4049A.

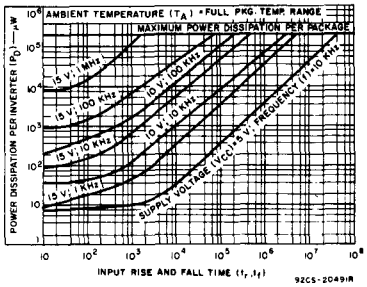


Fig. 18—Typical power dissipation vs. transition time per inverter CD4050A.

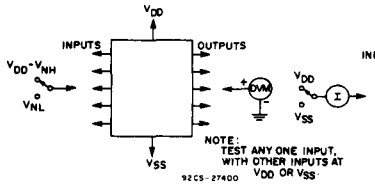


Fig. 19—Noise immunity test circuit.

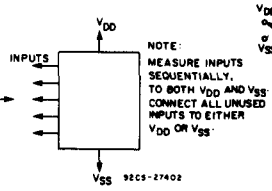


Fig. 20—Input leakage current test circuit.

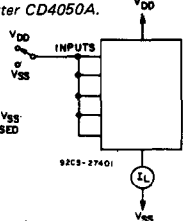


Fig. 21—Quiescent device current test circuit.

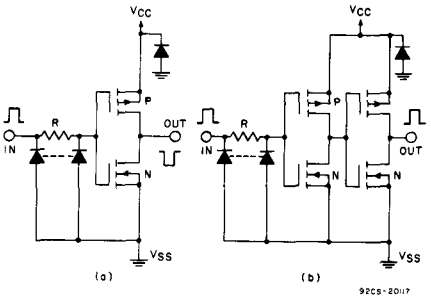


Fig. 22 – (a)Schematic diagram of CD4049A, 1 of 6 identical units.
(b) Schematic diagram of CD4050A, 1 of 6 identical units.

CMOS LSI 4-Bit Arithmetic Logic Unit

The RCA-CD4057A is a low-power arithmetic logic unit (ALU) designed for use in LSI computers. An arithmetic system of virtually any size can be constructed by wiring together a number of CD4057A ALU's. The CD4057A provides 4-bit arithmetic operations, time sharing of data terminals, and full functional decoding for all control lines. The distributed control system of this device provides great flexibility in system designs by allowing hard-wired connection of N units in 4^N unique combinations. Four control lines provide 16 instructions which include Addition, Subtraction, Bidirectional and Cycle Shifts, Up-Down Counting, AND, OR, and Exclusive-OR logic operations.

Two mode control lines allow the CD4057A to function as any 4-bit section of a larger arithmetic unit by controlling the bidirectional serial transfer of data to adjacent arithmetic arrays. By means of three "Conditional Control" lines Overflow, All Zeros, and Negative State conditions may be detected and used to establish a conditional operation. Predetermined operation of the CD4057A on a conditional basis allows greater ALU flexibility. Although especially applicable as a parallel arithmetic unit, the CD4057A also finds use in virtually any application requiring one or more of its 16 basic instructions. The CD4057A is supplied in a hermetically sealed 28-lead dual-in-line ceramic package (CD4057AD), 28-lead ceramic flat package (CD4057AK), and in chip form (CD4057AH).

Applications:

- **Parallel Arithmetic Units**
- **Process Controllers**
- **Remote Data Sets**
- **Graphic Display Terminals**

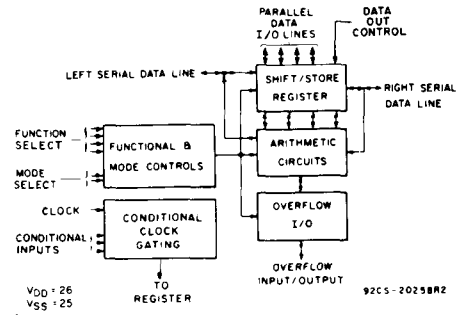


Fig. 1 – Block diagram – CD4057A.

Features:

- **LSI Complexity on a Single Chip**
- **16-Instruction Capability**
  - **-Add, Subtract, Count**
  - **-AND, OR, Exclusive-OR**
  - **-Right, Left, or Cyclic Shifts**
- **Bidirectional Data Busses**
- **Instruction Decoding on Chip**
- **Fully Static Operation**
- **Single-Phase Clocking**
- **Easily Expandable to 8, 12, 16,. . . . Bit Operation**
- **Low Quiescent Device Dissipation . . . . . 10 μW (typ.)**
- **Conditional-Operation Controls on Chip**
- **Add Time (Data In-To Sum Out) =375 ns (typ) at 10V**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	−65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, K, H	−55 to +125°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −55 to +100°C (PACKAGE TYPES D, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	V
Setup Time, t_S DATA	5	40	–	ns
	10	20	–	
OP CODE	5	4590	–	
	10	1320	–	
Clock Pulse Width, t_W	5	1200	–	ns
	10	375	–	
Clock Input Frequency, f_{CL} Count Mode	5	0.13	–	MHz
	10	0.46	–	
Shift Mode	5	0.33	–	
	10	1.4	–	
Clock Rise or Fall Time, t_rCL, t_fCL	5	–	15	μs
	10	–	15	

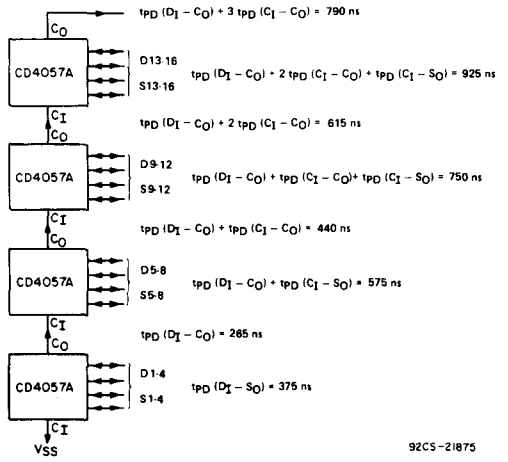


Fig. 2 – Typical speed characteristics of a 16-bit ALU at V_{DD} = 10 V.

CD4057A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			Limits at Indicated Temperatures (°C)							UNITS
				CD4057AD, CD4057AK, CD4057AH							
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55°C		25°C			125°C		
				Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
Quiescent Device Current I_L	–	–	5	–	5	–	0.5	5	–	150	μA
	–	–	10	–	10	–	1	10	–	300	
	–	–	15	–	50	–	1	50	–	2000	
Output Voltage; Low-Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.							V
	–	10	10	0 Typ.; 0.05 Max.							
High Level, V_{OH}	–	0	5	4.95 Min.; 5 Typ.							V
	–	0	10	9.95 Min.; 10 Typ.							
Noise Immunity (All Inputs) V_{NL}, V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.							V
	1	–	10	3 Min.; 4.5 Typ.							
	4.2	–	5	1.5 Min.; 2.25 Typ.							
	9	–	10	3 Min.; 4.5 Typ.							
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.							V
	9	–	10	1 Min.							
Inputs High, V_{NMH}	0.5	–	5	1 Min.							
	1	–	10	1 Min.							
Output Drive Current: I_DN, I_DP Zero Indicator	0.5	–	5	0.11	–	0.09	0.16	–	0.06	–	mA
n-channel	0.5	–	10	0.12	–	0.10	0.16	–	0.07	–	
p-channel	3	–	5	0.04	–	0.03	0.06	–	0.02	–	
	7	–	10	0.08	–	0.07	0.13	–	0.05	–	
Negative Indicator	0.5	–	5	0.11	–	0.09	0.30	–	0.06	–	
n-channel	0.5	–	10	0.12	–	0.10	0.40	–	0.07	–	
p-channel	4.5	–	5	0.07	–	0.06	0.19	–	0.04	–	
	9.5	–	10	0.12	–	0.10	0.30	–	0.07	–	
Overflow Indicator	0.5	–	5	0.25	–	0.20	0.50	–	0.14	–	
n-channel	0.5	–	10	0.37	–	0.30	0.90	–	0.21	–	
p-channel	4.5	–	5	0.08	–	0.07	0.21	–	0.05	–	
	9.5	–	10	0.12	–	0.10	0.38	–	0.07	–	
All Other Outputs	0.5	–	5	0.11	–	0.09	0.10	–	0.06	–	
n-channel	0.5	–	10	0.06	–	0.05	0.12	–	0.03	–	
p-channel	4.5	–	5	0.02	–	0.02	0.05	–	0.01	–	
	9.5	–	10	0.06	–	0.05	0.08	–	0.03	–	
Input Leakage Current I_{IL}, I_{IH}	Any Input –	–	15	$\pm 10^{-5}$ Typ., ± 1 Max.							μA

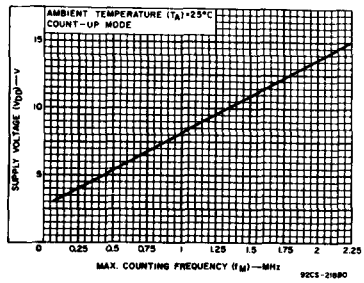


Fig. 3 — Maximum counting frequency vs. supply voltage for a typical CD4057A.

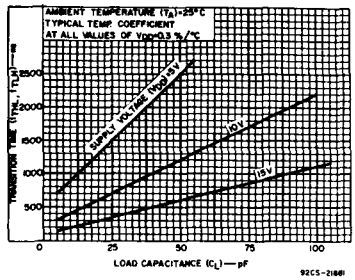


Fig. 4 — Transition time vs. load capacitance for data outputs (D1-D4).

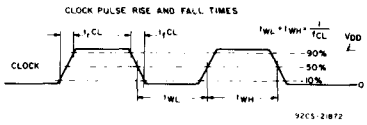


Fig. 5 — Clock pulse rise and fall times.

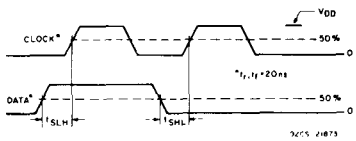


Fig. 6 — Data setup time.

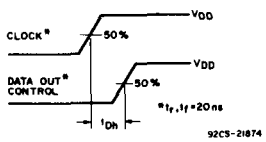


Fig. 7 — Data hold time.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ and $C_L = 15$ pF, $R_L = 200$ kΩ, $t_r, t_f = 20$ ns

Typical Temperature Coefficient at all values of $V_{DD} = 0.3\%/°C$

CHARACTERISTICS	TEST CONDITIONS	LIMITS CD4057AD, CD4057AK			UNITS
	V_{DD}	Min.	Typ.	Max.	
Propagation Delay Time: t_{PLH}, t_{PHL} DATA IN-to-SUM OUT	5	–	1430	3900	ns
	10	–	375	720	
CARRY IN-to-SUM OUT	5	–	915	2550	
	10	–	310	840	
DATA IN-to-CARRY OUT	5	–	950	2580	
	10	–	265	720	
CARRY IN-to-CARRY OUT	5	–	485	1320	
	10	–	175	480	
ZI Input -to- ZI Output	5	–	1980	5400	
	10	–	750	2040	
	5	–	265	720	
	10	–	110	300	
Transition Time: t_{TLH}, t_{THL} ZI Output	5	–	3700	10350	ns
	10	–	1650	4500	
	5	–	420	1140	
	10	–	220	600	
Negative Indicator and Overflow Indicator	5	–	300	825	
	10	–	165	450	
All Other Outputs	5	–	1000	2775	
	10	–	475	1275	
Minimum Clock Pulse Width, t_W	5	–	400	1200	ns
	10	–	125	375	
Clock Rise and Fall Time, t_rCL, t_fCL	5	–	–	15	μs
	10	–	–	15	
Minimum Set Up Time : t_{SLH}, t_{SHL} DATA	5	–	20	40	ns
	10	–	10	20	
OP CODE	5	–	1675	4590	ns
	10	–	485	1320	
Minimum Data Hold Time, t_{HLH}, t_{HHL}	5	–	20	40	ns
	10	–	10	20	
Maximum Clock Frequency: f_{CL} Count Mode	5	0.13	0.36	–	MHz
	10	0.46	1.35	–	
Shift Mode	5	0.33	0.90	–	
	10	1.4	3.8	–	
Input Capacitance, C_I	ANY INPUT	–	5	–	pF

LOGIC DESCRIPTION

OPERATIONAL MODES

The CD4057A arithmetic logic unit operates in one of four possible modes. These modes control the transfer of information, either serial data or arithmetic operation carries, to and from the serial-data lines. Fig. 8 shows the manner in which the four modes control the data on the serial-data lines.

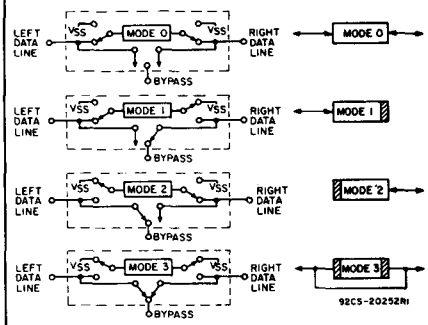


Fig. 8 – Schematic of "Mode" concept.

In MODE 0, data can enter or leave from either the left or the right serial-data line.

In MODE 1, data can enter or leave only on the left serial-data line.

In MODE 2, data can enter or leave only on the right serial-data line.

In MODE 3, serial data can neither enter nor leave the register, regardless of the nature of the operation. Furthermore, the register is by-passed electrically, i.e., there is an electrical bidirectional path between the right and left serial data terminals.

The two input lines labeled C1 and C2 in the terminal assignment diagram define one of four possible modes shown in Table I. Through the use of mode control, individual arithmetic arrays can be cascaded to form one large processor or many processors of various lengths.

TABLE I – MODE DEFINITION

C2	C1	MODE
0	0	0
0	1	1
1	0	2
1	1	3

Examples of how one " hard-wired " combination of three ALU's can form (a) a 12-bit parallel processor, (b) one 8-bit and one 4-bit parallel processor, or (c) three 4-bit parallel processors, merely by changes in the modes of each ALU are shown in Fig. 10.

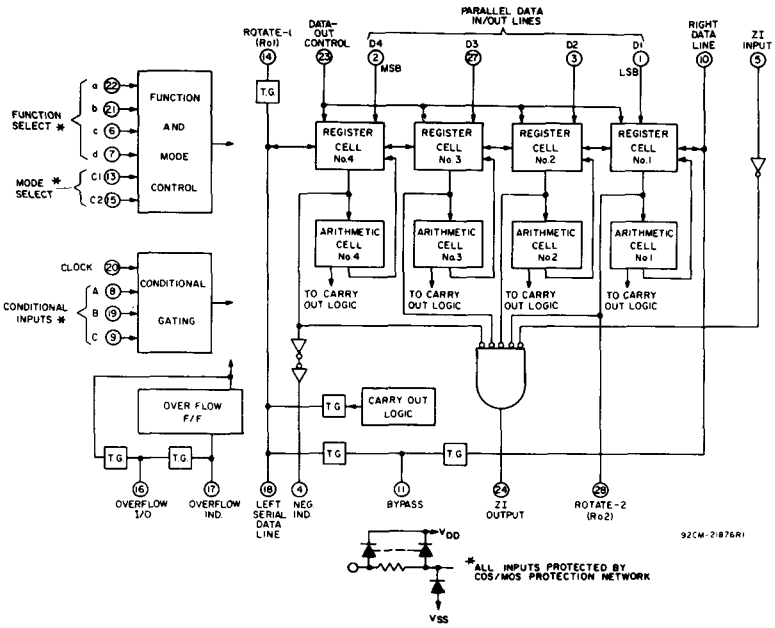


Fig. 9 – Simplified logic diagram.

Data-flow interruptions are shown by shaded areas. With these three ALU's and the four available modes, 61 more system combinations can be formed. If 4 ALU's are used, 4^4 combinations (256) are possible. *Fig. 11* shows a diagram of 4 CD4057A's interconnected to form a 16-bit parallel processor.

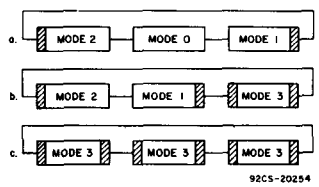


Fig. 10 – "Mode" connections for parallel processor:
(a) 12-bit unit,
(b) one 8-bit and one 4-bit unit
(c) three 4-bit units.

NOTE: The BYPASS terminal of the "most significant" CD4057A is connected to the bypass terminal of the "least significant" CD4057A. The bypass terminals on all other CD4057A's are left floating. This interconnection is performed whenever more than one CD4057A are used to form a processor.

INSTRUCTION REPERTOIRE

Four encoded lines are used to represent 16 instructions. Encoded instructions are as follows:

a	b	c	d	
0	0	0	0	NO-OP (Operational Inhibit)
0	0	0	1	AND
0	0	1	0	Count down
0	0	1	1	Count up
0	1	0	0	Subtract Stored number from zero (SMZ)
0	1	0	1	Subtract from parallel data lines (SM) (stored number from parallel data lines)
0	1	1	0	Add (AD)
0	1	1	1	Subtract (SUB) (Parallel data lines from stored number)
1	0	0	0	Set to all ones (SET)
1	0	0	1	Clear to all zeroes (CLEAR)
1	0	1	0	Exclusive-OR
1	0	1	1	OR
1	1	0	0	Input Data (From parallel data lines)
1	1	0	1	Left shift
1	1	1	0	Right shift
1	1	1	1	Rotate (cycle) right

All instructions are executed on the positive edge of the clock.

PARALLEL COMMANDS

a. **CLEAR** – sets register to zero.
b. **SET** –sets register to all ones.
c. **OR** –processes contents of register with value on parallel-data lines in a logical OR function.
d. **AND** –processes contents of register with value on parallel-data lines in a logical AND function.
e. **Exclusive-OR** – processes contents of register with data on parallel-data lines in a logical Exclusive-OR function.
f. **IN** –loads data on parallel-data lines into register.
g. **DATA OUT CONTROL** – unloads contents of register and overflow flip-flop onto parallel data lines and overflow I/O independent of all other controls.
h. **SUB:**
   In Mode 0, adds to the contents of the register the one's complement of the data on the parallel-data lines. Carries can enter on the right serial data line and can leave on the left serial data line. The overflow indicator does not change state.
   In Mode 1, adds to the contents of the register the two's complement of the data on the parallel-data lines. Generated carries can leave on the left serial line. The CARRY IN is set to zero. The overflow indicator does not change state.
   In Mode 2, same as Mode 0, except carries cannot leave on the right serial-data line.The absence or presence of an overflow is registered.
   In Mode 3, same as Mode 1, except carries cannot leave on the left serial-date line. The absence or presence of an overflow is registered.
i. **COUNT UP:**
   In Mode 0, adds to the contents of the register the data on the right serial-data line and permits any resulting carry to leave on the left serial-data line. No data enters the parallel-data lines.
   In Mode 1, internally adds a one to the contents of the register and permits any resulting carry to leave on the left serial-data line. No data enters or leaves the right serial-data line.
   In Mode 2, adds to the contents of the register the data on the right serial-data line. No data enters or leaves the left serial-data line.
   In Mode 3, internally adds a one to the contents of the register No data enters or leaves the register on any serial-data or parallel-data line.
   In all modes, with the DATA OUT control high

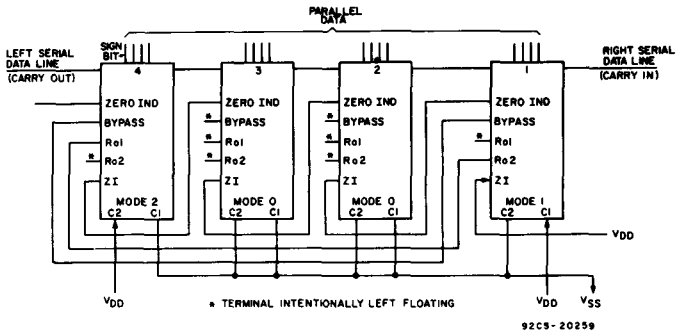


Fig. 11 — Connection for 16-bit arithmetic logic unit.

the count is presented on the parallel data lines (D1-D4).

j. COUNT DOWN:

In Mode 0, subtracts a one (2's complement form) from the contents of the register and adds to this result the data on the right serial-data line and permits any resulting carry to leave on the left serial-data line. No data enters on the parallel-data lines.

In Mode 1, internally subtracts a one from the contents of the register and permits any resulting carry to leave on the left serial-data line. No data enters or leaves the right serial-data line.

In Mode 2, subtracts a one from the contents of the register and adds to this result the data on the right serial-data line. No data enters or leaves on the left serial-data line.

In Mode 3, internally subtracts a one from the contents of the register. No data enters or leaves on the serial-data lines.

In all modes, with the DATA OUT control high the count is presented on the parallel data lines (D1-D4).

k. ADD(AD):

In Mode 0, adds the contents of the register to the data on the parallel-data lines and the right serial-data line. Any resulting carry can leave on the left serial-data line. The overflow indicator does not change state.

In Mode 1, adds the contents of the register to the data on the parallel-data lines and allows any resulting carry to leave on the left serial-data line. The right serial-data line is open-circuited. The overflow indicator does not change state. The CARRY-IN is set to zero.

In Mode 2, adds the contents of the register to the data on the parallel data lines and the right serial-data line. Any overflow sets the overflow indicator. The left serial-data line is open-circuited. The absence or presence of an overflow is registered.

In Mode 3, adds contents of the register to the data on the parallel-data lines. Any resulting carry sets the overflow indicator. The two serial-data lines are open circuited. The absence or presence of an overflow is registered. The CARRY-IN is set to zero.

l. SM — same operation as AD except the contents of the register are two's complemented during addition in Mode 1 and Mode 3. In Mode 0 or Mode 2, the contents of the register are one's complemented and added to the data on the right serial-data line and the parallel-data lines. Overflows occurring in Mode 1 or Mode 0 do not alter the overflow indicator. The presence or absence of overflows is registered on the overflow indicator in Mode 2 or Mode 3.

m. SMZ:

In Mode 0, one's complements the contents of the register and adds the data on the right serial-data line to the contents of the register. Any resulting carry can leave on the left serial-data line. The overflow indicator does not change state.

In Mode 1, two's complements the contents of the register and permits any carry to leave on the left serial-data line. No data can enter the right serial-data line. The overflow indicator does not change state. The CARRY-IN is set to zero.

In Mode 2, one's complements the contents of the register and adds the data on the right serial-data line to the contents of the register. Carries cannot leave the left serial data line. The absence or presence of an overflow alters the overflow indicator.

In Mode 3, two's complements the contents of the register. Serial data can neither enter the right serial-data line nor leave the left serial-data line. The overflow indicator is at zero. The CARRY-IN is set to zero.

n. NO-OP — no operation takes place, The clock input is inhibited and the state of all registers and indicators remains unchanged.

SERIAL-SHIFT OPERATIONS

a. ROTATE (cycle) RIGHT — This operation is internal. The contents of the register shift to the right, cyclic fashion with the leftmost stage accepting data from the rightmost stage regardless of the mode. Data can leave the register serially on the right data line only while the register is in Mode 1 or Mode 0. Data can enter the left data line serially while the register is in Mode 1 or Mode 0. The Ro1 terminal of the "Most Significant" CD4057A must be connected to the Ro2 terminal of the "Least Significant" CD4057A. All other Ro1 and Ro2 terminals must be left floating. When only one CD4057A is used, Ro1 must be connected to Ro2.

b. RIGHT SHIFT — The contents of the register shift to the right and serial operations are as follows:

In Mode 0, data can enter serially on the left data line, shift through the register, and leave on the right data line.

In Mode 1, data can enter serially on the left data line. The right data line effectively is open - circuited.

In Mode 2, data can leave serially on the right data line. The left data line effectively is open-circuited. Vacant spaces are filled with zeros.

In Mode 3, serial data can neither enter nor leave the register; however, the contents shift to the right and vacated places are filled with zeros.

In all modes, with the DATA OUT control high the data is presented on the parallel data lines (D1-D4).

c. **LEFT SHIFT** – The contents of the register shift to the left and serial operations are as follows;

In Mode 0, data can enter the right data line, shift through the register, and leave on the left data line.

In Mode 1, data can leave serially on the left data line. The right data line effectively is open-circuited. All vacant positions are filled with zeros.

In Mode 2, data can enter serially on the right data line. The left data line effectively is open-circuited.

In Mode 3, data can neither enter nor leave the register; however, the contents shift to the left, and vacated places are filled with zeros.

In all modes, with the DATA OUT control high the data is presented on the parallel data lines (D1-D4).

Because the "DATA OUT" control instruction is independent of the other 16 instructions, care must be taken not to activate this control when data are to be loaded into the processor. This instruction should only be activated when the processor is executing a NO-OP, any SHIFT, SMZ, COUNT UP or DOWN, CLEAR, or SET.

If a data line, serial or parallel, is used as an input and the logic state of that line is not defined (i.e., the line is an open circuit),then the result of any operation using that line is undefined.

OPERATIONAL SEQUENCE FOR ARITHMETIC ADD CYCLE

1. Apply IN Instruction and Word A on Parallel Data Lines (D1–D4).
2. Apply CLOCK to load Word A into the register.
3. Apply OP CODE Instruction and Word B on Data Lines.
4. Apply CLOCK to load resulting function of A and B into the register.
5. Apply "DATA OUT" control to present result to Parallel Data Lines.

NOTE: Transitions of Step 2 and Step 3 may occur almost simultaneously; i.e. separated by only one data-hold time.

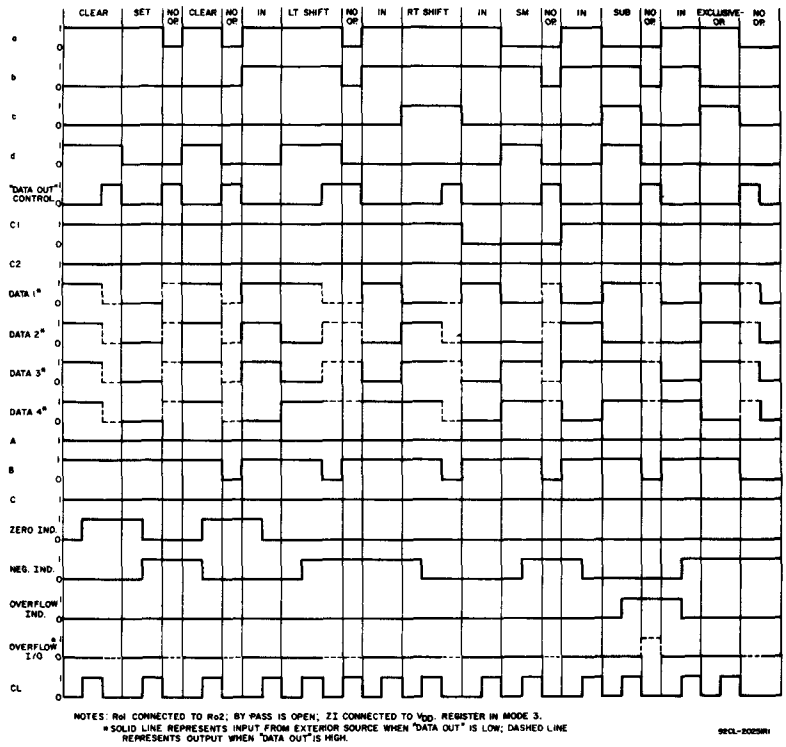


Fig. 12 – Timing diagram.

NEGATIVE-NUMBER DETECTION

The NEG IND terminal of the CD4057A is connected to the output of the flip-flop that is in the most significant bit position. A "1" on the NEG IND terminal indicates a negative number is in the register. This detection is also independent of modes.

ZERO DETECTION

The condition of "all zeros" is indicated by a "1" on the Zero Indicator terminal of the "Most Significant" CD4057A. As shown in Fig. 11, terminal ZI of the CD4057A containing the least significant set of bits is connected to V_{DD}. Zero indication is independent of modes.

COMPLEMENTING NUMBERS

1. One's complement of number in ALU register.
   a) ALU must be in MODE 0 or MODE 2.
   b) Zero on Rt. Data Line.
   c) Execute an SMZ instruction.

(Continued)

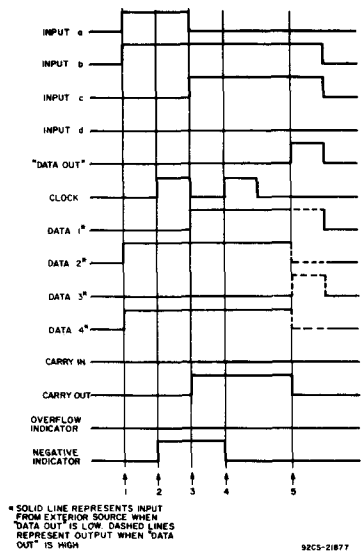
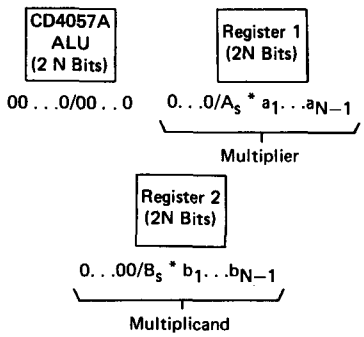


Fig. 13 – Add cycle waveforms.

2. One's complement of number to be loaded into ALU register.
   a) If zero indicator output is low, execute a CLEAR instruction, and make Rt. Data Line = 0.
   b) ALU must be in MODE 0 or MODE 2.
   c) Execute an SUB instruction.
3. Two's complement of number in ALU register.
   a) ALU must be in MODE 1 or MODE 3.
   b) Execute an SMZ instruction.
4. Two's complement of number to be loaded into ALU register.
   a) If zero indicator output is low, execute a CLEAR instruction, and make Rt. Data Line = 0.
   b) ALU must be in MODE 1 or MODE 3.
   c) Execute an SUB instruction.

The following algorithms are given as a general guideline to demonstrate some of the capabilities of the CD4057A.

MULTIPLICATION OF TWO N-BIT NUMBERS

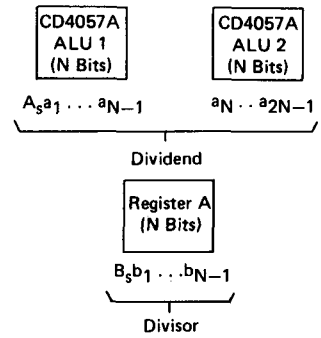


*A_s and B_s are sign bits

Multiplication Algorithm

1. Clear ALU to Zero
2. Store $A_s \oplus B_s$ in External Flip-Flop.
3. If A_s = 1, Complement Register 1.
4. If B_s = 1, Complement Register 2.
5. Load Register 2 into ALU.
6. Do shift Left on ALU N Times (N = *number of bits*).
7. Do N Times:
   (1)
   a) If MSB of ALU = 1 (Negative Indicator = High), Then shift ALU left 1 bit; add Register 1 to ALU.
   b) If MSB of ALU = 0 (Negative Indicator = Low) Then shift ALU left 1 bit.
8. If $A_s \oplus B_s$ = 1, then Complement ALU.
9. Answer in ALU.

Division Algorithm



1. Store $A_s \oplus B_s$ in External Flip-Flop.
2. If A_s = 1, complement ALU 1 and ALU 2.
3. If B_s = 1, complement Register A.
4. Check for Divisor = 0
   a) If Divisor = 0; stop, indicates division by 0.
   b) If Divisor ≠ 0; continue.
5. Apply SUB instruction to ALU 1 and the contents of Register A to ALU 1 data lines.
6. Put a zero on RT data line of ALU 2 and shift ALU 1 & ALU 2 left 1 bit.
7. Do "N" times.
   (1) Apply a sub instruction to ALU 1 and the contents of Register A to the ALU 1 data lines.
   a) If C_O = 1, then clock ALU 1, and put a 1 on right data line of ALU 2.
   b) If C_O = 0, then do not clock, and put a 0 on right data line of ALU 2.
   (2) Shift left 1 bit.
8. If sign Flip Flop = 1, complement ALU 2.
9. Answer in ALU 2.

CONDITIONAL OPERATION

Inhibition of the clock pulse can be accomplished with a programmed NO-OP instruction or through conditional input terminals A,B,and C.In a system of many CD4057A's, each CD4057A can be made to automatically control its own operation or the operation of any other CD4057A in the system in conjunction with the Overflow, Zero, or Negative (Number) indicators. Table II, the conditional inputs, truth table, defines the interactions among A,B, and C.

TABLE II – CONDITIONAL-INPUTS TRUTH TABLE

A	B	C	OPERATION PERMITTED
0	X	X	Yes
1	0	0	Yes
1	0	1	No
1	1	0	No
1	1	1	Yes

X = don't care

Two examples of how the conditional operation can be used are as follows:

1) For the Multiplication Algorithm
   A = 1, for step 7 (1)
   A = 0, for step 7 (2)
   B = 1
   C = negative Indicator
2) For the Division Algorithm
   A = 1, for step 7 (1)
   A = 0, for step 7 (2)
   B = 1
   C = C_O (left data line)

OVERFLOW DETECTION

The CD4057A is capable of detecting and indicating the presence or absence of an arithmetic two's-complement overflow. A two's-complement overflow is defined as having occurred if the signs of the two initial words are the same and the sign of the result is different while performing a carry-generating instruction.

For example:
0.011
(+) 0.110
1.001

Overflows can be detected and indicated only during operation in Mode 2 or Mode 3 and can occur for only four instructions (AD, SMZ, SM, and SUB). If an overflow is detected and stored in the overflow flip-flop, any one of the five instructions AD, SMZ, SM, SUB, or IN can change the overflow indicator.

When any of the three subtraction instructions is used, the sign bit of the data being subtracted is complemented and this value is used as one of the two initial signs to detect overflows. If an overflow has occurred, the final sign of the sum or difference is one's complemented and stored in the most-significant-bit position of the register.

The overflow flip-flop is updated at the same time the new result is stored in the CD4057A. Whenever data on the parallel-data lines are loaded into the CD4057A, whatever is on the Overflow I/O line is loaded into the overflow flip-flop. Also, whenever data are dumped on the parallel data lines from the CD4057A, the contents of the overflow flip-flop are dumped on the Overflow I/O line. Thus overflows may be stored elsewhere and then fed into the CD4057A at another time.

OPERATIONAL SEQUENCE AND WAVEFORMS FOR PROPAGATION-DELAY MEASUREMENTS

1. DATA-IN-to-CARRY OUT and DATA IN-to-SUM OUT
   - A. Apply Word A and IN instruction
   - B. Apply Clock to load word A into register
   - C. Apply AD instruction
   - D. Apply Word B (data in)
   - E. Apply Clock to load result (sum out)
   - F. Apply DATA OUT CONTROL to look at result

2. CARRY IN-to-CARRY OUT and CARRY IN-to-SUM OUT
   - A. Apply Word A and IN instruction
   - B. Apply Clock to load word A into register
   - C. Apply AD instruction
   - D. Apply Word B
   - E. Apply CARRY IN (carry in)
   - F. Apply Clock to load result (sum out)
   - G. Apply DATA OUT CONTROL to look at result

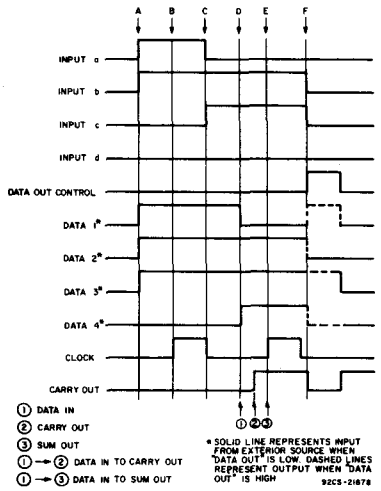


Fig. 14(a) – DATA IN-to-CARRY OUT and DATA IN-to-SUM OUT.

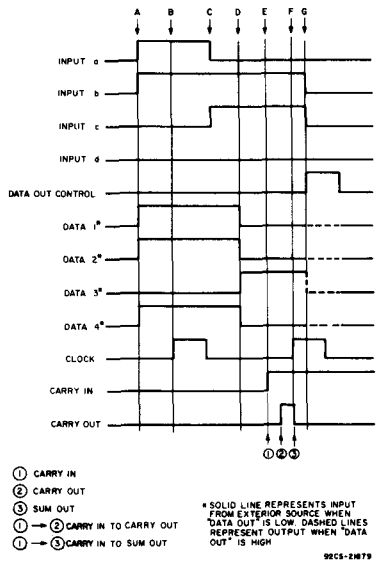


Fig. 14(b) – CARRY IN-to-CARRY OUT and CARRY IN-to-SUM OUT.

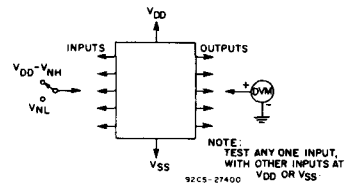


Fig. 15 – Noise-immunity test circuit.

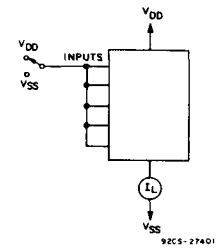


Fig. 16 – Quiescent-device-current test circuit

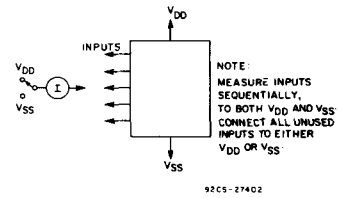


Fig. 17 – Input-leakage-current test circuit.

TYPICAL APPLICATION

The CD4057A has been designed for use as a parallel processor in flexible, programmable, easily expandable, special or general purpose computers, where minimization of external connections and data busing are primary design goals. The block diagram of Fig. 18 is an example of a computer that processes 8 bits in parallel.

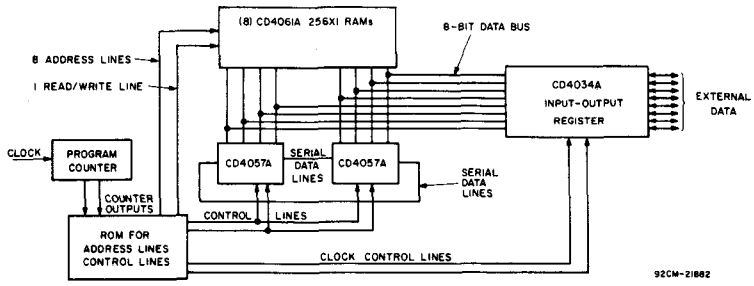


Fig. 18 – Example of computer organization using CD4057A.

CMOS Programmable Divide-by-"N" Counter

Standard "A"-Series Types (3-to-15-Volt Rating)

RCA-CD4059 standard "A"-Series types are divide-by-N down-counters that can be programmed to divide an input frequency by any number "N" from 3 to 15,999. The output signal is a pulse one clock-cycle wide occurring at a rate equal to the input frequency divided by N. This single output has TTL drive capability. The down-counter is preset by means of 16 jam inputs.

The three Mode-Select Inputs Ka, Kb, and Kc determine the modulus ("divide-by" number) of the first and last counting sections in accordance with the truth table shown in Table I. Every time the first (fastest) counting section goes through one cycle, it reduces by 1 the number that has been preset (jammed) into the three decades of the intermediate counting section and into the last counting section, which consists of flip-flops that are not needed for operating the first counting section. For example, in the ÷ 2 mode, only one flip-flop is needed in the first counting section. Therefore the last counting section has three flip-flops that can be preset to a maximum count of seven with a place value of thousands. If ÷ 10 is desired for the first section, Ka is set to 1, Kb to 1, and Kc to 0. Jam Inputs J1, J2, J3, and J4 are used to preset the first counting section and there is no last counting section. The intermediate counting section consists of three cascaded BCD decade (÷ 10) counters presettable by means of Jam Inputs J5 through J16.

The Mode-Select Inputs permit frequency-synthesizer channel separations of 10, 12.5, 20, 25, or 50 parts. These inputs set the maximum value of N at 9999 (when the first counting section divides by 5 or 10) or 15,999 (when the first counting section divides by 8, 4, or 2).

The three decades of the intermediate counting section can be preset to a binary 15 instead of a binary 9, while their place values are still 1, 10, and 100, multiplied by the number of the ÷ N mode. For example, in the ÷ 8 mode, the number from which counting-down begins can be preset to:

3rd decade:	1500
2nd decade:	150
1st decade:	15
Last counting section	1000

The total of these numbers (2665) times 8 equals 21,320. The first counting section can be preset to 7. Therefore, 21,327 is the maximum possible count in the ÷ 8 mode.

The highest count of the various modes is shown in the column entitled Extended Counter Range of Table 1. Control inputs Kb and Kc can be used to initiate and lock the counter in the "master preset" state. In this condition the flip-flops in the counter are preset in accordance with the jam inputs and the counter remains in that state as long as Kb and Kc both remain low. The counter begins to count down from the preset state when a counting mode other than the master preset mode is selected.

The counter should always be put in the *master preset mode before the ÷5 mode is* selected.

Whenever the master preset mode is used, control signals Kb=0 and Kc=0 must be applied for at least 3 full clock pulses.

After the Master Preset Mode inputs have been changed to one of the ÷ modes, the next positive-going clock transition changes an internal flip-flop so that the countdown can begin at the second positive-going clock transition. Thus, after an MP (Master Preset) mode, there is always one extra count before the output goes high. Fig.1 illustrates a total count of 3 (÷ 8 mode). If the Master Preset mode is started two clock cycles or less before an output pulse, the output pulse will appear at the time due. If the Master Preset Mode is not used the counter jumps back to the "JAM" count when the output pulse appears.

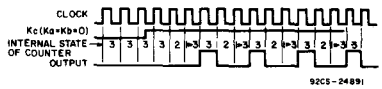
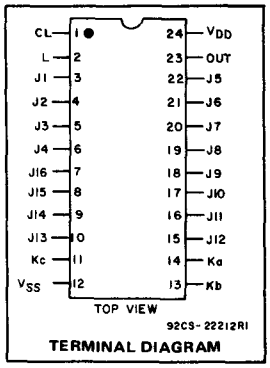


Fig.1 – Total count of 3.

A "1" on the Latch Enable input will cause the counter output to remain high once an output pulse occurs, and to remain in the high state until the latch input returns to "0". If the Latch Enable is "0", the output pulse will remain high for only 1 cycle of the clock-input signal.

As illustrated in the sample applications, this device is particularly advantageous in communication digital frequency synthesis (VHF, UHF, FM, AM, etc.) where programmable divide-by-"N" counters are an integral part of the synthesizer phase-locked-loop subsystem. The CD4059A can also be used to perform the synthesizer "Fixed Divide-by-R" counting function. It is also useful in general-purpose counters for instrumentation functions such as totalizers, production counters, and "time out" timers.



TERMINAL DIAGRAM

Operational and Performance Features:

- **Synchronous Programmable ÷ N Counter: N = 3 to 9999 or 15,999**
- **Presettable down-counter**
- **Fully static operation**
- **Mode-select control of initial decade counting function (÷ 10,8,5,4,2)**
- **T^2L drive capability**
- **Master preset initialization**
- **Latchable ÷ N output**
- **Quiescent current specified to 15 volts**
- **Max. input leakage current of 1 μA at 15 volts, full package-temperature range**
- **1 volt noise margin, full package-temperature range**
- **5-V and 10-V parametric ratings**

Applications

- **Communications digital frequency synthesizers: VHF, UHF, FM, AM, etc.**
- **Fixed or programmable frequency division**
- **"Time out" timer for consumer-application industrial controls**
- ***Companion Application Note*, ICAN-6374, "Application of the CMOS CD4059A Programmable Divide-by-N Counter in FM and Citizens Band Transceiver Digital Tuners"**

The CD4059A series types are available in a 24-lead ceramic dual-in-line package (D and F suffixes), 24-lead dual-in-line plastic package (E suffix), 24-lead ceramic flat package (K suffix), and in chip form (H suffix).

CD4059A Types

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +15 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, K, H) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, K, H) ..... Derate Linearly to 100 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, K, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions V_O (V)	V_{IN} (V)	V_{DD} (V)	Limits *Values at −55°C,+25°C,+125°C Apply to D, K, H, Packages; Values at −40°C,+25°C,+85°C Apply to E Packages* −55°	−40°	+85°	+125°	+25° Min.	+25° Typ.	+25° Max.	Units
Quiescent Device Current, I_L Max.			5	10	10	700	300	–	0.02	10	μA
			10	20	20	200	400	–	0.02	20	
			15	–	–	–	–	–	–	500	
Output Voltage: Low Level, V_{OL} Max.		0,5	5	0.05				–	0	0.05	V
		0,10	10	0.05				–	0	0.05	
High Level, V_{OH} Min.		0,5	5	4.95				4.95	5	–	
		0,10	10	9.95				9.95	10	–	
Noise Immunity: Inputs Low, V_{NL} Min.			5	1.5				1.5	2.25	–	V
			10	3				3	4.5	–	
Inputs High, V_{NH} Min.			5	1.5				1	2.25	–	
			10	3				3	4.5	–	
Noise Margin: Inputs Low, V_{NML} Min.	4.5		5	1							V
	9		10	1							
Inputs High, V_{NMH} Min.	0.5		5	1							
	1		10	1							
Output Drive Current: N-Channel (Sink) I_{DN} Min.	0.4		5	2.5	2.3	1.6	1.4	2	4	–	mA
	0.5		10	5	4.7	3.3	2.8	4	9	–	
P-Channel (Source) I_{DP} Min.	2.5		5	−2	−1.8	−1.3	−1.15	−1.6	−3.2	–	
	4.6		5	−0.5	−0.45	−0.36	−0.3	−0.4	−0.8	–	
	9.5		10	−1.1	−1	−0.75	−0.65	−0.9	−1.8	–	
Input Leakage Current:* I_{IL}, I_{IH} Max.			15	±1					$\pm 10^{-5}$	±1	μA

* Any Input

OPERATING CONDITIONS AT T_A = 25°C (Unless otherwise specified)

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

Characteristic	V_{DD}	Min.	Max.	Units
Supply Voltage Range (over full temp. range)	–	3	12	V
Clock Pulse Width	5	200	–	ns
	10	100	–	
Clock Input Frequency	5	–	1.5	MHz
	10	–	3	
Clock Input Rise and Fall Time	5	–	15	μs
	10	–	5	

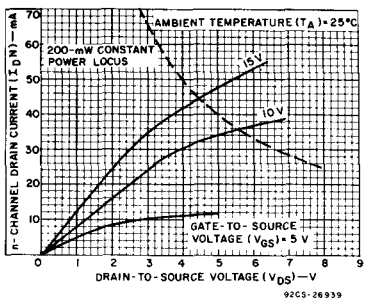


Fig.2 — Minimum output n-channel drain characteristics.

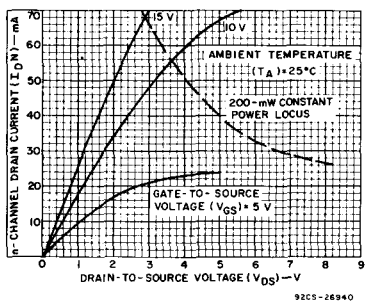


Fig.3 — Typical output n-channel drain characteristics.

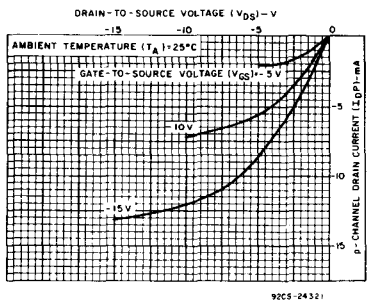
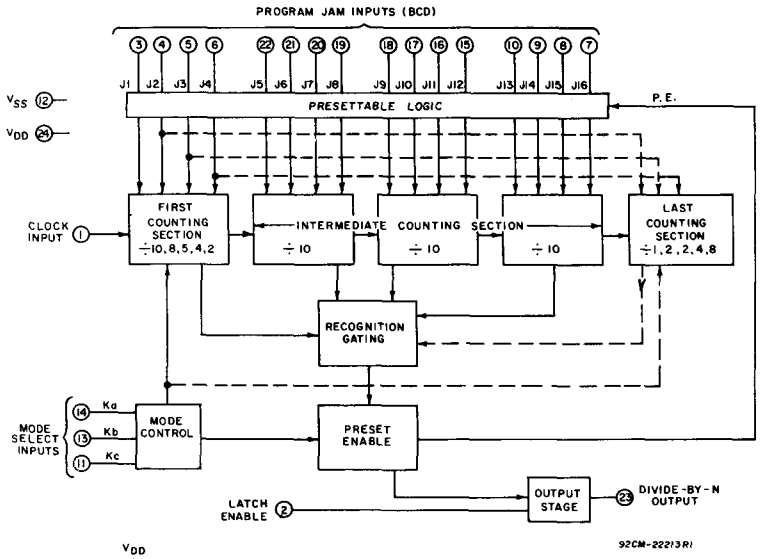
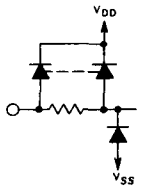


Fig.4 — Minimum output p-channel drain characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS AT $T_A = 25^oC$, $C_L = 50$ pF, Input $t_r, t_f = 20$ ns, $R_L = 200$ kΩ

CHARACTERISTIC	CONDITIONS V_{DD} (V)	LIMITS ALL PACKAGES			UNITS
		Min.	Typ.	Max.	
Propagation Delay Time; t_{PHL}, t_{PLH}	5	–	180	360	ns
	10	–	90	180	
Transition Time:					
t_{THL}	5	–	35	70	ns
	10	–	20	40	
t_{TLH}	5	–	100	200	
	10	–	50	100	
Maximum Clock Input Frequency, f_{CL}	5	1.5	3	–	MHz
	10	3	6	–	
Average Input Capacitance, C_I (any input)	–	–	5	–	pF





ALL INPUTS (TERMS. 1-11, 13-22) PROTECTED BY CMOS PROTECTION NETWORK

Fig.5 – Functional block diagram.

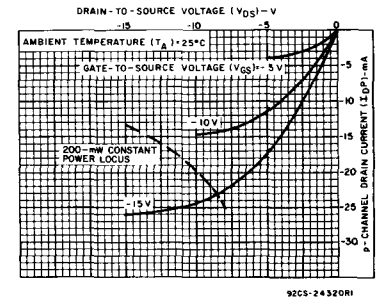


Fig.6 – Typical output p-channel drain characteristics.

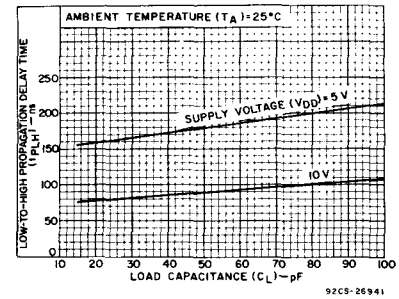


Fig.7 – Typical low-to-high propagation delay time vs. load capacitance.

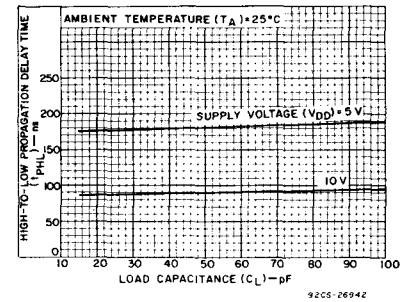


Fig.8 – Typical high-to-low propagation delay time vs. load capacitance.

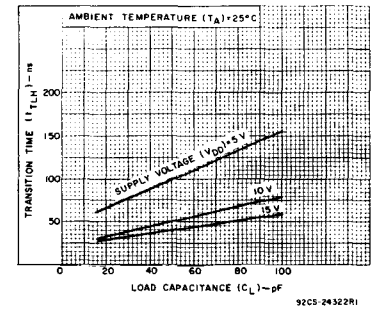


Fig.9 – Typical low-to-high transition time vs. load capacitance.

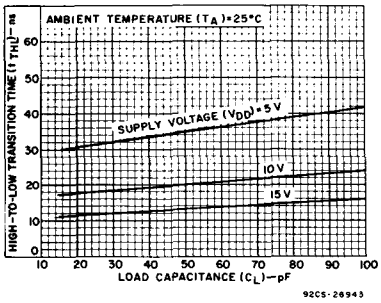


Fig.10 – Typical high-to-low transition time vs. load capacitance.

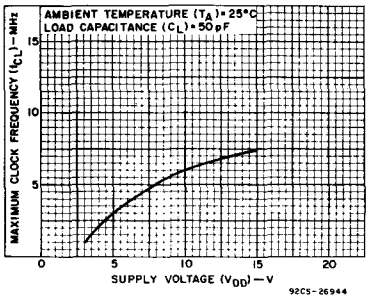


Fig.11 – Typical max. clock frequency vs. supply voltage.

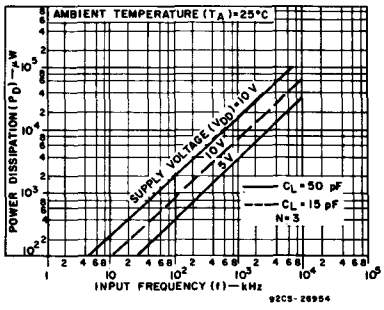


Fig.12 – Typical power dissipation vs. input frequency.

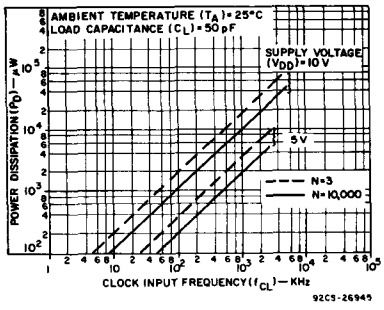


Fig.13 – Typical power dissipation vs. clock input frequency.

TABLE I

MODE SELECT INPUT			FIRST COUNTING SECTION			LAST COUNTING SECTION			COUNTER RANGE	
									DESIGN	EXTENDED
Ka	Kb	Kc	MODE Divides by:	Can be preset to a max of:	Jam▲ inputs used:	MODE Divides by:	Can be preset to a max of:	Jam▲ inputs used:	Max.	Max.
1	1	1	2	1	J1	8	7	J2,J3,J4	15,999	17,331
0	1	1	4	3	J1,J2	4	3	J3,J4	15,999	18,663
1	0	1	5#	4	J1,J2,J3	2	1	J4	9,999	13,329
0	0	1	8	7	J1,J2,J3	2	1	J4	15,999	21,327
1	1	0	10	9	J1,J2,J3,J4	1	0	–	9,999	16,659
X	0	0	MASTER PRESET			MASTER PRESET			–	–

X = Don't Care

▲ J1 = Least significant bit.
J4 = Most significant bit.

#Operation in the ÷5 mode (1st counting section) requires going through the Master Preset mode prior to going into the ÷5 mode. At power turn-on, kc must be a logic "0" for a period of 3 input clock pulses after V_{DD} reaches a minimum of 3 volts. See Fig. 21 for a suggested external preset circuit.

HOW TO PRESET THE CD4059A TO DESIRED ÷ N

The value N is determined as follows:

$$N = [MODE^*] \quad [1000 \times \text{Decade 5 Preset} + 100X \text{ Decade 4 Preset} + 10X \text{ Decade 3 Preset} + 1X \text{ Decade 2 Preset}] + \text{Decade 1 Preset} \qquad (1)$$

* MODE= First counting section divider (10, 8, 5, 4 or 2)

To calculate preset values for any N count, divide the N count by the Mode.

The resultant is the corresponding preset values of the 5th through 2nd decade with the remainder being equal to the 1st decade value.

$$\text{Preset Value} = \frac{N}{\text{Mode}} \qquad (2)$$

Examples:

A) N = 8479, Mode = 5

1695 + 4 ← Preset Values

5 | 8479

Mode, N

MODE SELECT = 5

Ka	Kb	Kc
1	0	1

PROGRAM JAM INPUTS (BCD)

4			1	5				9				6			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	0	1	1	1	0	1	0	1	0	0	1	0	1	1	0

To verify the results use equation 1 :

N = 5 (1000X 1 + 100 X 6 + 10 X 9 + 1 X 5) + 4

N = 8479

B) N = 12382, Mode = 8

1547 + 6

8 | 12382

MODE SELECT = 8

Ka	Kb	Kc
0	0	1

PROGRAM JAM INPUTS

6			1	7				4				5			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
0	1	1	1	1	1	1	0	0	0	1	0	1	0	1	0

To verify:

N = 8 (1000 X 1 + 100 X 5 + 10 X 4 + 1 X 7) + 6

N = 12382

MODE SELECT = 10

C) N = 8479, Mode = 10

$$10 \overline{)\,8479}\quad 0847 + 9$$

Ka	Kb	Kc
1	1	0

PROGRAM JAM INPUTS

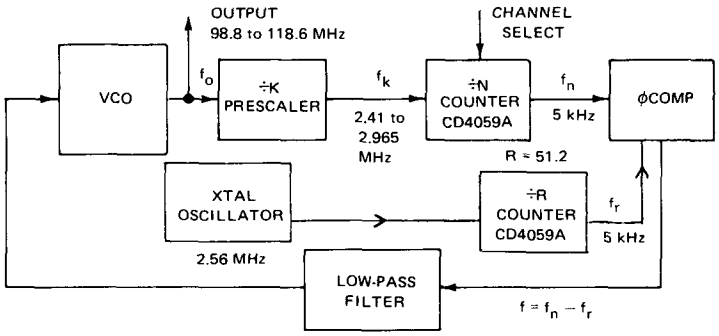
9				7				4				8			
J1	J2	J3	J4	J5	J6	J7	J8	J9	J10	J11	J12	J13	J14	J15	J16
1	0	0	1	1	1	1	0	0	0	1	0	0	0	0	1

To Verify:

N = 10 (1000 X 0 + 100 X 8 + 10 X 4 + 1 X 7) + 9

N = 8479

DIGITAL PHASE-LOCKED LOOP (PLL) FOR FM BAND SYNTHESIZER



1) Calculating Min & Max "N" Values :

Output Freq. Range (f_o) = 98.8 to 118.6 MHz

Channel Spacing Freq. (f_c) = 200 kHz

Division Factor (k) = 40

$$\text{Reference Freq. } (fr) = \frac{f_c}{k} = \frac{200}{40}\ \text{kHz} = 5\ \text{kHz}$$

$$f_k = \frac{f_o}{40} \quad : \quad f_k\text{Max.} = \frac{118.6\ \text{MHz}}{40} = 2.965\ \text{MHz};\ f_k\text{Min} = \frac{98.8\ \text{MHz}}{40} = 2.47\ \text{MHz}$$

$$N = \frac{f_o}{f_c}$$

$$N_{Max} = \frac{118.6\ \text{MHz}}{200\ \text{kHz}} = 593 \qquad N_{Min} = \frac{98.8\ \text{MHz}}{200\ \text{kHz}} = 494 \qquad R = \frac{2.56\ \text{MHz}}{5\ \text{kHz}} = 512$$

"CASCADING" VIA OTHER COUNTERS

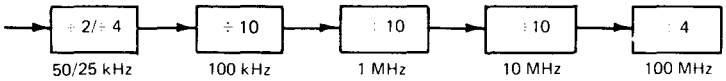
Fig. 14 shows a BCD-switch compatible arrangement suitable for ÷ 8 and ÷ 5 modes, which can be adapted, with slight changes, to the other divide-by-modes. In order to be able to preset to any number from three to about 256,000, while preserving the BCD-switch compatible character of the jam inputs, a rather complex cascading scheme is required. Such a cascading scheme is necessary because the CD4059A can never be preset to a count less than 3 and logic is needed to detect the condition that one of the numbers to be preset in the CD4059A is rather small. In order to simplify the detection logic, only that condition is detected where the jam inputs to terminals 6, 7, and 9 would be low during one count. If such a condition is detected, and if at least 1 is expected to be jammed into the MSB counter, the detection logic removes one from the number to be jammed into the MSB counter (with a place value of 2000 times the divide-by-mode) and jams the same 2000 into the CD4059A by forcing terminals 6, 7, and 9 high.

The clock of the CD4013A may be driven directly from the output of the CD4059A, as shown by dashed option (1), or by the inverted output of the CD4059A, option (2). If option (2) is used the CD4029A cannot count cycles shorter than 3. If option (1) is used propagation delay problems may occur at high counting speeds.

The general circuit in Fig.14 can be simplified considerably if the range of the cascaded counters does not have to start at a very low value. Fig.15 shows an arrangement in the ÷ 4 mode, where the counting range extends in a BCD-switch compatible manner from 88,003 to 103,999. The arrangement shown in Fig.15 is easy to follow; once during each cycle, the less significant digits are jammed in (14,712 in this case) and then 11,000 (4 x 2750) is jammed in eight times in succession, by forcing jam inputs high or low, as required.

Numbers larger than the extended counter range can also be produced by cascading the CD4059A with some other counting device. Fig.16 shows such an arrangement where only one fixed divide-by number is desired which is close to three times the extended counter range as shown in the last column of Table I. The dual flip-flop wired to produce a ÷ 3 count, can be replaced by other counters such as the CD4029, CD4510, CD4516, CD4017, or the CD4022. In Fig.16 the ÷ N subsystem is preset once to a number smaller than the desired divide-by number. This smaller number represents the less significant digits of the divide-by number. The subsystem is then preset one or more times to a round number (e.g. 1000, 2000) and multiplied by the number of the divide-by mode (÷ 2 in the example of Fig.16). It is important that the second counting device has an output that is high or low, as the case may be, during only one of its counting states.

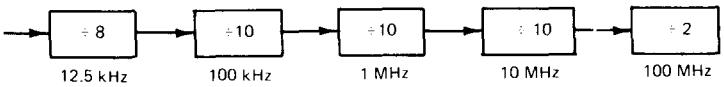
2) ÷ N Counter Configuration for UHF – 220 to 400 MHz
Channel Spacing: 50 kHz or 25 kHz



$$N_{Max} = \frac{400\ MHz}{25\ kHz} = 16{,}000 \qquad N_{Max} = \frac{400\ MHz}{50\ kHz} = 8{,}000$$

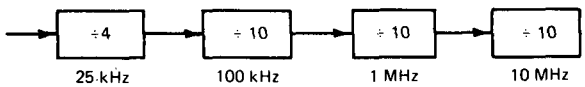
$$N_{Min} = \frac{220\ MHz}{25\ kHz} = 8{,}800 \qquad N_{Min} = \frac{220\ MHz}{50\ kHz} = 4{,}400$$

3) ÷ N Counter Configuration to VHF – 116 MHz
Channel Spacing = 12.5 kHz



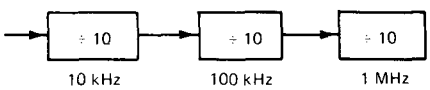
$$N_{Max} = \frac{160\ MHz}{12.5\ kHz} = 12{,}800 \qquad N_{Min} = \frac{116\ MHz}{12.5\ kHz} = 9{,}300$$

4) ÷ N Counter Configuration for VHF – 30 to 80 MHz
Channel Spacing: 25 kHz



$$N_{Max} = \frac{80\ MHz}{25\ kHz} = 3{,}200 \qquad N_{Min} = \frac{30\ MHz}{25\ kHz} = 1200$$

5) ÷ N Counter Configuration for AM – 995 to 2055 kHz
Channel Spacing = 10 kHz



$$N_{Max} = \frac{2055\ kHz}{10\ kHz} = 205 \qquad N_{Min} = \frac{995\ kHz}{10\ kHz} = 99$$

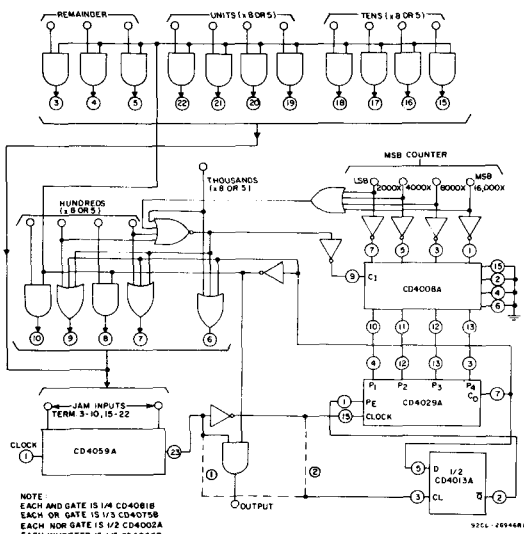


Fig.14 – BCD switch-compatible ÷N system of the most general kind.

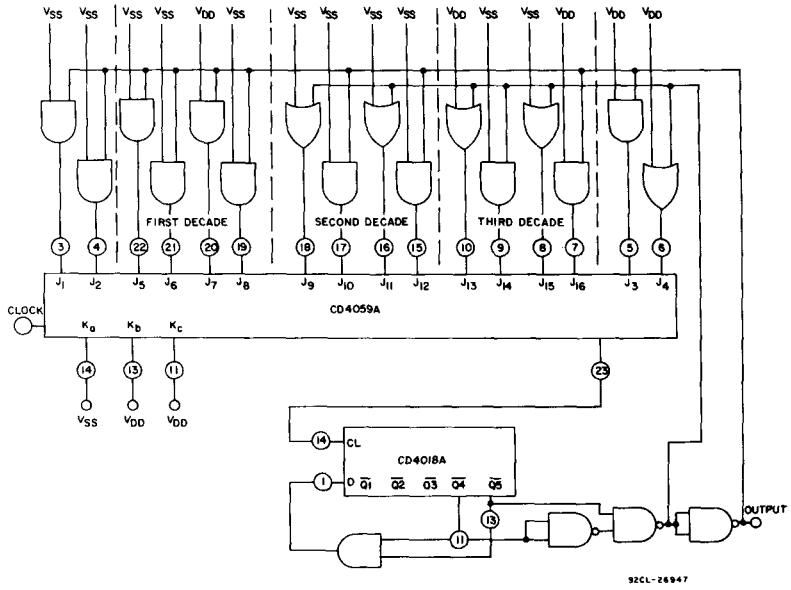


Fig.15 – Dividing by any number from 88,003 to 103,999.

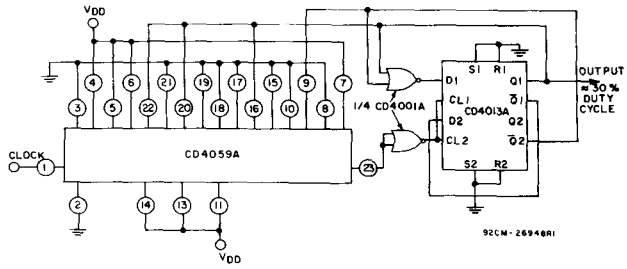


Fig.16 – Division by 47,690 in ÷2 mode.

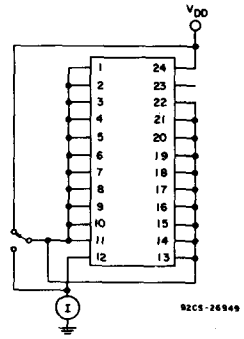


Fig.17 – Quiescent device current test circuit.

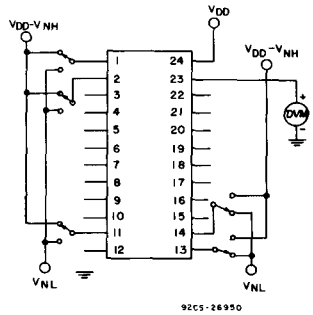


Fig.18 – Noise immunity test circuit.

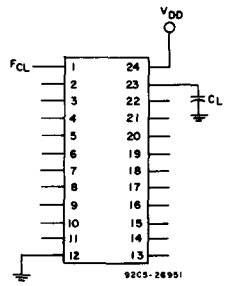


Fig.19 – Power dissipation test circuit (all ÷ modes).

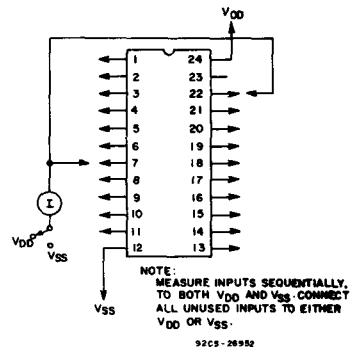
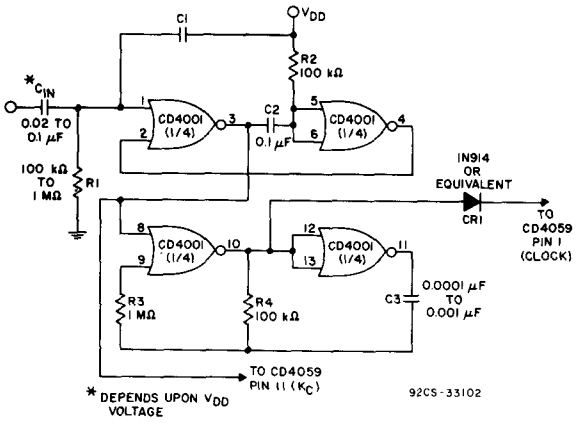
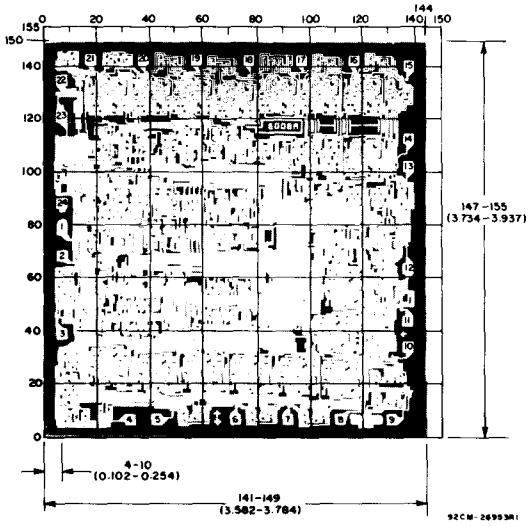


Fig.20 – Input leakage current test circuit.



For changing from any mode other than mode 5 (with power on), apply positive pulse to C_{in}. This circuit automatically selects master preset mode (K_b = 0, K_c = 0) before going into the select conditions for mode 5 (K_a = 1, K_b = 0, K = 1). The selection of C_1 and C_2 is critical. C_1 is determined by the VDD voltage--the lower VDD's need larger C_1's. C_2 must be 0.1 μF or larger.

Fig.21 - CD4059A mode 5 power on master preset circuit.



The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CD4059AH.

CMOS 14-Stage Ripple-Carry Binary Counter/Divider and Oscillator

The RCA-CD4060A consists of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits. A RESET input is provided which resets the counter to the all-0's state and disables the oscillator. A high level on the RESET line accomplishes the reset function. All counter stages are master-slave flip-flops. The state of the counter is advanced one step in binary order on the negative transition of $\phi_I(\phi_O)$. All inputs and outputs are fully buffered.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

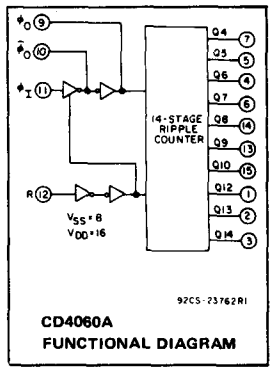
- **4-MHz operating frequency (typ.) at $V_{DD} - V_{SS}$ = 10 V**
- **Common reset**
- **Fully static operation**
- **10 buffered outputs available**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 μA at 15 V (full package-temperature range)**
- **1-V noise margin (full package-temperature range)**

Oscillator Features:

- **All active components on chip**
- **RC or crystal oscillator configuration**

Applications:

- **Timers**
- **Frequency dividers**



CD4060A FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE (T_{stg}) ..... −65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPES D, F, K, H ..... −55 to +125°C
PACKAGE TYPE E ..... −40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... −0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = −40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
INPUT VOLTAGE RANGE, ALL INPUTS ..... −0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS at T_A = 25°C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, K, H Packages		*E Package*		
		Min.	Max.	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Input-Pulse Width, t_W f = 100 kHz	5	400	–	500	–	ns
	10	110	–	125	–	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$	5	–	15	–	15	μs
	10	–	7.5	–	7.5	
Input-Pulse Frequency, f_ϕ	5	–	1	–	0.9	MHz
	10	–	3	–	2.75	
Reset Pulse Width, t_W	5	1000	–	1250	–	ns
	10	500	–	600	–	

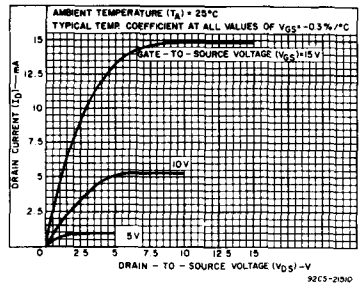


Fig. 1 – Typical n-channel drain characteristics.

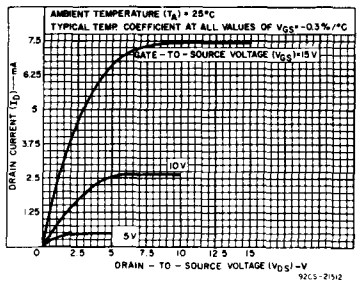


Fig. 2 – Minimum n-channel drain characteristics.

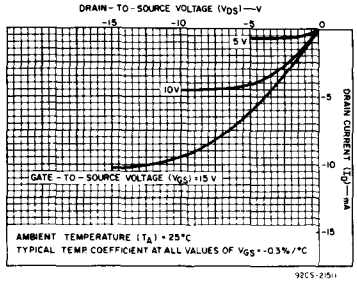


Fig. 3 – Typical p-channel drain characteristics.

CD4060A Types

STATIC ELECTRICAL CHARACTERISTICS

Characteristic	Conditions			Limits at Indicated Temperatures (°C)								Units
				D, F, K, H Packages				E Package				
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	+25 Typ.	+25 Limit	+125	−40	+25 Typ.	+25 Limit	+85	
Quiescent Device Current I_L Max.	–	–	5	15	0.5	15	900	50	1	50	700	μA
	–	–	10	25	1	25	1500	100	2	100	1400	
	–	–	15	50	2.5	50	2000	500	5	500	5000	
Output Voltage: Low Level, V_{OL}	–	5	5	0 Typ.; 0.05 Max.								V
	–	10	10	0 Typ.; 0.05 Max.								
High Level V_{OH}	–	0	5	4.95 Min.; 5 Typ.								
	–	0	10	9.95 Min.; 10 Typ.								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	1.5 Min.; 2.25 Typ.								V
	9	–	10	3 Min.; 4.5 Typ.								
Inputs High V_{NH}	0.8	–	5	1.5 Min.; 2.25 Typ.								
	10	–	10	3 Min.; 4.5 Typ.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min.								V
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min.								
	1	–	10	1 Min.								
Output Drive Current:* n-Channel (Sink), I_DN Min.	0.5	–	5	0.22	0.36	0.18	0.125	0.21	0.36	0.18	0.15	mA
	0.5	–	10	0.44	0.75	0.36	0.25	0.42	0.75	0.36	0.3	
p-Channel (Source), I_DP Min.	4.5	–	5	-0.15	-0.25	-0.125	-0.085	-0.145	-0.25	-0.125	-0.1	
	9.5	–	10	-0.3	-0.5	-0.25	-0.175	-0.29	-0.5	-0.25	-0.2	
Input Leakage Current, I_{IL}, I_{IH}	Any Input	–	15	$\pm 10^{-5}$ Typ., ±1 Max.								μA

* Data not applicable to Terminal 9 or 10

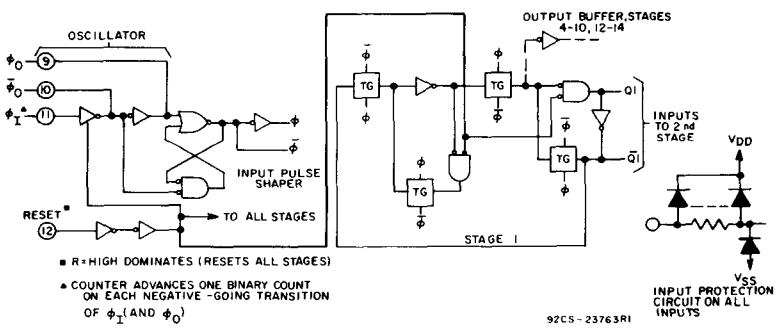


Fig. 7 – Logic diagram of CD4060A oscillator, pulse shaper, and 1 of 14 counter stages.

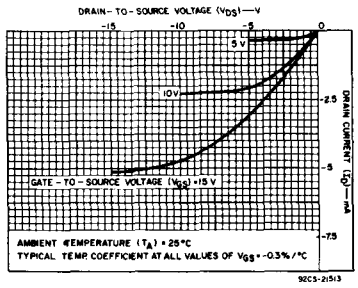


Fig. 4 – Minimum p-channel drain characteristics.

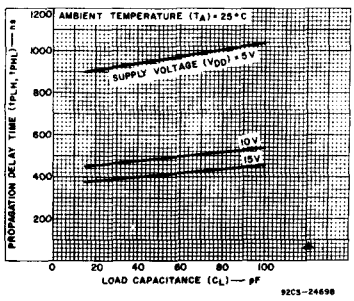


Fig. 5 – Typical propagation delay time vs. load capacitance (ϕ_I to Q4 output).

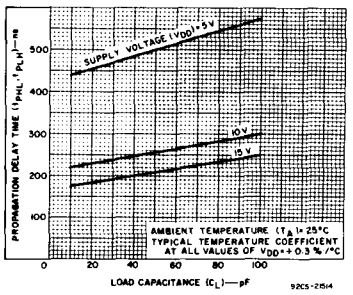


Fig. 6 – Typical propagation delay time vs. load capacitance (Q_n to Q_{n+1}).

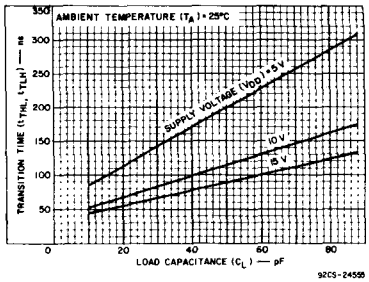


Fig. 8 – Typical output transition time vs. load capacitance.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} (V)	LIMITS D, F, K, H Packages Min.	Typ.	Max.	LIMITS E Package Min.	Typ.	Max.	UNITS
Input-Pulse Operation									
Propagation Delay Time, ϕ_I to Q4 Out; t_{PHL}, t_{PLH}		5	–	900	1800	–	900	1900	ns
		10	–	450	900	–	450	950	
Propagation Delay Time, Q_n to Q_{n+1}; t_{PHL}, t_{PLH}		5	–	450	900	–	450	950	ns
		10	–	225	450	–	225	475	
Transition Time, t_{THL}, t_{TLH}		5	–	150	300	–	150	350	ns
		10	–	75	150	–	75	175	
Min. Input-Pulse Width t_W	f=100 kHz	5	–	200	400	–	200	500	ns
		10	–	75	110	–	75	125	
Input-Pulse Rise & Fall Time, $t_{r\phi}$, $t_{f\phi}$		5	–	–	15	–	–	15	μs
		10	–	–	7.5	–	–	7.5	
Max. Input-Pulse Frequency, f_ϕ		5	1	1.75	–	0.9	1.75	–	MHz
		10	3	4	–	2.75	4	–	
Input Capacitance, C_I	Any Input		–	5	–	–	5	–	pF
Reset Operation									
Propagation Delay Time, t_{PHL}		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	
Minimum Reset Pulse Width, t_W		5	–	500	1000	–	500	1250	ns
		10	–	250	500	–	250	600	

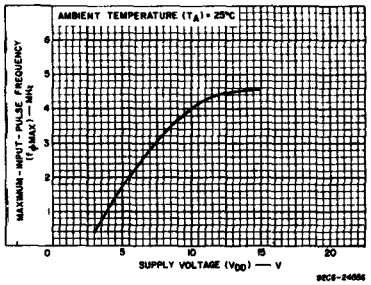


Fig. 9 – Typical maximum-input-pulse frequency vs. supply voltage.

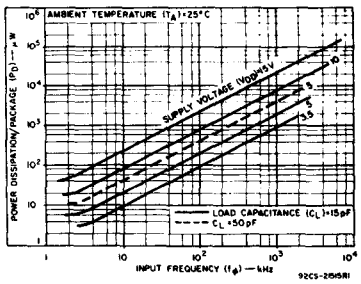


Fig. 10 – Typical dynamic power dissipation characteristics.

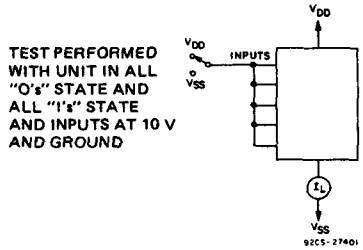


Fig. 11 – Quiescent-device current test circuit.

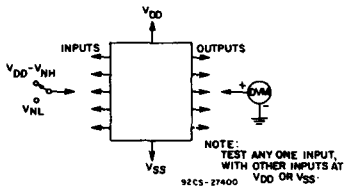


Fig. 12 – Noise-immunity test circuit.

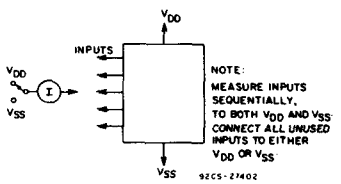


Fig. 13 – Input-leakage-current test circuit.

CD4062A Types

CMOS 200-Stage Dynamic Shift Register

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES K, T, H ..... -55 to +125°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

For T_A = -55 to +100°C (PACKAGE TYPES K, T) ..... 500 mW

For T_A = +100 to +125°C (PACKAGE TYPES K, T) ..... Derate Linearly at 12 mW/°C to 200 mW

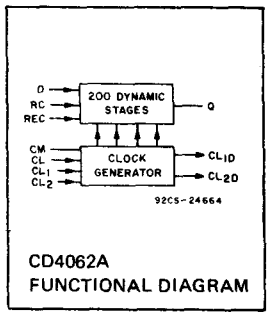
DEVICE DISSIPATION PER OUTPUT TRANSISTOR

For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C



CD4062A
FUNCTIONAL DIAGRAM

The RCA-CD4062A is a 200-stage dynamic shift register with provision for either single- or two-phase clock input signals. Single-phase-clocked operation is intended for low-power, low clock-line capacitance requirements. Single-phase clocking is specified for medium-speed operation (< 1 MHz) at supply voltages up to 10 volts. Clock input capacitance is extremely low (< 5 pF), and clock rise and fall times are non-critical. The clock-mode signal (CM) must be low for single-phase operation.

Two-phase clock-input signals may be used for high-speed operation (up to 5 MHz) or to further reduce clock rise and fall time requirements at low speeds. Two-phase operation is specified for supply voltages up to 15 volts. Clock input capacitance is only 50 pF/phase. The clock-mode signal (CM) must be high for two-phase operation. The single-phase-clock input has an internal pull-down device which is activated when CM is high and may be left unconnected in two-phase operation.

The logic level present at the data input is transferred into the first stage and shifted one stage at each positive-going clock transition for single-phase operation, and at the positive-going transition of CL_1 for two-phase operation.

The CD4062A-Series types are supplied in 12-lead hermetic TO-5 packages (T suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Features:

- **Minimum shift rates over full temperature range—**

  Single-phase clock: $3 V \leq V_{DD} \leq 10 V$; f_{min} = 10 kHz; $-55° C \leq T_A \leq +125° C$ (f_{min} = 1 kHz up to $T_A \leq 75° C$)

  Two-phase clock: $3 V \leq V_{DD} \leq 15 V$; f_{min} = 10 kHz; $-55° C \leq T_A \leq +125° C$ (f_{min} = 1 kHz up to $T_A \leq 75° C$)

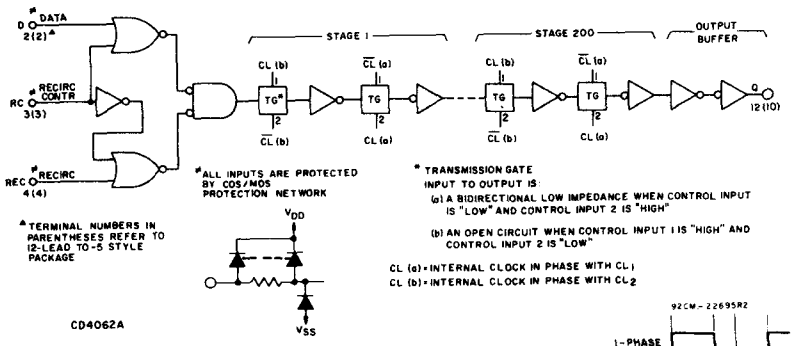


Fig. 1 – CD4062A logic block diagram.

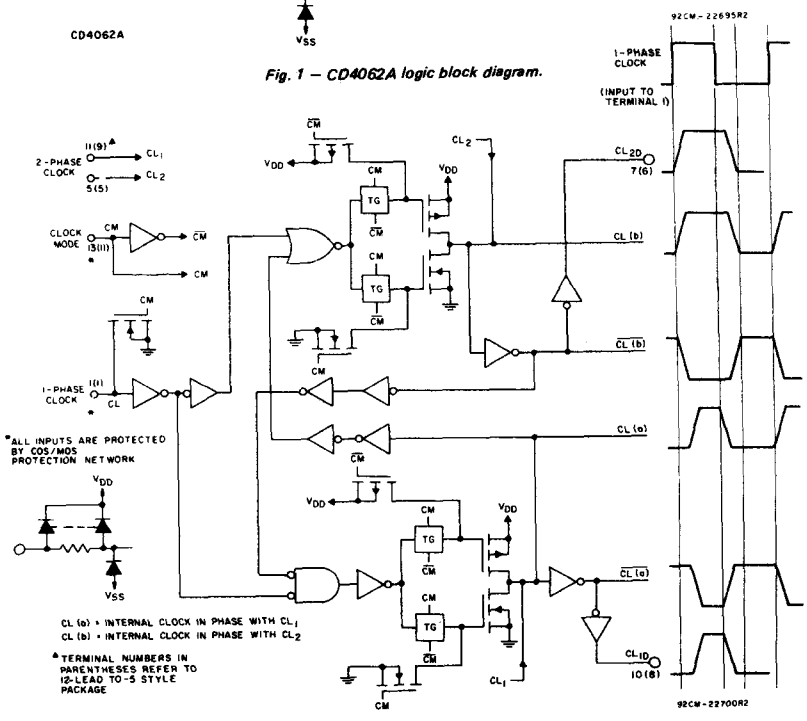


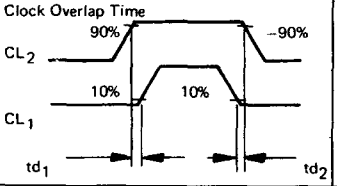
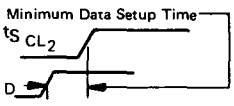
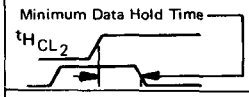
Fig. 2 – Clock circuit logic diagram.

RECOMMENDED OPERATING CONDITIONS at T_A = 25° C, Except as Noted.
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	V_{DD} (V)	LIMITS MIN.	LIMITS MAX.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range):				
Single-Phase Clock		3	10	V
Two-Phase Clock		3	12	V
Clock Input Frequency, f_{CL}*	5	0.15	500	kHz
	10	0.15	1000	kHz
Clock Pulse Width, t_W*	5	250	66.7 X 10^6	ns
	10	500	66.7 X 10^6	ns
Clock Rise or Fall Times, t_rCL or t_fCL*	5	–	10	μs
	10	–	1	μs
Data Hold Time, t_H*	5	150	–	ns
	10	50	–	ns

* For single-phase clock, 50% duty cycle

Two-Phase Clock Operation (CL_1, CL_2); Clock Mode (CM) = High; 3 V ≤ V_{DD} ≤ 15 V. See Figure 4.

CHARACTERISTIC	TEST CONDITIONS V_{DD} V	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Maximum Clock Input Frequency, f_{CL}	5	1.25	2.5	–	MHz
	10	2.5	5	–	MHz
Minimum Clock Input Frequency, f_{CL}	5	150	10	–	Hz
	10	150	10	–	Hz
Clock Overlap Time 		40	–	–	ns
Average Input Capacitance, C_I CL_1, CL_2		–	50	–	pF
Propagation Delays; t_{PHL}, t_{PLH} CL_1 to Q	5	–	250	500	ns
	10	–	100	200	ns
CL_1 to CL_{1D} CL_2 to CL_{2D}	5	–	250	500	ns
	10	–	100	200	ns
Minimum Data Setup Time 	5	–	150	300	ns
	10	–	50	100	ns
Minimum Data Hold Time 	5	–	–	0	ns
	10	–	–	0	ns
Clock Rise and Fall Times t_rCL_1, CL_2 t_fCL_1, CL_2		No Restrictions If Clock Overlap Requirement Is Met			

Features (Cont'd):

- Low power dissipation
  0.3 mW/bit at 1 MHz and 10 V
  0.04 mW/bit at 0.5 MHz and 5V
  (alternating 1-0 data pattern)
- Data output TTL-DTL compatible
- Recirculating capability
- Delayed two-phase clock outputs available for cascading registers
- Asynchronous ripple-type presettable to all 1's or 0's
- Ultra-low-power-dissipation standby operation
- Quiescent current specified to 15 V
- Maximum input leakage current of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications:

- Serial shift registers
- Time-delay circuits
- CRT refresh memory
- Long serial memory

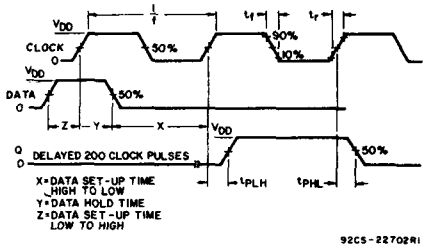


Fig. 3 – Timing diagram–single-phase clock.

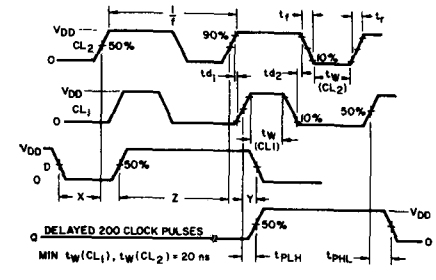


Fig. 4 – Timing diagram–two-phase clock.

CD4062A Types

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS		CONDITIONS V_O (V)	V_{IN} (V)	V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) -55	+25 TYP.	+25 LIMIT	+125	UNITS
Quiescent Device Current, I_L Max.		–	–	5	12	0.5	12	720	μA
		–	–	10	25	1	25	1500	
CM=High, CL_1=High, CL_2=Low		–	–	15	50	1	50	2000	
Output Voltage: Low Level, V_{OL}		–	5	5	0 Typ.; 0.05 Max				V
		–	10	10	0 Typ.; 0.05 Max				
High Level V_{OH}		–	0	5	4.95 Min.; 5 Typ.				
		–	0	10	9.95 Min.; 10 Typ.				
Noise Immunity: Inputs Low, V_{NL}		4.2	–	5	1.5 Min.; 2.25 Typ.				V
		9	–	10	3 Min.; 4.5 Typ.				
Inputs High V_{NH}		0.8	–	5	1.5 Min.; 2.25 Typ.				
		1	–	10	3 Min.; 4.5 Typ.				
Noise Margin: Inputs Low, V_{NML}		4.5	–	5	1 Min.				V
		9	–	10	1 Min.				
Inputs High, V_{NMH}		0.5	–	5	1 Min.				
		1	–	10	1 Min.				
Output Drive Current: N-Channel (Sink), I_DN Min.	Q	0.4	–	4.5	1.6	2.6	1.3	0.91	mA
	Output	0.5	–	10	5	8*	4	3.2	
	CL_{1D},	0.5	–	5	0.87	1.4	0.7	0.49	
	CL_{2D}	0.5	–	10	2.2	3.6	1.8	1.26	
P-Channel (Source):		4.5	–	5	-0.31	-0.5	-0.25	-0.17	mA
I_DP Min.	Q	2.5	–	5	-0.93	-1.5	-0.75	-0.52	
	Output	9.5	–	10	-0.87	-1.4	-0.7	-0.49	
	CL_{1D},	4.5	–	5	-0.43	-0.7	-0.35	-0.24	
	CL_{2D}	9.5	–	10	-1.1	-1.8	-0.9	-0.63	
Input Leakage Current, I_{IL}, I_{IH}		Any Input –	–	15	$\pm 10^{-5}$ Typ., ±1 Max.				μA

* Maximum power dissipation rating ⩽ 200 mW.

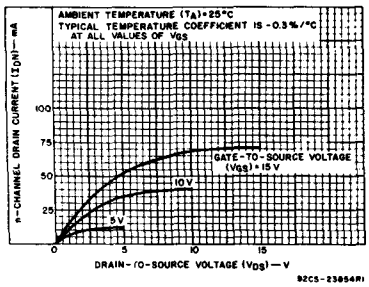


Fig. 5— Typical n-channel drain characterstics for Q output.

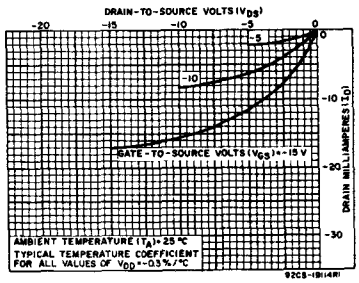


Fig. 6— Typical p-channel drain characteristics for Q output.

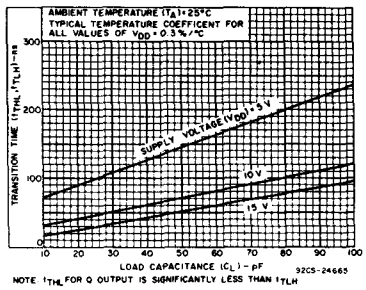


Fig. 7— Typical transition time vs. C_L for data outputs.

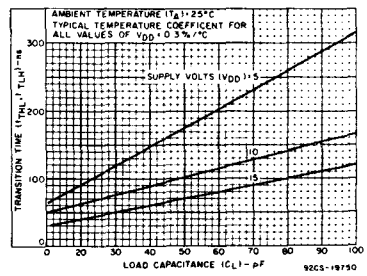
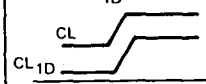
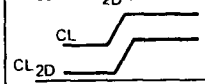
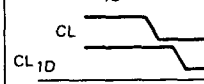
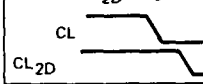
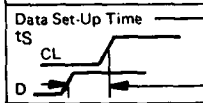
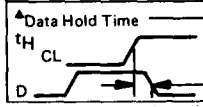


Fig. 8— Typical transition time vs. C_L for delayed clock output.

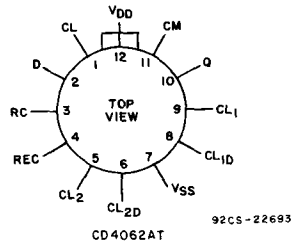
DYNAMIC CHARACTERISTICS AT T_A = 25°C, V_{SS} = 0 V, C_L = 50 pF, Input t_r, t_f = 20 ns, except t_rCL and t_fCL

Single-Phase-Clock Operation; Clock Mode (CM) = Low; 3 V ≤ V_{DD} ≤ 10 V (See Figure 3)

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS
Maximum Clock Input Frequency, f_{CL} (50% Duty Cycle)	t_r, t_f=20 ns	5	0.5	1	–	MHz
		10	1	2	–	
Minimum Clock Input Frequency, f_{CL} (50% Duty Cycle)		5	150	10	–	Hz
		10	150	10	–	
Clock Rise and Fall Times** t_rCL, t_fCL		5	–	–	10	μs
		10	–	–	1	
Average Input Capacitance, C_I	All Inputs Except CL_1 and CL_2		–	5	–	pF
Propagation Delays: CL to Q		5	–	1000	2000	ns
		10	–	400	800	
CL to CL_{1D} (Positive Going) 	(50% Points)	5	–	750	1500	ns
		10	–	300	600	
CL to CL_{2D} (Positive Going) 	(50% Points)	5	–	500	1000	
		10	–	200	400	
CL to CL_{1D} (Negative Going) 	(50% Points)	5	–	450	900	
		10	–	175	350	
CL to CL_{2D} (Negative Going) 	(50% Points)	5	–	750	1500	
		10	–	300	600	
Transition Time: t_{TLH}, t_{THL} Q Output		5	–	100	200	ns
		10	–	50	100	
CL_{1D}, CL_{2D}		5	–	200	400	
		10	–	100	200	
Data Set-Up Time t_S 		5	–	–	0	ns
		10	–	–	0	
▲Data Hold Time t_H 		5	–	–	150	ns
		10	–	–	150	

** If more than one unit is cascaded in single-phase parallel clocked application, t_rCL should be made less than or equal to the sum of the propagation delay at 15 pF, and the transition time of the output driving stage. (See Figs. 5 and 7 for cascading options.)

▲ Use of delayed clock permits high-speed logic to precede CD4062A register (see cascade register operation).



CD4062AT

TERMINAL DIAGRAM

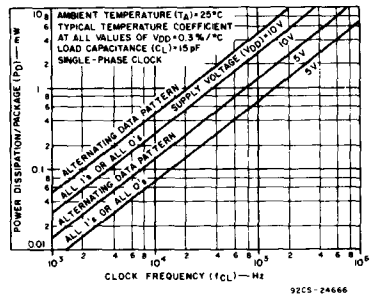


Fig. 9— Typical power dissipation vs. frequency.

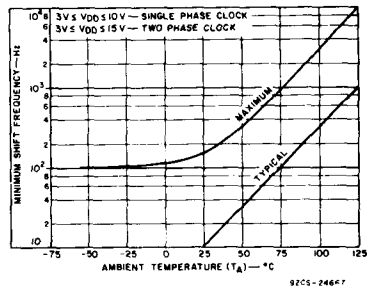


Fig. 10— Minimum shift frequency vs. ambient temperature.

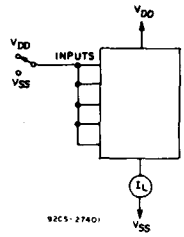


Fig. 11— Quiescent-device-current test circuit.

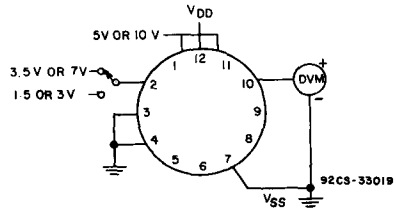


Fig. 12— Noise-immunity test circuit.

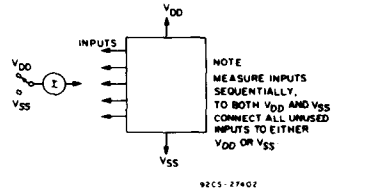


Fig. 13—Input-leakage-current test circuit.

CD4066A Types

CMOS Quad Bilateral Switch

For Transmission or Multiplexing of Analog or Digital Signals

RCA CD4066A is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with RCA-CD4016, but exhibits a much lower ON resistance. In addition, the ON resistance is relatively constant over the full input-signal range.

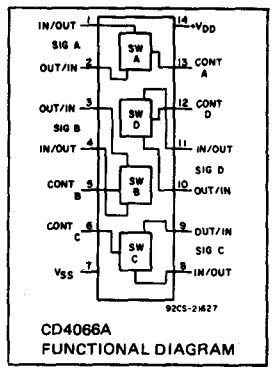
The CD4066A consists of four independent bilateral switches. A single control signal is required per switch. Both the p and the n device in a given switch are biased ON or OFF simultaneously by the control signal. As shown in Fig. 1, the well of the n-channel device on each switch is either tied to the input when the switch is ON or to V_{SS} when the switch is OFF. This configuration eliminates the variation of the switch-transistor threshold voltage with input signal, and thus keeps the ON resistance low over the full operating-signal range.

The advantages over single-channel switches include peak input-signal voltage swings equal to the full supply voltage, and more constant ON impedance over the input-signal range. For sample-and-hold applications, however, the CD4016 is recommended.

These types are supplied in 14-lead hermetic dual-in-line ceramic packages (D and 'F' suffixes), 14-lead dual-in-line plastic package (E suffix), 14-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- **15-V digital or ± 7.5-V peak-to-peak switching**
- **80Ω typical ON resistance for 15-V operation**
- **Switch ON resistance matched to within 5 Ω over 15-V signal-input range**
- **ON resistance flat over full peak-to-peak signal range**
- **High ON/OFF output-voltage ratio: 65 dB typ. @ f_{is} = 10 kHz, R_L = 10 kΩ**
- **High degree of linearity: < 0.5% distortion typ. @ f_{is} = 1 kHz, V_{is} = 5 V_{p-p}, $V_{DD}-V_{SS} \geq$ 10 V, R_L = 10 kΩ**
- **Extremely low OFF switch leakage resulting in very low offset current and high effective OFF resistance: 10 pA typ. @ $V_{DD}-V_{SS}$ = 10 V, T_A = 25°C**
- **Extremely high control input impedance (control circuit isolated from signal circuit): 10^{12} Ω typ.**
- **Low crosstalk between switches: -50 dB typ. @ f_{is} = 0.9 MHz, R_L = 1 kΩ**
- **Matched control-input to signal-output capacitance: Reduces output signal transients**
- **Frequency response, switch ON = 40 MHz (typ.)**
- **Quiescent current specified to 15-V**
- **Maximum control input leakage current of 1-μA at 15-V (Full package-temperature range)**



CD4066A
FUNCTIONAL DIAGRAM

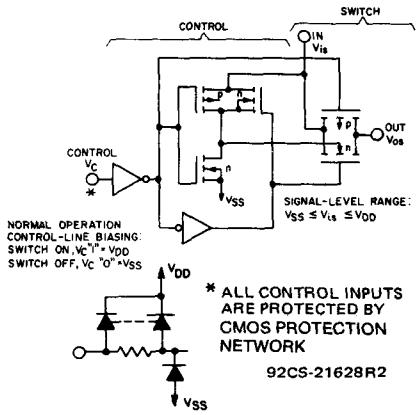


Fig. 1 – Schematic diagram of 1 of 4 identical switches and its associated control circuitry.

SPECIAL CONSIDERATIONS – CD4066A

1. In applications where separate power sources are used to drive V_{DD} and the signal inputs, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066A bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066A.
2. In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8, or 11, the voltage drop across the bidirectional switch must not exceed 0.8 volt (calculated from R_{ON} values shown).

   No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9, or 10.
3. Minimum bilateral switch output load resistance is 100 Ω.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +125°C

OPERATING TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, K, H . . . . . -55 to +125°C

PACKAGE TYPE E . . . . . -40 to +85°C

DC SUPPLY VOLTAGE RANGE, V_{DD}

(Voltages referenced to V_{SS}) . . . . . -0.5 to +15 V

INPUT CURRENT (TRANSMISSION GATE INCL.) . . . . . ±10 mA

POWER DISSIPATION PER PACKAGE:

FOR T_A = -40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 12 mW/°C . . . . . 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K) Derate Linearly at 12 mW/°C . . . 200 mW

DEVICE DISSIPATION PER SECTION:

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

ALL SIGNAL AND DIGITAL CONTROL INPUTS . . . . . $V_{SS} \leq V_I \leq V_{DD}$

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

OPERATING CONDITIONS AT T_A = 25°C

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD}	MIN.	MAX.	UNITS
Supply Voltage Range (T_A = Full Package Temperature Range)	–	3	12	V

Applications:

- **Analog signal switching/multiplexing**
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating switch
- **Digital signal switching/Multiplexing**
- **Transmission-gate logic implementation**
- **Analog-to-digital & digital-to-analog conversion**
- **Digital control of frequency, impedance, phase, and analog-signal gain**

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS *All Voltage Values Are in Volts*			LIMITS Values at -55°C, +25°C, +125°C Apply to D, F, K, H Packages; Values at -40°C, +25°C, +85°C Apply to E Package						UNITS
			V_{DD} (V)	-55°	-40°	+85°	+125°	+25° TYP.	+25° MAX.	
Quiescent Device Current, I_L max. D, F, H Pkgs.			5	0.25	–	–	7.5	0.01	0.25	μA
			10	0.5	–	–	15	0.01	0.5	
			15	2	–	–	40	0.02	2	
E Pkg.			5	–	2.5	15	–	0.25	2.5	μA
			10	–	5	30	–	0.25	5	
			15	–	50	500	–	0.5	50	
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})										
ON Resistance, R_{ON} Max.	$V_C = V_{DD}$	V_{SS}	V_{is}							Ω
	$R_L = 10k\Omega$*									
	+7.5	-7.5	-7.5 to +7.5	220	250	300	320	80	280	
	+15	0	0 to +15							
	+5	-5	-5 to +5	400	450	520	550	120	500	
	+10	0	0 to +10							
	+2.5	-2.5	-2.5 to +2.5	3000	3500	5200	5500	270	5000	
	-5	0	0 to +5							
Δ_{ON} Resistance Between Any 2 of 4 Switches, ΔR_{ON}	$R_L = 10k\Omega$*									Ω
	+7.5 or +15	-7.5 or 0	+7.5 to -7.5; +15 to 0	–	–	–	–	5	–	
	+5 or +10	-5 or 0	+5 to -5; +10 to 0	–	–	–	–	10	–	
Sine Wave Response (Distortion)	+5	-5	5V p-p▲	–	–	–	–	0.4	–	%
	$R_L = 10k\Omega$, $f_{is} = 1kHz$									
Frequency Response Switch ON (Sine-Wave Input)	+5	-5	-5 p-p	–	–	–	–	40	–	MHz
	$R_L = 1k\Omega$, $20\log_{10}\frac{V_{os}}{V_{is}} = -3dB$									
Feedthrough-Switch OFF	+5	-5	-5 p-p	–	–	–	–	1.25	–	MHz
	$R_L = 1k\Omega$, $20\log_{10}\frac{V_{os}}{V_{is}} = -50dB$									
Input or Output Leakage – Switch OFF (Effective OFF Resistance)	V_{DD}	$V_C = V_{SS}$	±7.5	–	–	–	–	±0.1	±100*	nA
	+7.5	-7.5								
	+5	-5	±5	–	–	–	–	±0.1	±100*	
Crosstalk Between Any 2 of the 4 Switches (f at –50 dB)	$V_C(A)=V_{DD}=+5$, $V_C(B)=V_{SS}=-5$, $R_L = 1k\Omega$		(A) 5V p-p	–	–	–	–	0.9	–	MHz
	$20\log_{10}\frac{V_{os}(B)}{V_{is}(A)} = -50dB$									

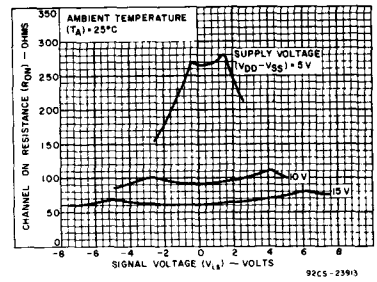


Fig. 2 (a) – Typical channel ON resistance vs. signal voltage for three values of supply voltage ($V_{DD}-V_{SS}$).

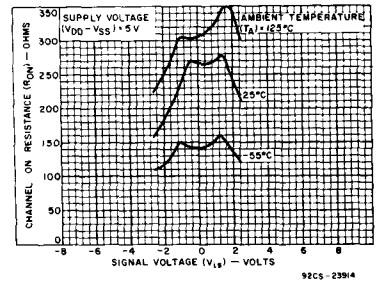


Fig. 2 (b) – Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 5 V.

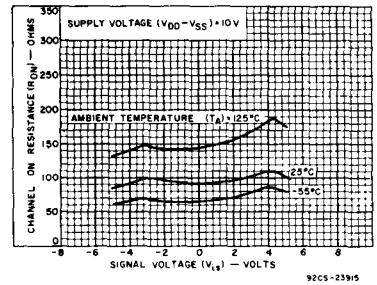


Fig. 2 (c) – Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 10 V.

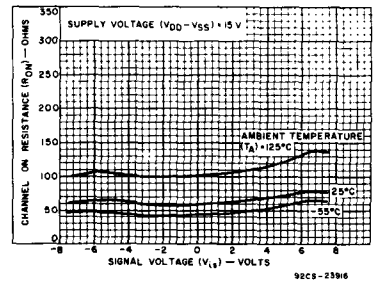


Fig. 2 (d) – Typical channel ON resistance vs. signal voltage with supply voltage ($V_{DD}-V_{SS}$) = 15 V.

ELECTRICAL CHARACTERISTICS (Cont'd)

CHARACTERISTIC	TEST CONDITIONS *All Voltage Values Are in Volts*		V_{DD} (V)	LIMITS Values at -55°C, +25°C, +125°C Apply to D, F, K, H Packages; Values at -40°C, +25°C, +85°C Apply to E Package						UNITS
				-55°	-40°	+85°	+125°	+25° TYP.	+25° MAX.	
Propagation Delay (Signal Input to Signal Output) t_{pd}	V_{DD} = 5	$V_C = V_{DD}$, V_{SS} = GND, C_L = 15pF, V_{is} = sq. wave, t_r, t_f = 20 ns (Input Signal)		–	–	–	–	20	50	ns
	V_{DD} = 10			–	–	–	–	10	25	
Capacitance: Input, C_{is}		V_{DD} = +5, $V_{CC} = V_{SS}$ = -5		–	–	–	–	8	–	pF
Output, C_{os}				–	–	–	–	8	–	
Feedthrough, C_{ios}				–	–	–	–	0.5	–	
CONTROL (V_C)										
Noise Immunity, V_{NL} Min.	$V_{is} \leq V_{DD}$, I_{is} = 10μA, $V_{DD} - V_{SS}$ = 10			2	2	2	2	2 min 4.5	–	V
Input Leakage Current, I_{IL} Max.	$V_{is} \leq V_{DD}$, $V_{DD} - V_{SS}$ = 15, $V_C \leq V_{DD} - V_{SS}$			±1				$\pm 10^{-6}$	±1	μA
Crosstalk Control Input to Signal Output	$V_{DD} - V_{SS}$ = 10, V_C = 10 (sq. wave), $t_{rC} = t_{fC}$ = 20 ns	R_L = 10kΩ		–	–	–	–	50	–	mV
Propagation Delay, t_{pdC}		R_L = 300kΩ, $V_{is} \leq 10$, C_L = 15pF		–	–	–	–	35	–	ns
Maximum Allowable Control Input Repetition Rate	V_{DD} = 10, V_{SS} = GND, R_L = 1kΩ, C_L = 15pF, V_C = 10 (sq. wave), t_r, t_f = 20 ns			–	–	–	–	10	–	MHz
Av. Input Capacitance, C_I				–	–	–	–	5	–	pF

* Limit determined by minimum feasible leakage measurement for automatic testing.

Δ Symmetrical about 0 volts. • For all test conditions.

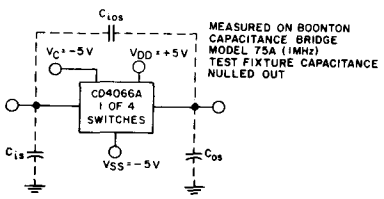


Fig. 6 – Capacitance test circuit.

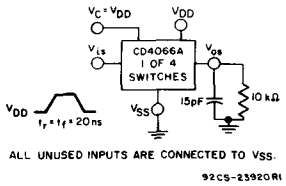


Fig. 8 – Propagation delay time signal input (V_{is}) to signal output (V_{os}).

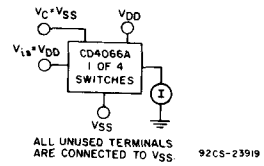


Fig. 7 – OFF switch input or output leakage.

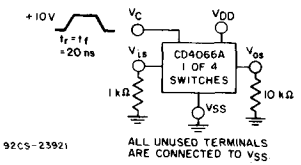


Fig. 9 – Crosstalk-control input to signal output.

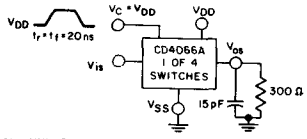


Fig. 11 – Propagation delay t_{PLH}, t_{PHL} control-signal output.

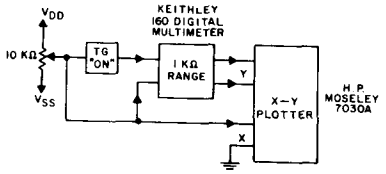


Fig. 3 – Channel ON resistance measurement circuit.

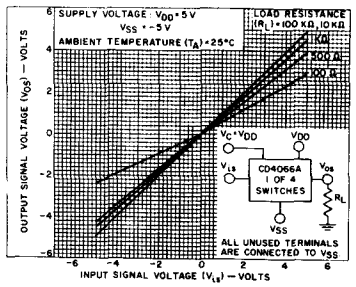


Fig. 4 – Typical ON characteristics for 1 of 4 channels.

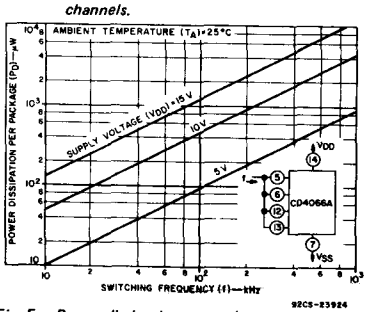


Fig. 5 – Power dissipation per package vs. switching frequency.

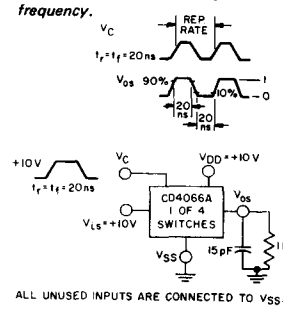


Fig. 10 - Maximum allowable control input repetition rate.

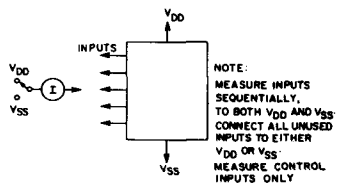


Fig. 12 – Input leakage current test circuit.

CMOS Telecommunications, Display-Driver, and Interface Circuits

Technical Data

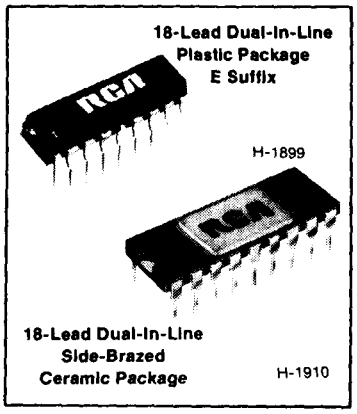
CA3300 Types

CMOS Video Speed 6-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

Features:

- *CMOS low power with speed*
- *Parallel conversion technique*
- *15-MHz sampling rate (66-ns conversion time)*
- *6-bit latched 3-state output with overflow bit*
- *±½ LSB accuracy*
- *Single supply voltage (3 to 10 V)*
- *2 units in series allow 7-bit output*
- *2 units in parallel allow 30-MHz sampling rate*
- *Internal V_{REF} with ext V_{REF} option*
- *Available with EVP processing for improved reliability*



The RCA-CA3300 types are CMOS 50-mW parallel (FLASH) analog-to-digital converters designed for applications demanding both low-power consumption and high-speed digitization.

The CA3300 types operate over a wide full-scale input-voltage range of 2.4 volts up to the dc supply voltage with maximum power consumption as low as 50 to 200 mW, depending upon the clock frequency selected. When operated from a 5-volt supply at a clock frequency of 11 MHz, the power consumption of the CA3300 is less than 50 mW. When operated from an 8-volt supply at a frequency of 15 MHz, the power consumption is less than 150 mW.

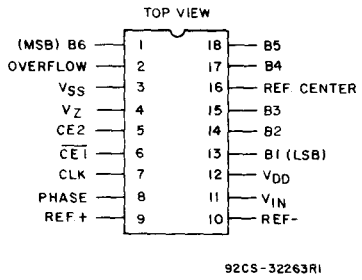
The intrinsic high conversion rate makes the CA3300 types ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3300's in series to increase the resolution of the conversion system. A series connection of two CA3300's may be used to produce a 7-bit high-speed converter. Operation of two CA3300's in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz). CA3300's in parallel may be combined with a high-speed 6-bit D/A converter, a binary adder, control logic, and an op amp to form a very-high-speed A/D converter.

Sixty-four paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3300. Sixty-three comparators are required to quantize all input voltage levels in this 6-bit converter, and the additional comparator is required for the overflow bit.

The CA3300 types are available as follows: Types CA3300D and CA3300DX in an 18-lead dual-in-line ceramic package (D suffix), types CA3300E and CA3300CE in an 18-lead dual-in-line plastic package (E suffix), or in chip form (H suffix). The CA3300DX offers the additional advantage of improved reliability as a result of EVP (Extra Value Program) processing. For further information on EVP, see RCA publication EVP-300B or contact your RCA representative.

Applications:

- *The CA3300 types are especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing (industrial/security)*
- *High-speed A/D conversion*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *High-energy physics research*
- *High-speed oscilloscope storage/display*
- *General-purpose hybrid ADC's*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*



TERMINAL ASSIGNMENT

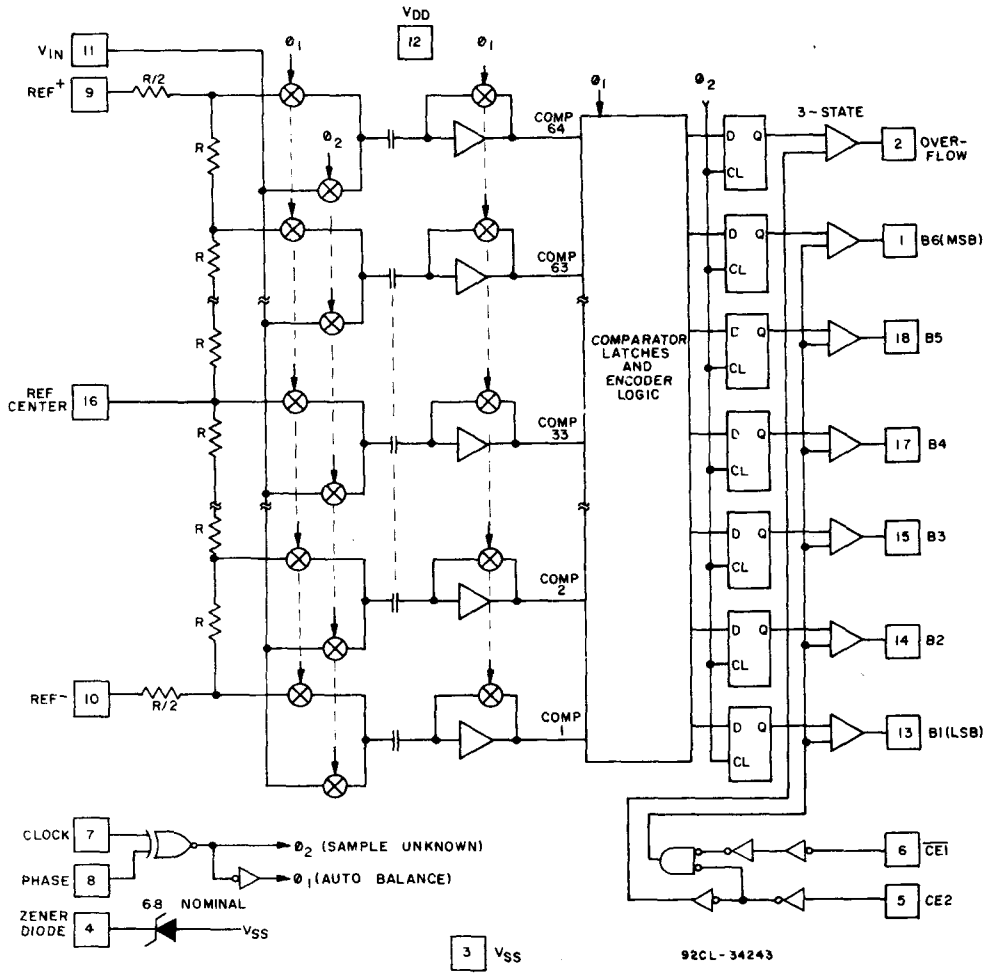


Fig. 1 - Block diagram for the CA3300.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE (V_{DD})
(VOLTAGE REFERENCED TO V_{SS} TERMINAL) ..... -0.5 to 10 V
INPUT VOLTAGE RANGE
ALL INPUTS EXCEPT ZENER (PIN 4) ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT
CLK, PH, $\overline{CE1}$, CE2, V_{IN} ..... ± 10 mA
POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A = -55 to +55°C ..... 315 mW
FOR T_A = +55°C to +125°C ..... Derate linearly at 3.3 mW/°C
TEMPERATURE RANGE
OPERATING (CA3300DX, Refer to Fig. 3) ..... -55 to +125°C
OPERATING (CA3300D, E, CE) ..... -40 to +85°C
STORAGE ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS @ 25°C	LIMITS CA3300D, DX, E			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	6	Bits
Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=15 MHz, gain adjusted	—	±0.5	±0.8	LSB
Differential Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=15 MHz	—	±0.5	±0.8	LSB
Quantizing Error		-½	—	½	LSB
Analog Input:	V_{DD}=8 V				
Full Scale Range	CLK=15 MHz	2.4	—	V_{DD}+0.5	V
Input Capacitance		—	50	—	pF
Input Current		—	600	1000	μA
Gain Temperature Coefficient	V_{DD}=8 V, CLK=15 MHz	—	0.016	—	LSB/°C
Maximum Conversion Speed	V_{DD}=5 V	—	12M	—	SPS
	V_{DD}=8 V	15M	19M	—	SPS
Device Current	V_{DD}=5 V (CLK=11 MHz)	—	7	—	mA
(Excludes I_{REF}, I_Z)	V_{DD}=8 V (CLK=15 MHz)	—	22	—	mA
	V_{DD}=5 V (Auto Balance State)	—	6.4	16	mA
	V_{DD}=8 V (Auto Balance State)	—	24	40	mA
Ladder Impedance		1000	1400	1800	Ω
Digital Inputs:					
Low Voltage	V_{DD}=5 V	—	—	1.5	V
	V_{DD}=8 V	—	—	2.5	V
High Voltage	V_{DD}=5 V	3.5	—	—	V
	V_{DD}=8 V	5.5	—	—	V
Input Current	V_{DD}=8 V	—	±1	—	μA
Digital Outputs:					
Output Low	V_{DD}=5 V, V_O=0.4 V	1.6	10	—	mA
(Sink) Current	V_{DD}=8 V, V_O=0.5 V	3.2	15	—	mA
Output High	V_{DD}=5 V, V_O=4.6 V	-0.8	6	—	mA
(Source) Current	V_{DD}=8 V, V_O=7.5 V	-1.6	9	—	mA
Zener Voltage	I_Z=10 mA	6.2	6.8	7.4	V
Zener Dynamic Impedance	I_Z=10 mA	—	10	30	Ω
Zener Temperature Coefficient		—	0.5	—	mV/°C
Digital Output Delay, t_d	V_{DD}=8 V	—	20	—	ns
Aperture Time	V_{DD}=8 V	—	25	—	ns

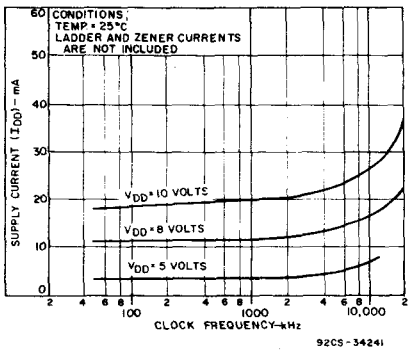


Fig. 2 - Typical current drain versus sampling rate as a function of supply voltage.

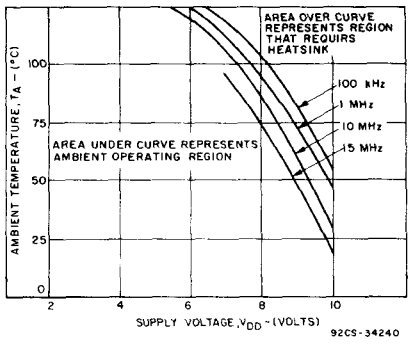


Fig. 3 - Maximum ambient temperature versus supply voltage. (Above curve includes ladder dissipation but not the zener dissipation.)

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS @ 25°C	LIMITS CA3300CE			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	6	Bits
Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=9 MHz, gain adjusted	—	±0.5	±0.8	LSB
Differential Linearity Error	V_{DD}=8 V, V_{REF}=7.68 V CLK=9 MHz	—	±0.5	±0.8	LSB
Quantizing Error		-½	—	½	LSB
Analog Input:	V_{DD}=8 V				
Full Scale Range	CLK=9 MHz	2.4	—	V_{DD}+0.5	V
Input Capacitance		—	50	—	pF
Input Current		—	450	1000	μA
Gain Temperature Coefficient	V_{DD}=8 V, CLK=9 MHz	—	0.016	—	LSB/°C
Maximum Conversion Speed	V_{DD}=5 V	6M	—	—	SPS
	V_{DD}=8 V	9M	19M	—	SPS
Device Current (Excludes I_{REF}, I_Z)	V_{DD}=5 V (CLK=7 MHz)	—	4	—	mA
	V_{DD}=8 V (CLK=9 MHz)	—	12	—	mA
	V_{DD}=5 V (Auto Balance State)	—	6.4	16	mA
	V_{DD}=8 V (Auto Balance State)	—	24	40	mA
Ladder Impedance		1000	1400	1800	Ω
Digital Inputs:					
Low Voltage	V_{DD}=5 V	—	—	1.5	V
	V_{DD}=8 V	—	—	2.5	V
High Voltage	V_{DD}=5 V	3.5	—	—	V
	V_{DD}=8 V	5.5	—	—	V
Input Current	V_{DD}=8 V	—	±1	—	μA
Digital Outputs:					
Output Low (Sink) Current	V_{DD}=5 V, V_O=0.4 V	1.6	10	—	mA
	V_{DD}=8 V, V_O=0.5 V	3.2	15	—	mA
Output High (Source) Current	V_{DD}=5 V, V_O=4.6 V	-0.8	6	—	mA
	V_{DD}=8 V, V_O=7.5 V	-1.6	9	—	mA
Zener Voltage	I_Z=10 mA	6.2	6.8	7.4	V
Zener Dynamic Impedance	I_Z=10 mA	—	10	30	Ω
Zener Temperature Coefficient		—	0.5	—	mV/°C
Digital Output Delay, t_d	V_{DD}=8 V	—	20	—	ns
Aperture Time	V_{DD}=8 V	—	25	—	ns

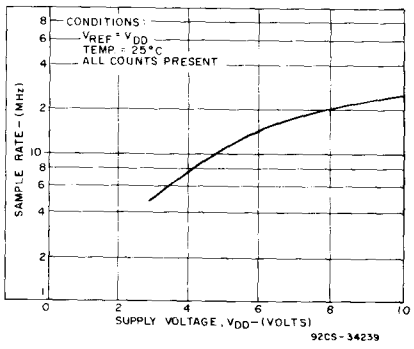


Fig. 4 - Typical maximum sample rate versus supply voltage.

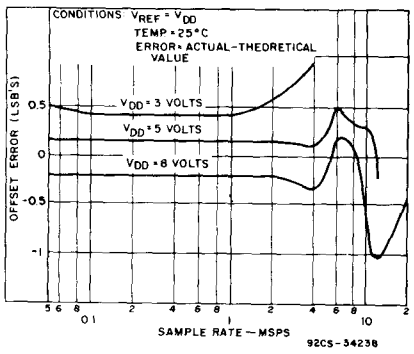
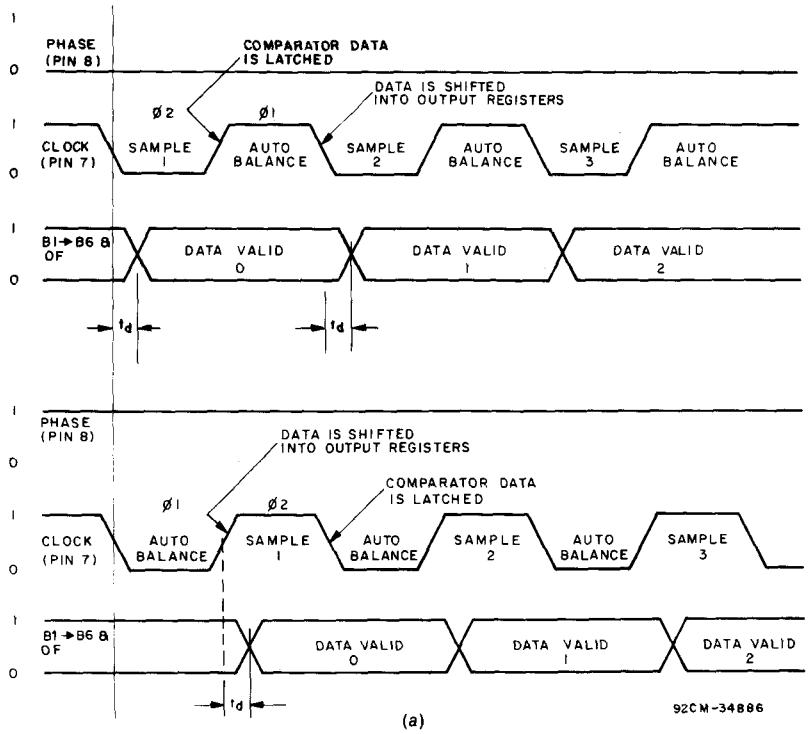
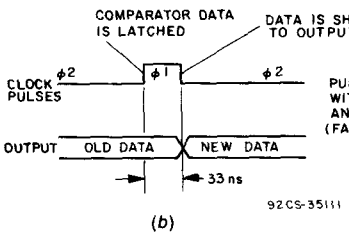


Fig. 5 - Typical offset error versus sample rate as a function of supply voltage. (See literature for offset trim.)





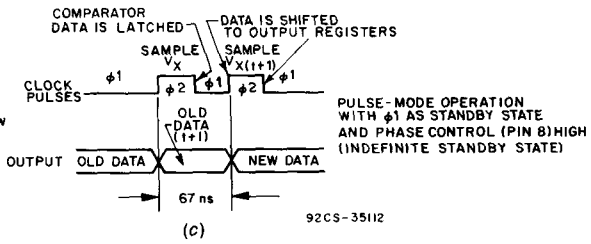


Fig. 6 - Timing diagrams for the CA3300.

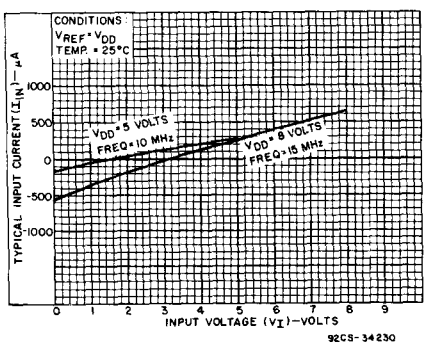


Fig. 7 - Typical input current versus input voltage as a function of supply voltage.

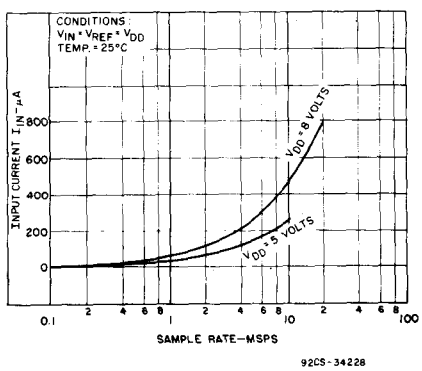


Fig. 8 - Typical input current versus sample rate as a function of supply voltage.

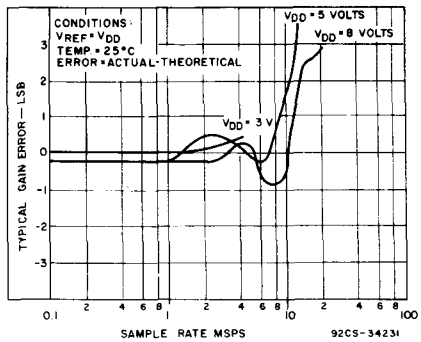


Fig. 9 - Typical gain error versus sample rate as a function of supply voltage. (See literature for gain trim.)

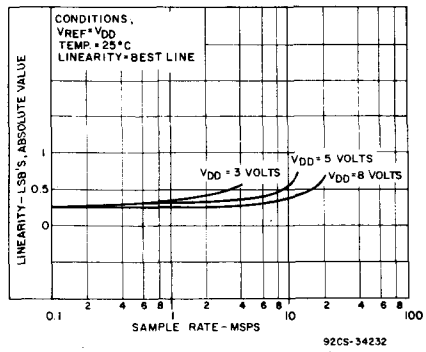


Fig. 10 - Typical linearity versus sample rate as a function of supply voltage.

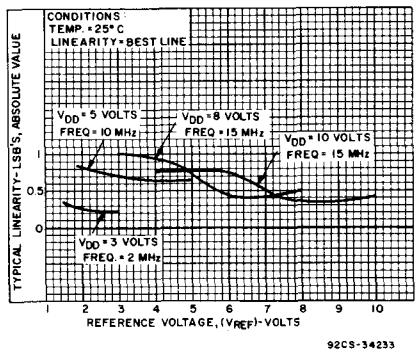


Fig. 11 - Typical linearity versus reference voltage as a function of supply voltage.

Device Operation

A sequential parallel technique is used by the CA3300 converter to obtain its high-speed operation. The sequence consists of the "Auto Balance" phase $\phi 1$ and the "Sample Unknown" phase $\phi 2$. (Refer to the circuit diagram.) Each conversion takes one clock cycle.* With the phase control (pin 8) low, the "Auto Balance" ($\phi 1$) occurs during the High period of the clock cycle, and the "Sample Unknown" ($\phi 2$) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, a transmission switch is used to connect each of 64 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{tap}(N) = [(V_{REF}/64) \times N] - [V_{REF}/(2 \times 64)]$$
$$= V_{REF}[(2N - 1)/128]$$

Where: $V_{tap}(n)$ = reference ladder tap voltage at point n

V_{REF} = voltage across R^- to R^+

N = tap number (1 through 64)

The other side of the capacitor is connected to a single stage amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately, $(V_{DD}-V_{SS})/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted, and V_{IN} is switched to all 64 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators with tap voltages greater than V_{IN} will drive the comparator outputs to a "low" state, all comparators with tap voltage lower than V_{IN} will drive the comparator outputs to a "high" state.

The status of all these comparator amplifiers are stored at the end of this phase ($\phi 2$), by a secondary latching amplifier stage. Once latched, the status of the 64 comparators is decoded by a 64-to 7-bit decode array and the results are clocked into a storage register at the rising edge of the next $\phi 2$.

A 3-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B6 when it is in a high state. CE2 will independently disable B1 through B6 and the OF buffers when it is in the low state.

To facilitate usage of this device a phase-control input is provided which can effectively complement the clock as it enters the chip. Also, an on-board zener is provided for use as a reference voltage.

Continuous Clock Operation

One complete conversion cycle can be traced through the CA3300 via the following steps. (Refer to timing diagram Fig. 6a.) With the phase control in a 'High' state, the rising edge of the clock input will start a "sample" phase. During this entire 'High' state of the clock, the 64 comparators will track the input voltage and the 64 latches will track the comparator outputs. At the falling edge of the clock, all 64 comparator outputs are captured by the 64 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this 'Low' state of the clock the output of the latches propagates through the decode array and a 7-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 7-bit code is shifted into the output registers and appears with time delay t_d as valid data at the output of the 3-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse Mode Operation

For sampling high-speed nonrecurrent or transient data, the converter may be operated in a pulse mode in one of two ways. The fastest method is to keep the converter in the Sample Unknown phase, $\phi 2$, during the standby state. The

*This device requires only a single phase clock. The terminology of $\phi 1$ and $\phi 2$ refers to the High and Low periods of the same clock.

device can now be pulsed through the Auto Balance phase with as little as 33 ns. The analog value is captured on the leading edge of $\phi 1$ and is transferred into the output registers on the trailing edge of $\phi 1$. We are now back in the standby state, $\phi 2$, and another conversion can be started within 33 ns, but not later than 1 μs due to the eventual droop of the commutating capacitors. Another advantage of this method is that it has the potential of having the lowest power drain. The larger the time ratio between $\phi 2$ and $\phi 1$, the lower the power consumption. (See timing diagram Fig. 6b.)

The second method uses the Auto Balance phase, $\phi 1$, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two $\phi 2$ pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second $\phi 2$ pulse is needed to transfer the data into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes place in 67 ns, but the repetition rate may be as slow as desired. The disadvantage to this method is the higher device dissipation due to the low ratio of $\phi 2$ to $\phi 1$. (See timing diagram Fig. 6c.)

Increased Accuracy

In most cases the accuracy of the CA3300 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, three adjustments can be made to obtain better accuracy; i.e., offset trim, gain trim, and midpoint trim.

Offset Trim

In general offset correction can be done in the preamp circuitry by introducing a dc shift to V_{IN} or by the offset trim of the op amp. When this is not possible the R^- (pin 10) input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is ½ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = \tfrac{1}{2} \text{ LSB} = \tfrac{1}{2}(V_{REF}/64)$$
$$= V_{REF}/128$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50-ohm pot connected between R^- and ground will accomplish the adjustment. Set V_{IN} to ½ LSB and trim the pot until the 0 to 1 transition occurs.

If V_{IN} for the first transition is greater than the theoretical, then the 50-ohm pot should be connected between R^- and a negative voltage of about 2 LSB's. The trim procedure is as stated previously.

Gain Trim

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 63 to overflow transition. That voltage is ½ LSB less than V_{REF} and is calculated as follows:

$$V_{IN} \text{ (63 to 64 transition)} = V_{REF} - V_{REF}/128$$
$$= V_{REF}\,(127/128)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overflow transition. Now adjust V_{REF} until that transition occurs on the outputs.

Midpoint Trim

The reference center (RC), pin 16, is available to the user as the approximate midpoint of the resistor ladder. The actual count that is brought out is count 33. To trim the midpoint, the offset and gain trims should be done first. The theoretical transition from count 32 to 33 occurs at 32½ LSB's. That voltage is as follows:

$$V_{IN} \text{ (32 to 33 transition)} = 32.5\ (V_{REF}/64)$$

An adjustable voltage follower can be connected to the RC pin or a 2-K pot can be connected between R^+ and R^- with the wiper connected to RC. Set V_{IN} to the 32 to 33 transition voltage, then adjust the voltage follower or the pot until the transition occurs on the output bits.

The Reference Center point can also be used to create some unique transfer functions. For example, if R^- is grounded, RC is connected to 3.25 volts, and R^+ is connected to 4.8 volts then the lower order counts, 1 through 33, will have an LSB value of 100 mV while the upper order counts, 34 through Overflow, will have an LSB value of 50 mV. This effectively provides twice the sensitivity in the upper counts as compared to the lower counts.

7-Bit Resolution

To obtain 7-bit resolution, two CA3300's can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, three-state outputs, and chip-enabler controls—all of which are available on the CA3300.

The first step for connecting a 7-bit circuit is to totem-pole the ladder networks, as illustrated in Fig. 13. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the seventh bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The three-state outputs of the two devices (bits 1 through 6) are now connected in parallel to complete the circuitry. The complete circuit for a 7-bit A/D converter is shown in Fig. 14.

8-Bit to 12-Bit Conversion Techniques

To obtain 8-to 12-bit resolution and accuracy, use a feed-forward conversion technique. Two A/D converters will be needed to convert up to 11 bits; three A/D converters to convert 12 bits. The high speed of the CA3300 allows 12-bit conversions in the 500 to 900-ns range.

The circuit diagram of a high-speed 12-bit A/D converter is shown in Fig. 15. In the feed-forward conversion method two sequential conversions are made. Converter A first does a coarse conversion to 6 bits. The output is applied to a 6-bit D/A converter whose accuracy level is good to 12 bits. The D/A converter output is then subtracted from the input voltage, multiplied by 32, and then converted by a second flash A/D converter, which is connected in a 7-bit configuration. The answers from the first and second conversions are added together with bit 1 of the first conversion overlapping bit 7 of the second conversion.

When using this method, take care that:

- The linearity of the first converter is better than ½ LSB.
- An offset bias of 1 LSB (1/64) is subtracted from the first conversion since the second converter is unipolar.
- The D/A converter and its reference are accurate to the total number of bits desired for the final conversion (the A/D converter need only be accurate to 6 bits).

  The first converter can be offset-biased by adding a 20-Ω resistor at the bottom of the ladder and increasing the reference voltage by 1 LSB. If a 6.40-voltage reference is used in the system, for example, then the first CA3300 will require a 6.5-V reference.

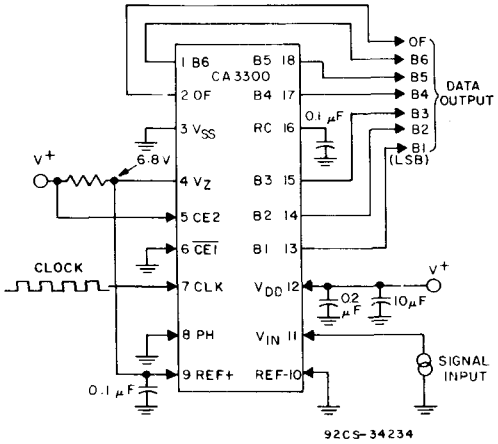


Fig. 12 - Typical CA3300 6-bit configuration 15-MHz sampling rate.

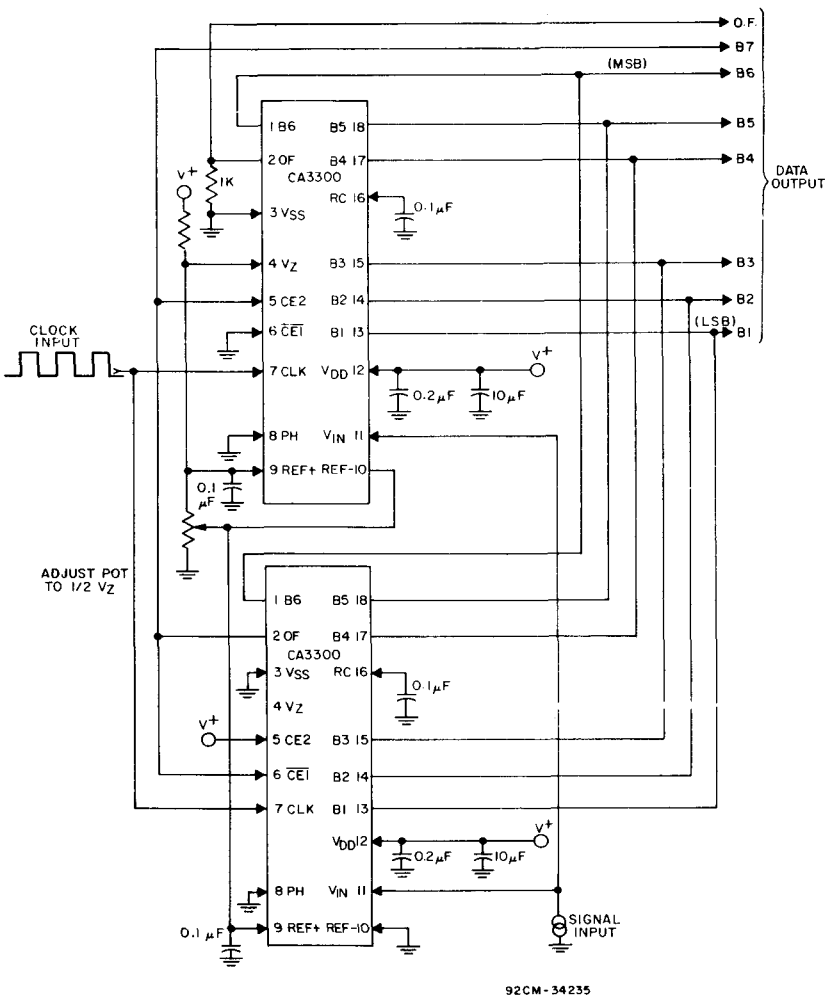


Fig. 13 - Typical CA3300 7-bit resolution configuration 15-MHz sampling rate.

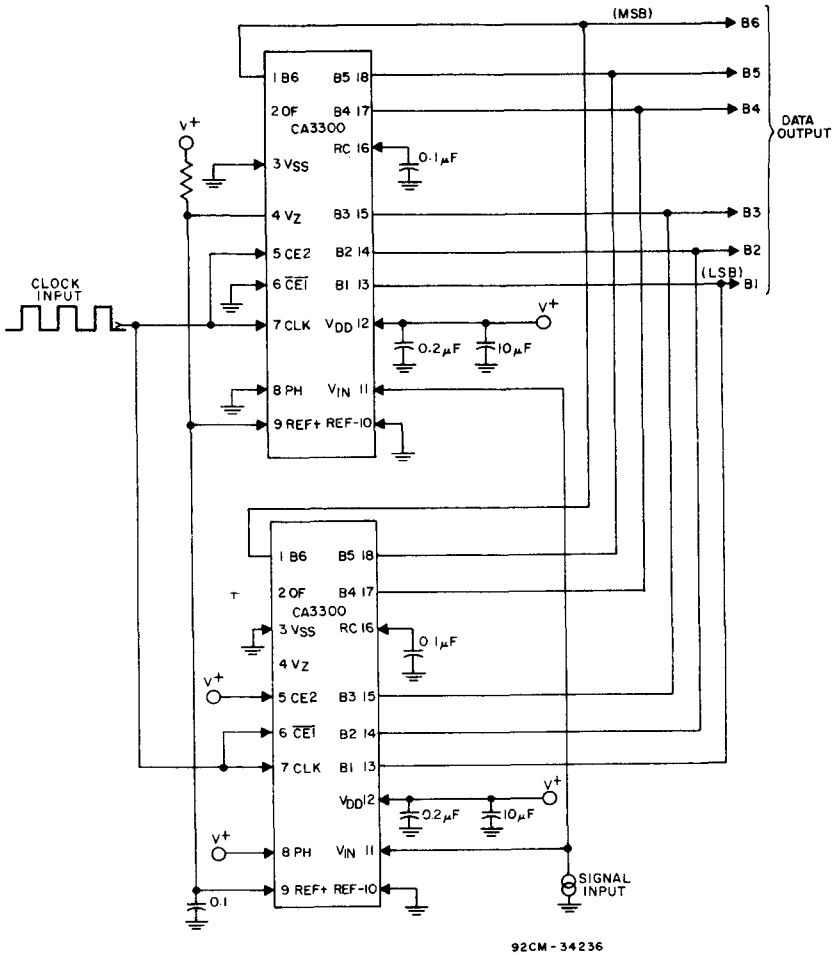


Fig. 14 - Typical CA3300 6-bit resolution configuration 30-MHz sampling rate.

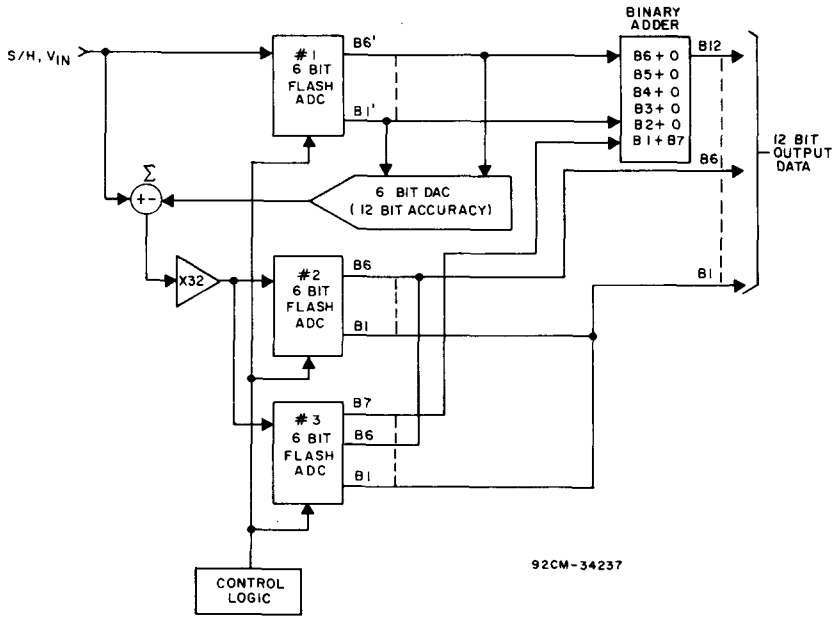


Fig. 15 - Typical CA3300 800-ns 12-bit ADC system.

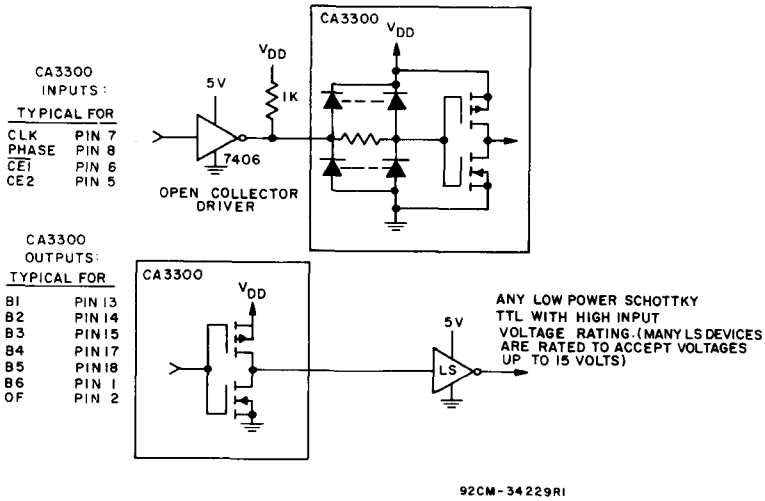
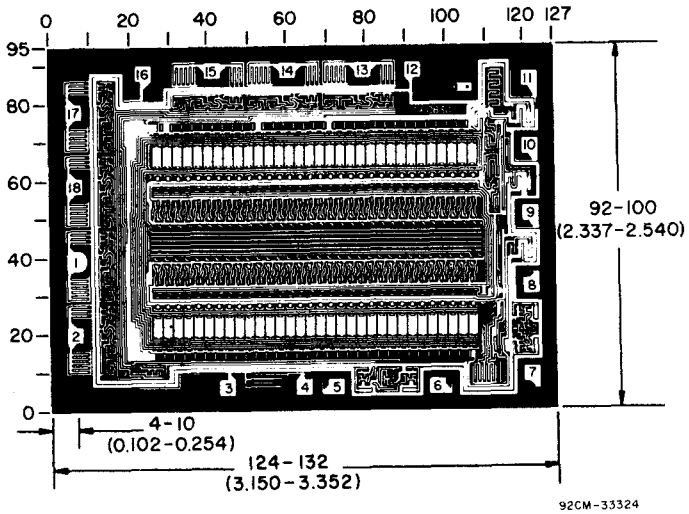


Fig. 16 - TTL interface circuit for $V_{DD} > 5.5$ volts.

OUTPUT CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE* V_{REF} 7.68 (V)	V_{REF} 6.40 (V)	V_{REF} 5.12 (V)	V_{REF} 3.20 (V)	BINARY OUTPUT CODE (LSB) 0F	B6	B5	B4	B3	B2	B1	DECIMAL COUNT
Zero	0.00	0.00	0.00	0.00	0	0	0	0	0	0	0	0
1 LSB	0.12	0.10	0.08	0.05	0	0	0	0	0	0	1	1
2 LSB	0.24	0.20	0.16	0.10	0	0	0	0	0	1	0	2
"		"						"				"
"		"						"				"
"		"						"				"
"		"						"				"
½ Full Scale — 1 LSB	3.72	3.10	2.48	1.55	0	0	1	1	1	1	1	31
½ Full Scale	3.84	3.20	2.56	1.60	0	1	0	0	0	0	0	32
½ Full Scale +1 LSB	3.96	3.30	2.64	1.65	0	1	0	0	0	0	1	33
"		"						"				"
"		"						"				"
"		"						"				"
"		"						"				"
Full Scale — 1 LSB	7.44	6.20	4.96	3.10	0	1	1	1	1	1	0	62
Full Scale	7.56	6.30	5.04	3.15	0	1	1	1	1	1	1	63
Overflow	7.68	6.40	5.12	3.20	1	1	1	1	1	1	1	127

*The voltages listed below are the ideal centers of each output code shown as a function of its associated reference voltage.



Dimensions and pad layout for CA3300H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

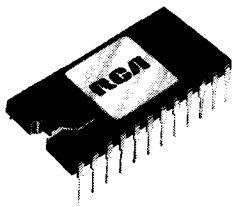
The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

CMOS Video Speed 8-Bit Flash Analog-to-Digital Converter

For Use in Low-Power Consumption, High-Speed Digitization Applications

Features:

- *CMOS low power with SOS speed*
- *Parallel conversion technique*
- *15-MHz sampling rate (66-ns conversion time)*
- *8-bit latched 3-state output with overflow bit*
- *± ½ LSB accuracy (typ.)*
- *Single supply voltage (4 to 8 V)*
- *2 units in series allow 9-bit output*
- *2 units in parallel allow 30-MHz sampling rate*



(D) SUFFIX
24-Lead Dual-In-Line
Side-Brazed Ceramic Package

The RCA CA3308* is a CMOS 200-mW parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high-speed digitization.

The CA3308 operates over a wide full-scale input-voltage range of 4 volts up to 8 volts with maximum power consumptions as low as 200 mW, depending upon the clock frequency selected. When operated from a 5-volt supply at a clock frequency of 15 MHz, the power consumption of the CA3308 is less than 150 mW.

The intrinsic high conversion rate makes the CA3308 ideally suited for digitizing high-speed signals. The overflow bit makes possible the connection of two or more CA3308s in series to increase the resolution of the conversion system. A series connection of two CA3308s may be used to produce a 9-bit high-speed converter. Operation of two CA3308s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15 to 30 MHz). CA3308s may be combined with a high-speed 8-bit D/A converter, a binary adder, control logic, and an op amp to form a very high-speed 15-bit A/D converter.

256 paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3308.

255 comparators are required to quantize all input voltage levels in this 8-bit converter, and the additional comparator is required for the overflow bit.

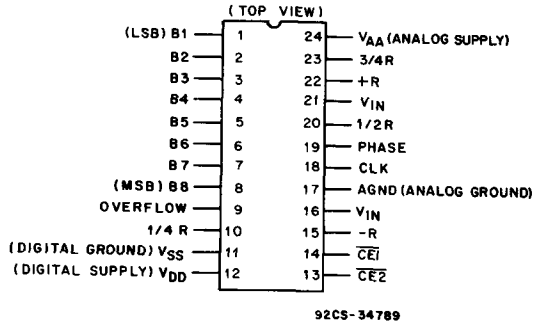
The voltage supply for analog circuitry is termed V_{AA} and AGND. The voltage supply for digital circuitry is termed V_{DD} and V_{SS}.

The CA3308 type is available in a 24-lead dual-in-line ceramic package (D suffix).

* Formerly Developmental Type No. TA11279.

Applications:

- *The CA3308 is especially suited for high-speed conversion applications where low power is also important*
- *TV video digitizing (industrial/security/broadcast)*
- *High-speed A/D conversion*
- *Ultrasound signature analysis*
- *Transient signal analysis*
- *High-energy physics research*
- *High-speed oscilloscope storage/display*
- *General-purpose hybrid ADCs*
- *Optical character recognition*
- *Radar pulse analysis*
- *Motion signature analysis*
- *μP data acquisition systems*



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE (V_{DD} AND V_{AA})
(VOLTAGE REFERENCED TO V_{SS} TERMINAL) ..... −0.5 to +8 V

INPUT VOLTAGE RANGE
ALL INPUTS ..... −0.5 to V_{DD} +0.5 V

DC INPUT CURRENT
CLK, PH, CE1, CE2, V_{IN} ..... ±10 mA

POWER DISSIPATION PER PACKAGE (P_D)
FOR T_A=−40 to 55°C ..... 315 mW
FOR T_A=55°C to 85°C ..... Derate linearly at 3.3 mW/°C

TEMPERATURE RANGE
OPERATING ..... −40 to +85°C
STORAGE ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING)
AT DISTANCE 1/16 ± 1/32 in. (1.59 ± 0.79 mm) FROM CASE FOR 10 s MAX. ..... +265°C

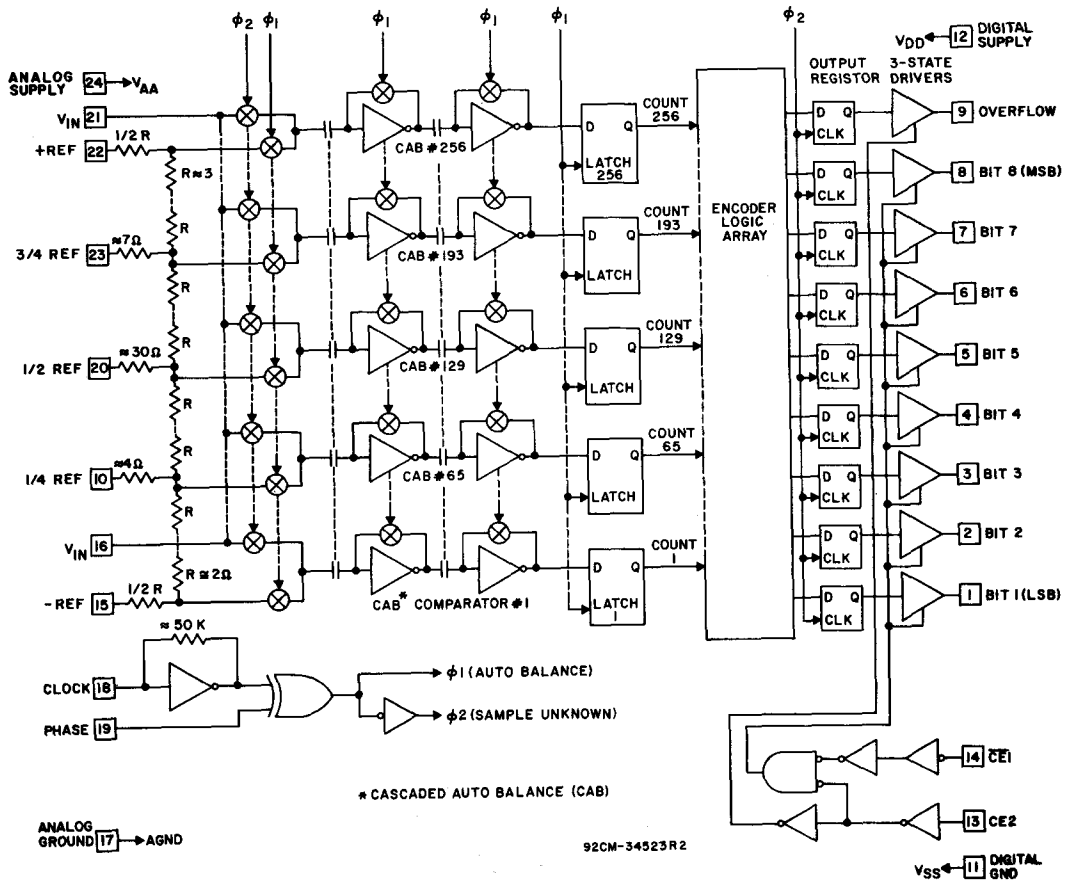


Fig. 1-Block diagram for the CA3308.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	TEST CONDITIONS $V_{AA} = V_{DD}$	LIMITS			UNITS
		MIN.	TYP.	MAX.	
Resolution		—	—	8	Bits
Linearity Error	V_{DD}=5 V, V_{REF}=6.4 V CLK=15 MHz, gain adjusted	—	—	±0.5 ±1	(CA3308AD) (CA3308D)
Differential Linearity Error	V_{DD}=5 V_{REF}=6.4 V CLK=15 MHz	—	—	±0.5 ±1	(CA3308AD) (CA3308D)
Quantizing Error		−½	—	½	LSB
Analog Input:	V_{DD}=5 V				
Full Scale Range	CLK=15 MHz	4	—	8	V
Input Capacitance		—	50	—	pF
Input Current	V_{IN}= 6.4 V	—	1000	2000	μA
Maximum Conversion Speed	V_{DD}=5 V	15 M	17 M	—	SPS
Device Current (Excludes I_{REF})	V_{DD}=5 V (CLK=15 MHz)	—	50	—	mA
Ladder Impedance		300	600	900	Ω
Digital Inputs:					
Low Voltage		—	—	1.5	V
High Voltage	V_{DD}=5 V	3.5	—	—	V
Input Current (Except Pin 18)		—	±1	—	μA
Digital Outputs:					
Output Low (Sink) Current	V_{DD}=5 V, V_O=0.4 V	3.2	10	—	mA
Output High (Source) Current	V_{DD}=5 V, V_O=4.6 V	1.6	−6	—	
Digital Output Delay, t_d	V_{DD}=5 V	—	25	—	ns

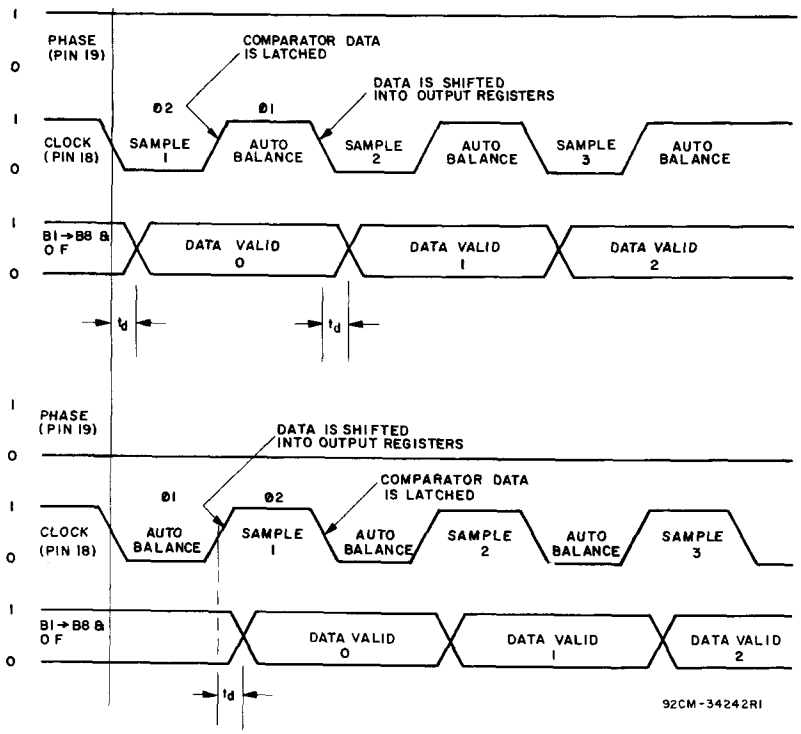


Fig. 2-Timing diagram for the CA3308.

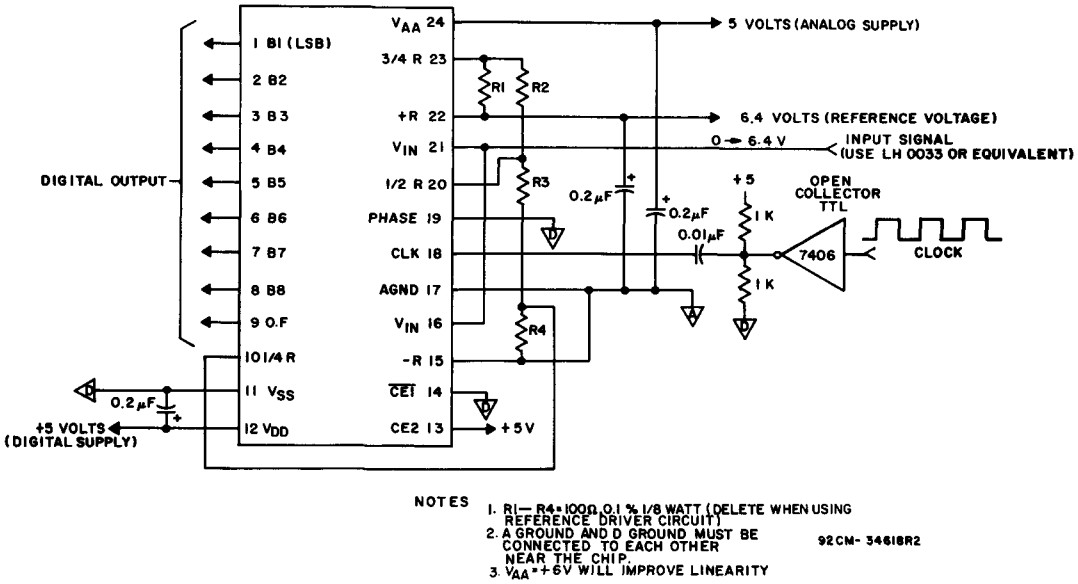


Fig. 3-Typical circuit configuration for the CA3308. (15-MHz sampling rate)

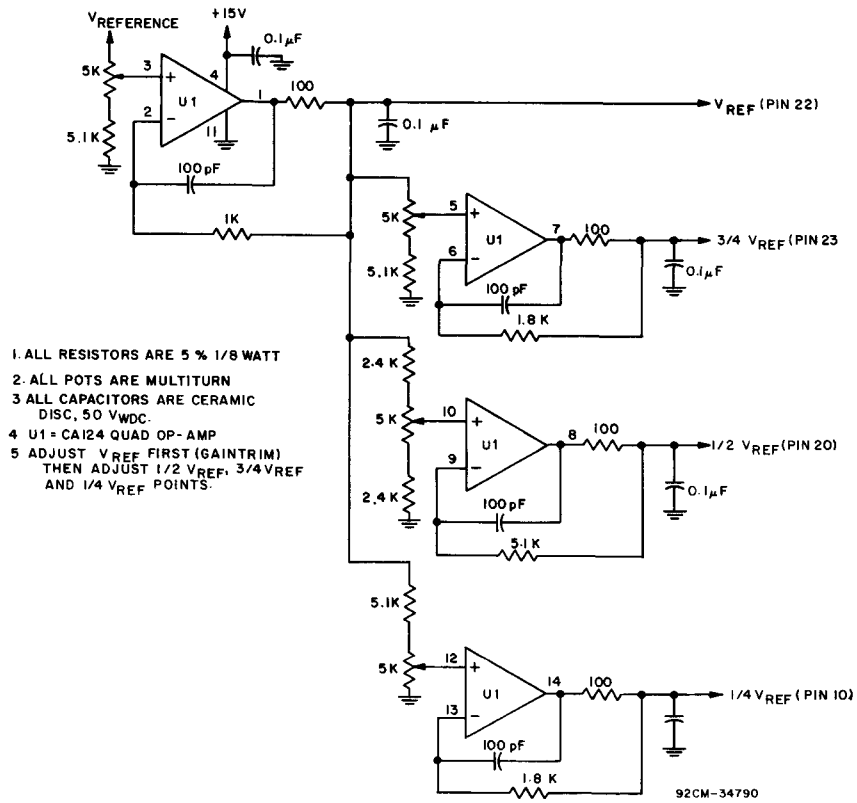


Fig. 4-Reference driver circuit. (Use for maximum linearity)

Device Operation

A sequential parallel technique is used by the CA3308 converter to obtain its high-speed operation. The sequence consists of the "Auto Balance" phase, Ø1, and the "Sample Unknown" phase Ø2. (Refer to the circuit diagram.) Each conversion takes one clock cycle.* With the phase control (pin 8) high, the "Auto Balance" (Ø1) occurs during the High period of the clock cycle, and the "Sample Unknown" (Ø2) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, a transmission switch is used to connect each of the first set of 256 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{tap}(N)=[(N/256)\,V_{REF}]-[(1/512)\,V_{REF}]$$
$$=[(2N-1/512]V_{REF}$$

Where:

V_{tap} (n)=reference ladder tap voltage at point n.

V_{REF}=voltage across −REF to +REF

N=tap number (1 through 256)

The other side of these capacitors are connected to single stage amplifiers whose outputs are shorted to their inputs by switches. This balances the amplifiers at their intrinsic trip points, which is approximately, $V_{DD}-V_{SS}/2$. The first set of capacitors now charge tc their associated tap voltages.

At the same time a second set of commutating capacitors and amplifiers are also auto-balanced. The balancing of the second stage amplifier at its intrinsic trip point removes any tracking differences between the first and second amplifier stages. The cascaded auto-balance (CAB) technique, used here, increases comparator sensitivity and temperature tracking.

In the "Sample Unknown" phase, all ladder tap switches and comparator shorting switches are opened. At the same time V_{in} is switched to the first set of commutating capacitors. Since the other end of the capacitors are now looking into an effectively open circuit, any input voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators that had tap voltages greater than V_{in} will go to a "low" state at their outputs. All comparators that had tap voltages lower than V_{in} will go to a "high" state.

The status of all these comparator amplifiers are ac coupled through the second stage comparator and stored at the end of this phase (Ø2), by a latching amplifier stage. Once latched, the status of the comparators are decoded by a 256 to 9-bit decode array and the results are clocked into a storage register at the rising edge of the next Ø2.

A 3-state buffer is used at the output of the 9 storage registers which are controlled by two chip-enable signals. CE1 will independently disable B1 through B8 when it is in a high state. CE2 will independently disable B1 through B8 and the OF buffers when it is in the low state.

To facilitate usage of this device a phase control input is provided which can effectively complement the clock as it enters the chip.

Continuous Clock Operation

One complete conversion cycle can be traced through the CA3308 via the following steps. (Refer to timing diagram No. 1.) With the phase control in a "low" state, the rising edge of the clock input will start a "sample" phase. During this entire "high" state of the clock, the comparators will track the input voltage and the latches will track the comparator outputs. At the falling edge of the clock, all 256 comparator outputs are captured by the 256 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this "low" state of the clock the output of the latches propagates through the decode array and a 9-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 9-bit code is shifted into the output registers and appears with time delay t_d as valid data at the output of the 3-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

*This device requires only a single phase clock. The terminology of 01 and 02 refers to the High and Low periods of the same clock.

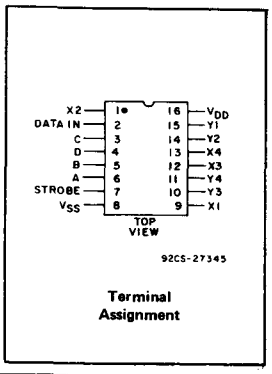
CMOS 4 x 4 Crosspoint Switch with Control Memory

High-Voltage Types (20-Volt Rating)

The RCA-CD22100 combines a 4 x 4 array of crosspoints (transmission gates) with a 4-line-to-16-line decoder and 16 latch circuits. Any one of the sixteen transmission gates (crosspoints) can be selected by applying the appropriate four line address. The selected transmission gate can be turned on or off by applying a logical one or zero, respectively, to the data input and strobing the strobe input to a logical one. Any number of the transmission gates can be ON simultaneously. When the required operating power is applied to the CD22100, the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high and data-in low, and then addressing all switches in succession.

Features:

- **Low ON resistance — 75 Ω typ. at V_{DD} = 12 V**
- **"Built-in" control latches**
- **Large analog signal capability — ± $V_{DD}/2$**
- **10-MHz switch bandwidth**
- **Matched switch characteristics ΔR_{ON} = 18Ω typ. at V_{DD} = 12 V**
- **High linearity — 0.5% distortion (typ.) at f = 1 kHz, V_{IN} = 5 V_{p-p}, V_{DD} = 10 V, and R_L = 1 kΩ**
- **Standard CMOS noise immunity**
- **100% tested for maximum quiescent current at 20 V**



Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT*	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER TRANSMISSION GATE	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

* Maximum current through transmission gates (switches) = 25 mA.

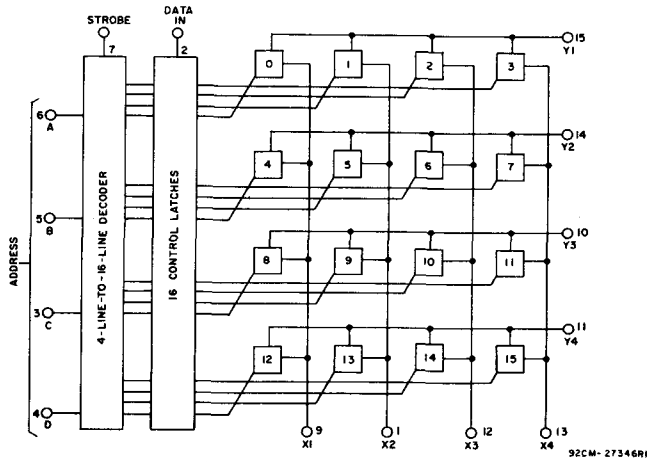


Fig. 1 — Functional diagram.

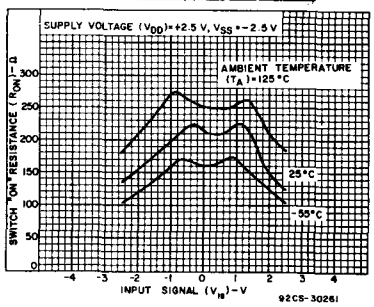


Fig. 2— Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS}$ = 2.5 V.

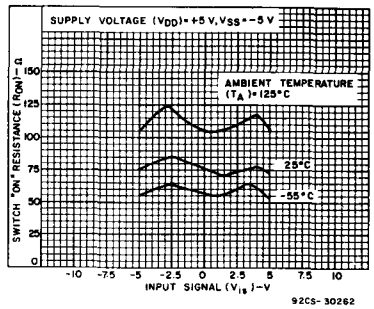


Fig. 3— Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS}$ = 5 V.

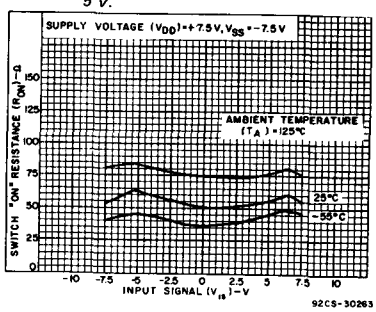


Fig. 4 — Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS}$ = 7.5 V.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V

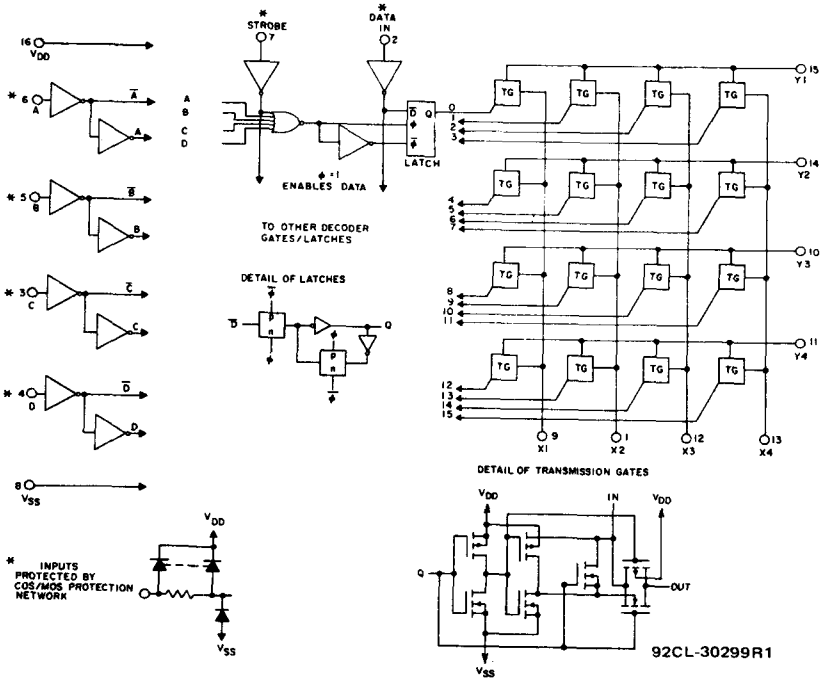


Fig. 6— Schematic diagram.

TRUTH TABLE								
Address				Select	Address				Select
A	B	C	D		A	B	C	D	
0	0	0	0	X1Y1	0	0	0	1	X1Y3
1	0	0	0	X2Y1	1	0	0	1	X2Y3
0	1	0	0	X3Y1	0	1	0	1	X3Y3
1	1	0	0	X4Y1	1	1	0	1	X4Y3
0	0	1	0	X1Y2	0	0	1	1	X1Y4
1	0	1	0	X2Y2	1	0	1	1	X2Y4
0	1	1	0	X3Y2	0	1	1	1	X3Y4
1	1	1	0	X4Y2	1	1	1	1	X4Y4

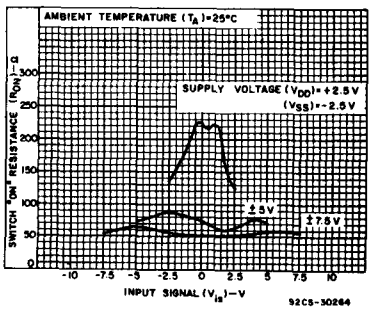


Fig. 5— Typical ON resistance as a function of input signal voltage at T_A = 25°C.

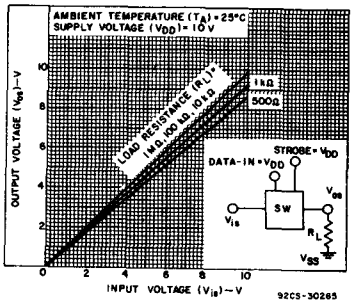


Fig. 7 — Typical switch ON transfer characteristics (1 of 16 switches).

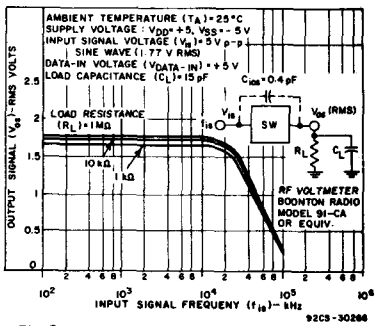


Fig. 8 — Typical switch ON frequency response characteristics.

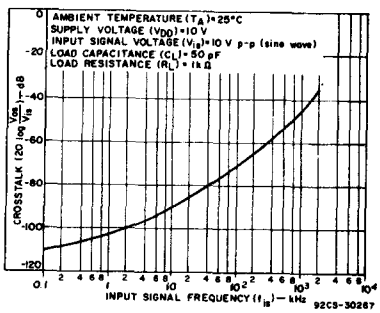


Fig. 9 — Typical crosstalk between switches as a function of signal frequency.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at −55,+25,+125,apply to D,F,H pkg Values at −40,+25,+85,apply to E pkg							Units
		V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
CROSSPOINTS											
Quiescent Device Current, I_{DD} Max.		–	5	5	5	150	150	–	0.04	5	μA
		–	10	10	10	300	300	–	0.04	10	
		–	15	20	20	600	600	–	0.04	20	
		–	20	100	100	3000	3000	–	0.08	100	
ON Resistance R_{ON} Max.	Any Switch V_{IS} = 0 to V_{DD}	–	5	475	500	725	800	–	225	600	Ω
		–	10	135	145	205	230	–	85	180	
		–	12	100	110	155	175	–	75	135	
		–	15	70	75	110	125	–	65	95	
ΔON Resistance, ΔR_{ON}	Between any two switches	–	5	–	–	–	–	–	25	–	Ω
		–	10	–	–	–	–	–	10	–	
		–	12	–	–	–	–	–	8	–	
		–	15	–	–	–	–	–	5	–	
OFF Switch Leakage Current I_L Max.	All switches OFF	0,18	18	±100		±1000		–	±1	±100*	nA
CONTROLS											
Input Low Voltage V_{IL} Max.	OFF switch I_L <0.2 μA	–	5	1.5				–	–	1.5	V
		–	10	3				–	–	3	
		–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	ON switch see R_{ON} characteristic	–	5	3.5				3.5	–	–	
		–	10	7				7	–	–	
		–	15	11				11	–	–	
Input Current, I_{IN} Max.	Any control	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

* Determined by minimum feasible leakage measurement for automatic testing.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	CONDITIONS				LIMITS			UNITS
	f_{is} kHz	R_L kΩ	V_{is}* (V)	V_{DD} (V)	Min.	Typ.	Max.	
CROSSPOINTS								
Propagation Delay Time, (Switch ON) Signal Input to Output, t_{PHL}, t_{PLH}	–	10	5	5	–	30	60	ns
			10	10	–	15	30	
			15	15	–	10	20	
	C_L = 50 pF; t_r, t_f = 20 ns							
Frequency Response, (Any Switch ON)	1	1	5	10	–	40	–	MHz
	Sine wave input, $20 \log \frac{V_{os}}{V_{is}} = -3$ dB							
Sine Wave Response, (Distortion)	1	1	5	10	–	0.5	–	%
Feedthrough (All Switches OFF)	1.6	1	5	10	–	−80	–	dB
	Sine wave input							

*Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$

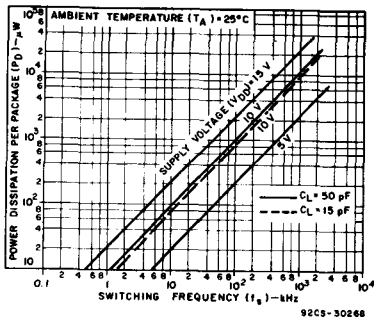


Fig. 10 – Typical dynamic power dissipation as a function of switching frequency.

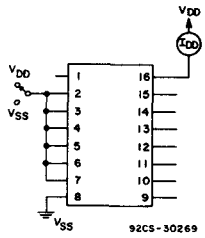


Fig. 11 – Quiescent current test circuit.

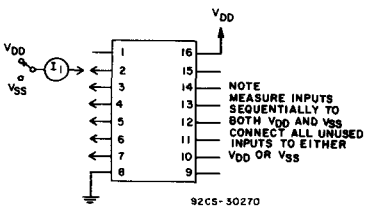


Fig. 12 – Input current test circuit.

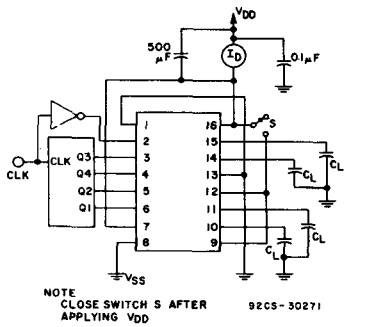


Fig. 13 – Dynamic power dissipation test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	CONDITIONS				LIMITS			UNITS
	f_{is} kHz	R_L kΩ	V_{is}● (V)	V_{DD} (V)	Min.	Typ.	Max.	
CROSSPOINTS (CONT'D)								
Frequency for Signal Crosstalk Attenuation of 40 dB	–	1	10	10	–	1.5	–	MHz
Attenuation of 110 dB	Sine wave input					0.1		kHz
Capacitance, X_n to Ground		–	–	5-15	–	18	–	pF
Y_n to Ground		–	–	5-15	–	30	–	
Feedthrough		–	–	–	–	0.4	–	
CONTROLS			See Fig.					
Propagation Delay Time: Strobe to Output, t_{PZH} (Switch Turn-ON to High Level)	R_L=1kΩ, C_L=50pF, t_r,t_f = 20 ns		18	5	–	300	600	ns
				10	–	125	250	
				15	–	80	160	
Data-In to Output, t_{PZH} (Turn-On to High Level)			19	5	–	110	220	
				10	–	40	80	
				15	–	25	50	
Address to Output, t_{PZH} (Turn-ON to High Level)			20	5	–	350	700	
				10	–	135	270	
				15	–	90	180	
Propagation Delay Time: Strobe to Output, t_{PHZ} (Switch Turn-OFF)			18	5	–	165	330	
				10	–	85	170	
				15	–	70	140	
Data-In to Output, t_{PZL} (Turn-ON to Low Level)			19	5	–	210	420	
				10	–	110	220	
				15	–	100	200	
Address to Output, t_{PHZ} (Turn-OFF)			20	5	–	435	870	
				10	–	210	420	
				15	–	160	320	
Minimum Setup Time, Data-In to Strobe, Address, t_{SU}				5	–	95	190	ns
				10	–	25	50	
				15	–	15	30	
Minimum Hold Time, Data-In to Strobe, Address, t_H				5	–	180	360	ns
				10	–	110	220	
				15	–	35	70	
Maximum Switching Frequency, f_ϕ	R_L=1kΩ, C_L=50 pF t_r, t_f = 20 ns			5	0.6	1.2	–	MHz
				10	1.6	3.2	–	
				15	2.5	5	–	
Minimum Strobe Pulse Width, t_W				5	–	300	600	ns
				10	–	120	240	
				15	–	90	180	
Control Crosstalk, Data-In, Address, or Strobe to Output	–	10	10	10	–	75	–	mV (peak)
	Square wave input t_r, t_f = 20 ns							
Input Capacitance, C_{IN}	Any Control Input			–	–	5	7.5	pF

● Peak-to-peak voltage symmetrical about $\frac{V_{DD}}{2}$

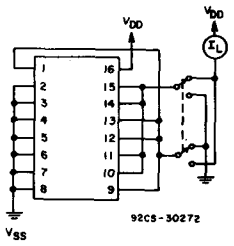


Fig. 14 – OFF switch input or output leakage current test circuit.

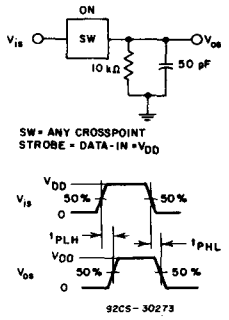


Fig. 15 – Propagation delay time test circuit and waveforms (signal input to signal output, switch ON).

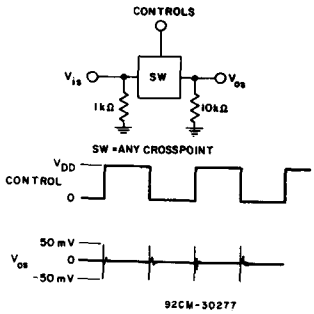


Fig. 16– Test circuit and waveforms for crosstalk (control input to signal output).

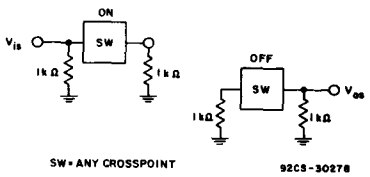


Fig. 17 – Test circuit for crosstalk between switch circuits in the same package.

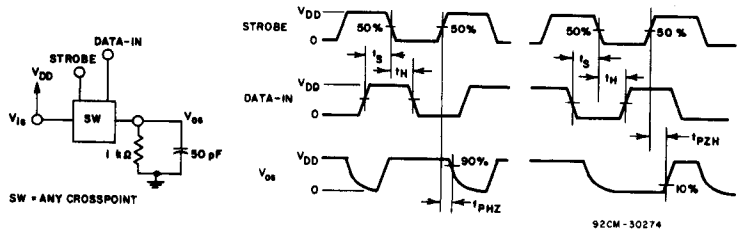


Fig. 18 — Propagation delay time test circuit and waveforms (strobe to signal output, switch Turn-ON or Turn-OFF).

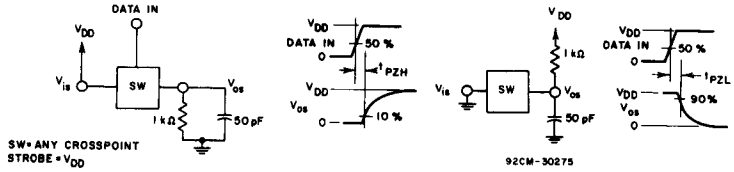


Fig. 19 — Propagation delay time test circuit and waveforms (data-in to signal output, switch Turn-ON to high or low level).

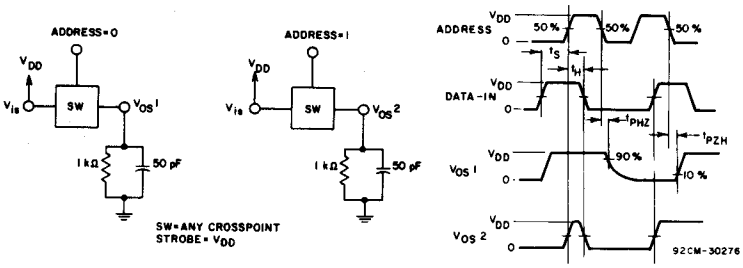
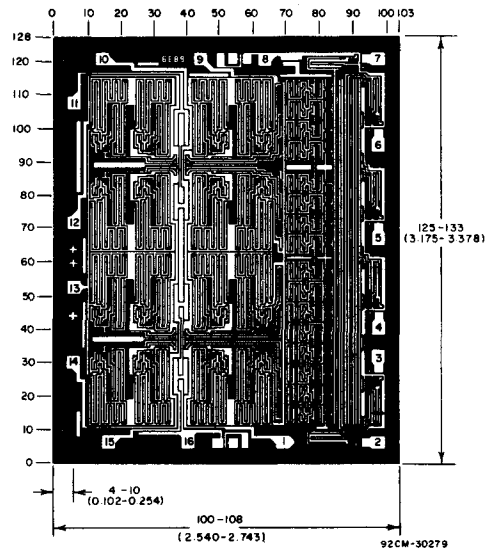


Fig. 20 — Propagation delay time test circuit and waveforms (address to signal output, switch Turn-On or Turn-OFF).



Dimensions and pad layout for CD22100H.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

CMOS 4 x 4 x 2 Crosspoint Switches With Control Memory

The RCA-CD22101 and CD22102 crosspoint switches consist of 4 x 4 x 2 arrays of crosspoints (transmission gates), 4-line to 16-line decoders, and 16 latch circuits. Any one of the sixteen crosspoint pairs can be selected by applying the appropriate four-line address, and any number of crosspoints can be *ON simultaneously*. *Corresponding* crosspoints in each array are turned on and off simultaneously, also.

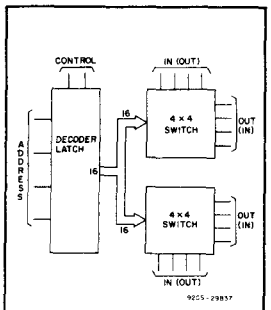
In the CD22101, the selected crosspoint pair can be turned on or off by applying a logical ONE or ZERO, respectively, to the data input, and applying a ONE to the strobe input. When the device is "powered up", the states of the 16 switches are indeterminate. Therefore, all switches must be turned off by putting the strobe high, data-in low, and then addressing all switches in succession.

The selected pair of crosspoints in the CD22102 is turned on by applying a logical ONE to the K_a (set) input while a logical ZERO is on the K_b input, and turned off by applying a logical ONE to the K_b (reset) input while a logical ZERO is on the K_a input. In this respect, the control latches of the CD22102 are similar to SET/RESET flip-flops. They differ, however, in that the simultaneous application of ONEs to the K_a and K_b inputs turns off (resets) all crosspoints. All crosspoints in both devices must be turned off as V_{DD} is applied.

The CD22101 and CD22102 types are supplied in 24-lead hermetic dual-in-line ceramic packages (D and F suffixes), 24-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

Features:

- **Low ON resistance — 75 Ω typ. at V_{DD} = 12 V**
- **"Built-in" latched inputs**
- **Large analog signal capability — ± V_{DD}/2**
- **10 MHz switch bandwidth**
- **Matched switch characteristics ΔR_{ON} = 8 Ω typ. at V_{DD} = 12 V**
- **High linearity — 0.25% distortion (typ.) at f = 1 kHz, V_{IN} = 5 V_{p-p}, $V_{DD} - V_{SS}$ = 10 V, and R_l = 1 kΩ**
- **Standard CMOS noise immunity**



CD22101, CD22102 Functional Diagram

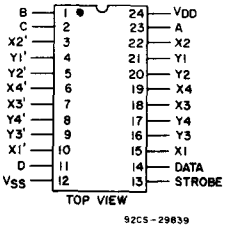
Applications:

- **Telephone systems**
- **PBX**
- **Studio audio switching**
- **Multisystem bus interconnect**

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT*	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D,F)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

* Maximum current through transmission gates (switches) = 25 mA.

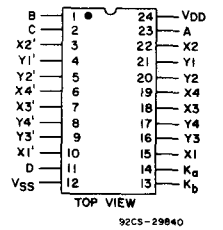


CD22101 Terminal Diagram

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	3	18	V



CD22102 Terminal Diagram

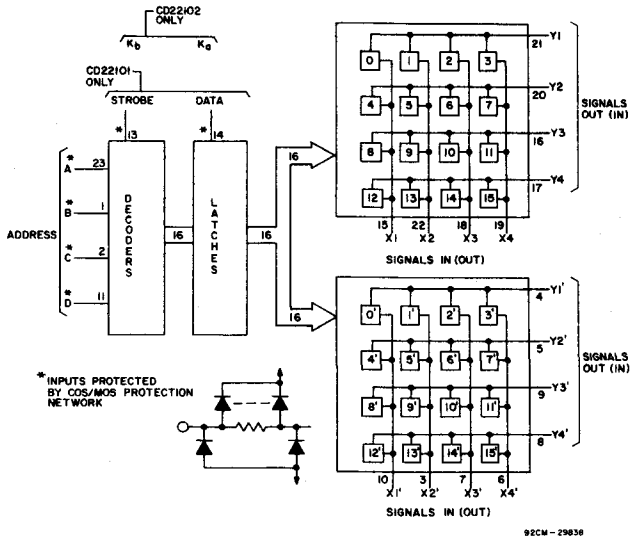


Fig. 1 – Functional block diagram.

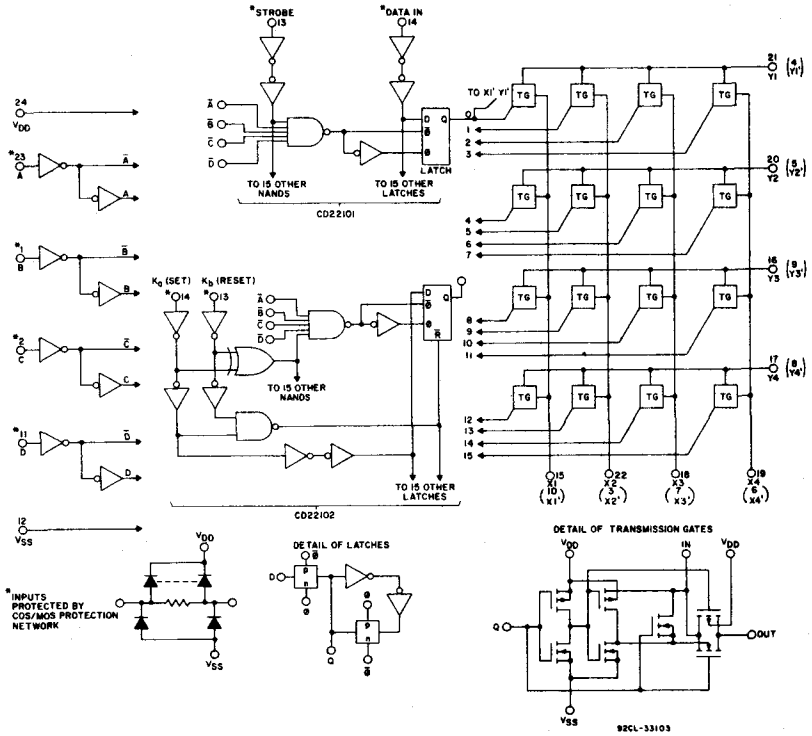


Fig. 2 – Logic diagram.

DECODER TRUTH TABLE

Address				Select	Address				Select
A	B	C	D		A	B	C	D	
0	0	0	0	X1Y1 & X1′Y1′	0	0	0	1	X1Y3 & X1′Y3′
1	0	0	0	X2Y1 & X2′Y1′	1	0	0	1	X2Y3 & X2′Y3′
0	1	0	0	X3Y1 & X3′Y1′	0	1	0	1	X3Y3 & X3′Y3′
1	1	0	0	X4Y1 & X4′Y1′	1	1	0	1	X4Y3 & X4′Y3′
0	0	1	0	X1Y2 & X1′Y2′	0	0	1	1	X1Y4 & X1′Y4′
1	0	1	0	X2Y2 & X2′Y2′	1	0	1	1	X2Y4 & X2′Y4′
0	1	1	0	X3Y2 & X3′Y2′	0	1	1	1	X3Y4 & X3′Y4′
1	1	1	0	X4Y2 & X4′Y2′	1	1	1	1	X4Y4 & X4′Y4′

CONTROL TRUTH TABLE FOR CD22101

Function	Address				Strobe	Data	Select
	A	B	C	D			
Switch On	1	1	1	1	1	1	15 (X4Y4) & 15′ (X4′Y4′)
Switch Off	1	1	1	1	1	0	15 (X4Y4) & 15′ (X4′Y4′)
No Change	X	X	X	X	0	X	X X X X

1 = High Level; 0 = Low Level; X = Don't Care

CONTROL TRUTH TABLE FOR CD22102

Function	Address				K_a	K_b	Select
	A	B	C	D			
Switch On	1	1	1	1	1	0	15 (X4Y4) & 15′ (X4′Y4′)
Switch Off	1	1	1	1	0	1	15 (X4Y4) & 15′ (X4′Y4′)
All Switches Off#	X	X	X	X	1	1	All
No Change	X	X	X	X	0	0	X X X X

1 = High Level; 0 = Low Level; X = Don't Care

In the event that K_a and K_b are changed from levels 1,1 to 0,0 K_b should not be allowed to go to 0 before K_a, otherwise a switch which was off will inadvertently be turned on.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS at Indicated Temperature (°C) Values at −55,+25,+125,apply to D,F,H pkg Values at −40,+25,+85,apply to E pkg							Units
		V_{IS} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
CROSSPOINTS											
Quiescent Device Current, I_{DD} Max.		–	5	5	5	150	150	–	0.04	5	μA
		–	10	10	10	300	300	–	0.04	10	
		–	15	20	20	600	600	–	0.04	20	
		–	20	100	100	3000	3000	–	0.08	100	
ON Resistance R_{ON} Max.	Any Switch V_{IS} = 0 to V_{DD}	–	5	475	500	725	800	–	225	600	Ω
		–	10	135	145	205	230	–	85	180	
		–	12	100	110	155	175	–	75	135	
		–	15	70	75	110	125	–	65	95	
ΔON Resistance, ΔR_{ON}	Between any two switches	–	5	–	–	–	–	–	25	–	Ω
		–	10	–	–	–	–	–	10	–	
		–	12	–	–	–	–	–	8	–	
		–	15	–	–	–	–	–	5	–	
OFF Leakage Current I_L Max.	All switches OFF	0,18	18	±1000				–	±1	±100*	nA
CONTROLS											
Input Low Voltage V_{IL} Max.	OFF switch I_L <0.2 μA;	–	5	1.5				–	–	1.5	V
		–	10	3				–	–	3	
		–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	ON switch see R_{ON} characteristic	–	5	3.5				3.5	–	–	
		–	10	7				7	–	–	
		–	15	11				11	–	–	
Input Current, I_{IN} Max.	Any control	0,18	18	±0.1	±0.1	±1	±1	–	$\pm 10^{-5}$	±0.1	μA

* Determined by minimum feasible leakage measurement for automatic testing.

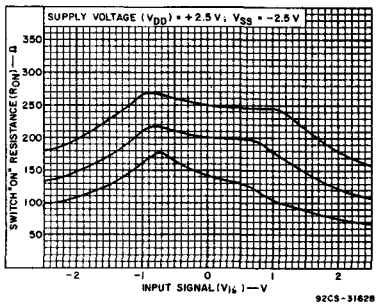


Fig. 3 – Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS} = 2.5$ V.

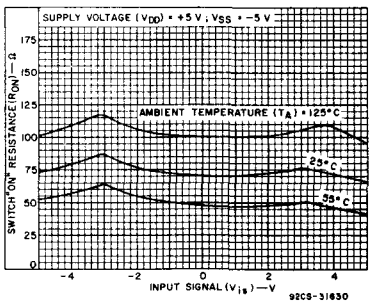


Fig. 4 – Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS} = 5$ V.

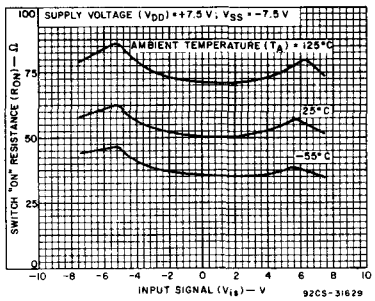


Fig. 5 – Typical ON resistance as a function of input signal voltage at $V_{DD} = -V_{SS} = 7.5$ V.

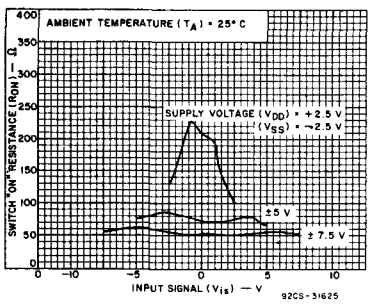


Fig. 6 – Typical ON resistance as a function of input signal voltage at $T_A = 25°C$.

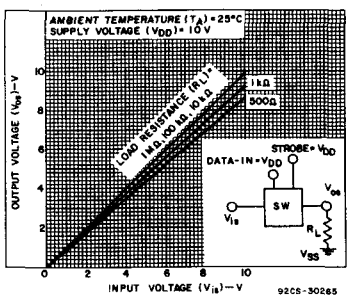


Fig. 7 – Typical switch ON transfer characteristics (1 of 16 switches).

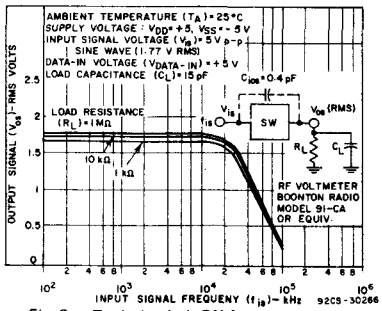


Fig. 8 – Typical switch ON frequency response characteristics.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	CONDITIONS f_{is} kHz	R_L kΩ	V_{is}● (V)	V_{DD} (V)	LIMITS Min.	Typ.	Max.	UNITS
CROSSPOINTS								
Propagation Delay Time, (Switch ON) Signal Input to Output, t_{PHL}, t_{PLH}	–	10	5	5	–	30	60	ns
			10	10	–	15	30	
			15	15	–	10	20	
	C_L = 50 pF; t_r, t_f = 20 ns							
Frequency Response, (Any Switch ON)	1	1	5	10	–	40	–	MHz
	Sine wave input, $20 \log \frac{V_{os}}{V_{is}} = -3$ dB							
Sine Wave Response, (Distortion	1	1	2.5	5	–	1	–	%
	1	1	5	10	–	0.25	–	
	1	1	7.5	15	–	0.15	–	
Feedthrough All Switches OFF (See Fig. 24)	1.6	0.6	2■	10	–	–96	–	dB
	Sine wave input							
Frequency for Signal Crosstalk Attenuation of 40 dB	–	0.6	1■	10	–	2.5	–	MHz
Attenuation of 95 dB (See Fig. 23)	Sine wave input					0.1		kHz
Capacitance, X_n to Ground		–	–	–	–	25	–	pF
Y_n to Ground		–	–	–	–	60	–	
Feedthrough		–	–	–	–	0.6	–	
CONTROLS			See Fig.					
Propagation Delay Time, High Impedance to High Level or Low Level, t_{PZH}, t_{PZL} Strobe to Output, CD22101	R_L = 1 kΩ, C_L = 50 pF, t_r, t_f = 20 ns		16	5	–	500	1000	ns
				10	–	230	460	
				15	–	170	340	
Data-In to Output, CD22101			17	5	–	515	1000	
				10	–	220	440	
				15	–	170	340	
K_a to Output, CD22102				5	–	500	1000	
				10	–	215	430	
				15	–	160	320	
Address to Output, CD22101, CD22102			18	5	–	480	960	
				10	–	225	450	
				15	–	155	300	
Propagation Delay Time, High Level or Low Level to High Impedance, t_{PHZ}, t_{PLZ} Strobe to Output, CD22101			16	5	–	450	900	
				10	–	200	400	
				15	–	135	270	
K_b to Output, CD22102				5	–	450	900	
				10	–	200	400	
				15	–	130	260	
Data-In to Output, CD22101				5	–	450	900	
				10	–	165	330	
				15	–	110	220	
K_a·K_b to Output, CD22102				5	–	280	560	
				10	–	130	260	
				15	–	90	180	

● Peak-to-peak voltage symmetrical about V_{DD} unless otherwise specified. ■ RMS

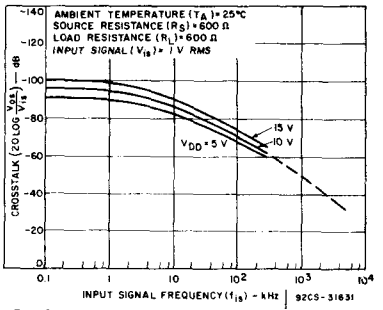


Fig. 9 — Typical crosstalk between switches as a function of signal frequency.

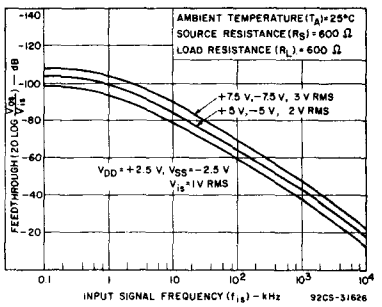


Fig. 10 — Typical feedthrough, any OFF switch as a function of frequency.

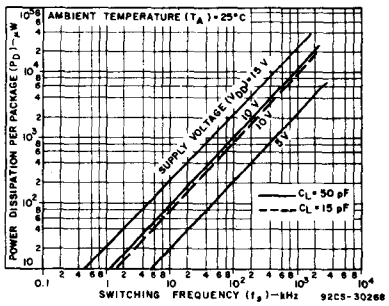


Fig. 11 — Typical dynamic power dissipation as a function of switching frequency for CD22101.

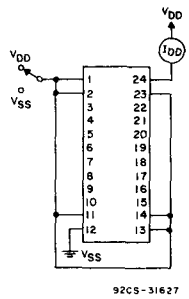


Fig. 12 — Quiescent current test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C (cont'd)

CHARACTERISTIC	CONDITIONS				LIMITS			UNITS
	f_{is} kHz	R_L kΩ	V_{is}● (V)	V_{DD} (V)	Min.	Typ.	Max.	
CONTROLS (cont'd)			See Fig.					
Address to Output, CD22101, CD22102	R_L = 1 k, C_L = 50 pF, t_r,t_f = 20 ns		18	5	–	425	850	ns
				10	–	190	380	
				15	–	130	260	
Minimum Strobe Pulse Width t_W CD22101				5	–	260	500	
				10	–	120	240	
				15	–	80	160	
Address to Strobe Setup or Hold Times, t_{SU}, t_h, CD22101			19	5	–	−160	0	
				10	–	−70	0	
				15	–	−50	0	
Strobe to Data-In Hold Time, Time, t_{HL}; t_{LH}, CD22101			20	5	–	200	400	
				10	–	80	160	
				15	–	60	120	
Address to K_a and K_b Setup or Hold Times, t_{SU}, t_H, CD22102				5	–	−160	0	
				10	–	−70	0	
				15	–	−50	0	
Minimum K_a*K_b Pulse Width, t_W CD22102				5	–	375	750	
				10	–	160	320	
				15	–	110	220	
Minimum K_a Pulse Width, t_W CD22102				5	–	425	850	
				10	–	175	350	
				15	–	120	240	
Minimum K_b Pulse Width, t_W CD22102				5	–	200	400	
				10	–	90	180	
				15	–	70	140	
Control Crosstalk, Data-In, Address, or Strobe to Output,	100	10	21	5	–	75	–	mv (peak)
	Square wave input = 5 V, t_r,t_f=20 ns, R_s=1kΩ							
Input Capacitance, C_{IN}	Any Control Input			–	–	5	7.5	pF

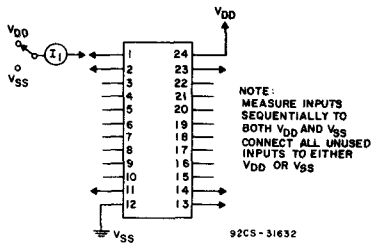


Fig. 13 – Input current test circuit.

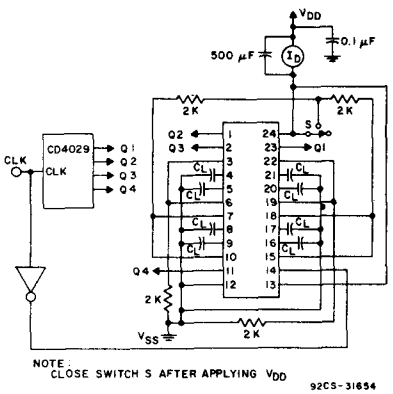


Fig. 14 – Dynamic power dissipation test circuit for CD22101.

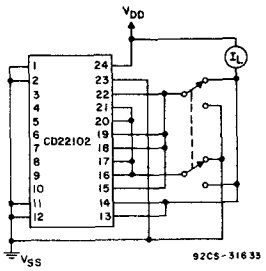


Fig. 15 – OFF switch input or output leakage current test circuit (16 of 32 switches).

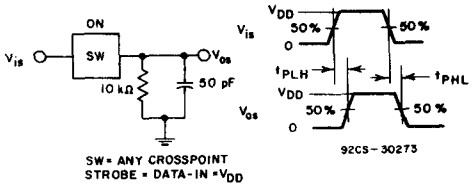


Fig. 16 – Propagation delay time test circuit and waveforms (signal input to signal output, switch ON).

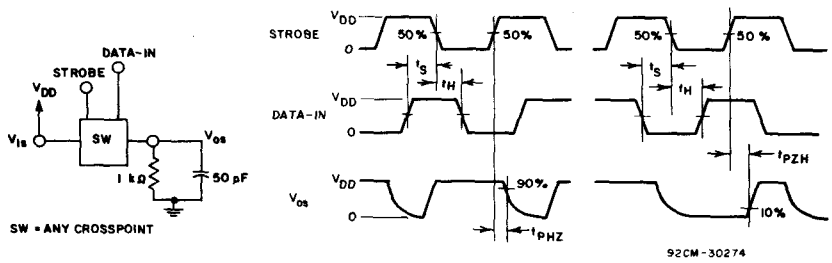


Fig. 17 – Propagation delay time test circuit and waveforms (strobe to signal output, switch Turn-ON or Turn-OFF).

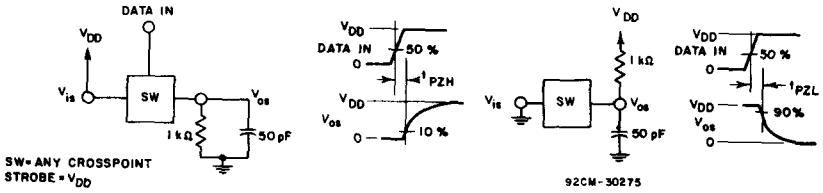


Fig. 18 – Propagation delay time test circuit and waveforms (data-in to signal output, switch Turn-ON to high or low level).

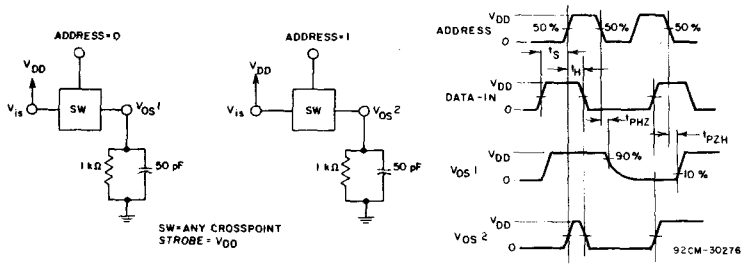


Fig. 19 – Propagation delay time test circuit and waveforms (address to signal output, switch turn-ON or Turn-OFF).

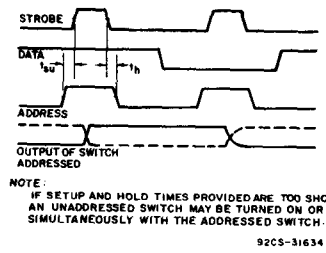


Fig. 20 – Address to strobe setup and hold times.

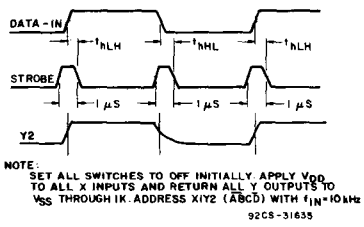


Fig. 21 – Strobe to Data-In hold time t_h, for CD22101.

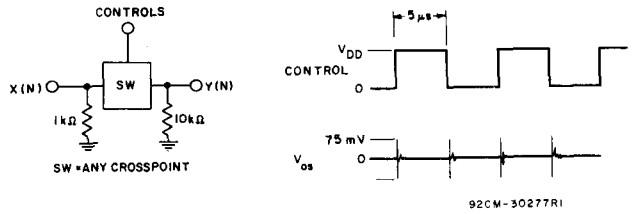


Fig. 22 – Test circuit and waveforms for crosstalk (control input to signal output).

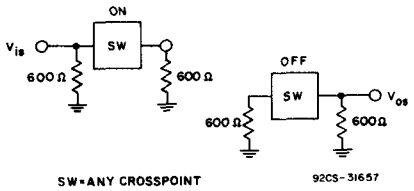


Fig. 23 – Test circuit for crosstalk between switch circuits in the same package.

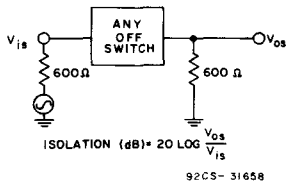
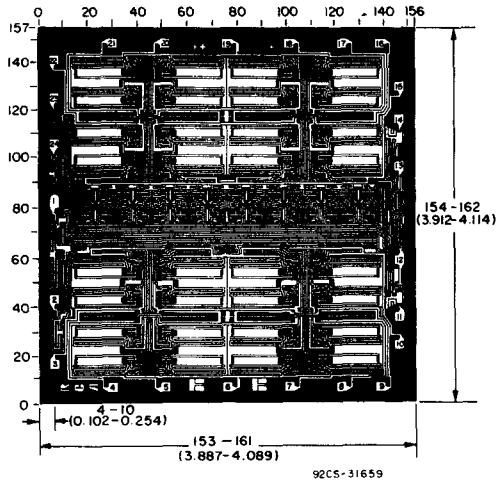
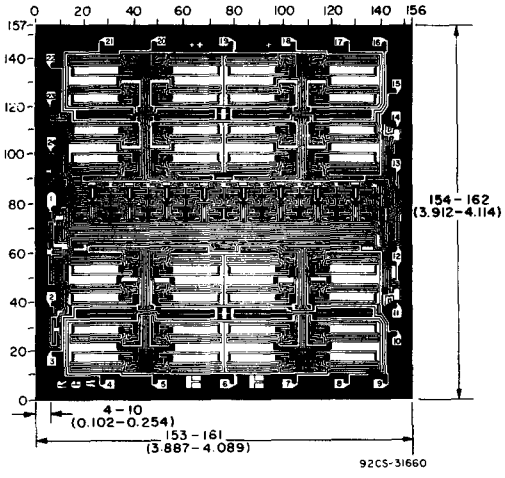


Fig. 24 – Test circuit for feedthrough (any OFF switch).



Dimensions and pad layout for CD22101H.



Dimensions and pad layout for CD22102H.

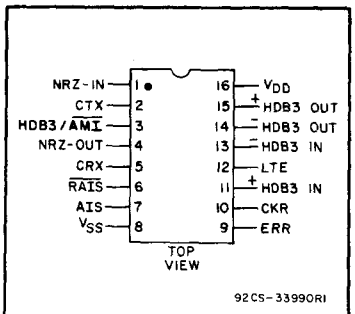
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of -3 mils to +16 mils applicable to the nominal dimensions shown.

CMOS HDB3 (High Density Bipolar 3) Transcoder for 2.048/8.448 Mb/s Transmission Applications

Features:

- *HDB3 coding and decoding for data rates from 50 Kb/s to 10 Mb/s in a manner consistent with CCITT G703 recommendations.*
- *HDB3/AMI transmission coding/reception decoding with code error detection is performed in independent coder and decoder sections.*
- *All transmitter and receiver inputs/outputs are TTL compatible.*
- *Internal Loop Test capability.*



Terminal Assignment

The RCA CD22103 is an LSI SOS integrated circuit which performs the HDB3 transmission coding and reception decoding functions with error detection. It is used in 2.048 and 8.448 Mb/s transmission applications. The CD22103 performs HDB3 coding and decoding for data rates from 50 Kb/s to 10 Mb/s in a manner consistent with CCITT G703 recommendations.

HDB3 transmission coding/reception decoding with code error detection is performed in independent code and decoder sections. All transmitter and receiver inputs/outputs are TTL compatible.

The HDB3 transmitter coder codes are NRZ binary unipolar input signal (NRZ-In) and a synchronous transmission clock (CTX) into two HDB3 binary unipolar RZ output signals (+HDB3 OUT, -HDB3 OUT). The TTL compatible output signals +HDB3 OUT, -HDB3 OUT are externally mixed to generate ternary bipolar HDB3 signals for driving transmission lines.

HDB3 reception decoding is performed on ternary bipolar HBD3 signals which have been externally split to provide binary unipolar receiver input signals, (+HDB3 IN, -HDB3 IN), and a synchronous receiver clock signal, (CRX) into binary unipolar NRZ signals (NRZ - Out).

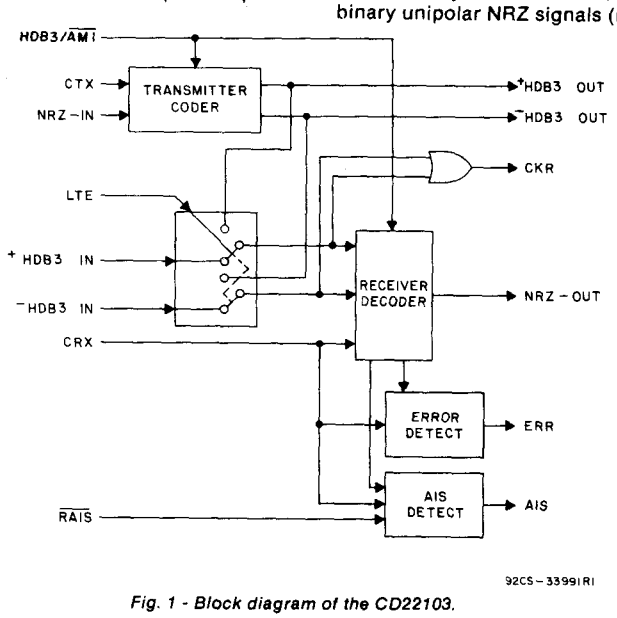


Fig. 1 - Block diagram of the CD22103.

Received signals not consistent with HDB3 coding rules are detected as errors. The receiver error output (ERR) is active high during one CRX period of each bit of received data which is inconsistent with HDB3 coding rules.

An input string consisting of all ones (or marks) is detected and signaled by a high level at the Alarm Signal (AIS) output. The AIS output is set to a high level when less than three zeros are received during two consecutive periods of the Reset Alarm Inhibit Signal (RAIS). The AIS output is subsequently reset to a low level when three or more zeros are received during two periods of the reset signal ($\overline{RAIS}$).

A diagnostic Loop-Test Mode may be entered by driving the Loop Test Enable Input (LTE) high. In this mode the HDB3 transmitter outputs (+HDB3 OUT, -HDB3 OUT) are internally connected to the HDB3 receiver inputs, and the external HDB3 receiving inputs (+HDB3 IN, -HDB3 IN) are disabled. The NRZ binary output signal (NRZ - Out) corresponds to the NRZ binary input signal (NRZ - In) delayed by approximately 8 clock periods.

The Clock Receiver Output (CKR) is the product of the two HDB3 input signals or-ed together. The CRX clock signal may be derived from the CKR signal with external clock extraction circuitry. In the Loop Test Mode (LTE = 1) CKR is the product of the +HDB3 OUT and -HDB3 OUT signals or-ed together.

The CD22103 may also be used to perform the AMI to NRZ coding/decoding function. To use the CD22103 in this mode, the HDB3/$\overline{AMI}$ control input is driven low.

The RCA CD22103 operates with a 5 V power supply voltage over the full military temperature range at data rates from 50 Kb/s up to 10 Mb/s.

The RCA CD22103 is similar in function and pin configuration to type MJ1471.

The CD22103 types are supplied in 16-lead hermetic dual-in-line ceramic packages (D suffix), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to + 8 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} + 0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ± 10 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to + 60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = + 60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/° C to 200 mW
For T_A = -55 to + 100° C (PACKAGE TYPE D) ..... 500 mW
For T_A = + 100 to + 125° C (PACKAGE TYPE D) ..... Derate Linearly at 12 mW/° C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPES D, H ..... -55 to + 125° C
PACKAGE TYPE E ..... -40 to + 85° C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to + 150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... + 265° C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
DC Supply Voltage Range	4.5	5.5	V

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		Min.	Typ.	Max.	
Quiescent Device Current	I_{DD}	—	—	100	μA
Operating Device Current f_{CL} = 10 MHz		—	—	8	mA
HDB3 Output Low (Sink) Current (V_{OL} = 0.5 V)	I_{OL1}	1.6	—	—	
HDB3 Output High (Source) Current (V_{OH} = 2.8 V)	I_{OH1}	-10	—	—	
All Other Outputs Low (Sink) Current (V_{OL} = 0.5 V)	I_{OL2}	1.6	—	—	
All Other Outputs High (Source) Current (V_{OH} = 2.8 V)	I_{OH2}	-1.6	—	—	
Input Low Current	I_{IL}	—	—	-1	μA
Input High Current	I_{IH}	—	—	1	
Input Low Voltage (Max.)	V_{IL}	—	—	0.8	V
Input High Voltage (Min.)	V_{IH}	2	—	—	
Input Capacitance	C_{IN}	—	—	5	pF

DYNAMIC ELECTRICAL CHARACTERISTICS

at T_A range of -40° C to 85° C for plastic package
-55° C to 125° C for ceramic package
V_{DD} range of 4.5 V to 5.5 V
C_L = 15 pF

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		Min.	Typ.	Max.	
INPUT					
CTX, CRX Input Frequency	f_{CTX}, f_{CRX}	.05	—	10	MHz
CTX, CRX Input Rise Time *	t_{rcl}	—	—	1	μs
Fall Time *	t_{fcl}	—	—	1	μs
NRZ-IN to CTX					
Data Setup Time *	t_s	—	—	15	ns
Data Hold Time *	t_H	—	—	15	ns
HDB3 IN to CRX					
Data Setup Time §	t_s	—	—	55	ns
Data Hold Time *	t_H	—	—	0	ns
CRX to CKR					
CRX = 8.448 MHz					
Pretrigger °	t_p	—	—	20	ns
Delay	t_d	—	—	20	ns

* See Fig. 4 § See Fig. 5 ° See Fig. 6

DYNAMIC ELECTRICAL CHARACTERISTICS

at T_A range of -40° C to 85° C for plastic package
-55° C to 125° C for ceramic package
V_{DD} range of 4.5 V to 5.5 V
C_L = 15 pF

CHARACTERISTIC	SYMBOL	LIMITS			UNITS
		Min.	Typ.	Max.	
OUTPUT					
Transmitter Coder					
CTX to HDB3 OUT:					
Data Propagation Delay Time *	tDD	—	—	90	ns
Handling Delay Time	tHD	—	4	—	clock period
HDB3 OUT Output Pulse Width *					
(Clock duty cycle = 50%)					
fCL = 2.048 MHz	tw	238	—	260	ns
fCL = 8.448 MHz	tw	53	—	65	ns
Receiver Decoder					
CRX to NRZ OUT:					
Data Propagation Delay Times §	tDD	—	—	90	ns
Handling Delay Time #	tHD	—	4	—	clock period
HDB3 IN to CKR					
HDB3 Propagation Delay Time †					
LTE = 0	tIN CKR	—	—	65	ns
LTE = 1		—	—	30	ns

§ See Fig. 5 * See Fig. 4 † See Fig. 2 # See Fig. 3

TRANSCODER OPERATION

Transmitter Coder (See Fig. 2)

The HDB3/AMI transmitter coder operates on 4 bit serial strings of NRZ binary data and a synchronous transmitter clock (CTX). NRZ binary data is serially clocked into the transmitter on the negative transition of the (CTX) clock. HDB3/AMI coding is performed on the 4 bit string, and HDB3/AMI binary output data is clocked out to the (+ HDB3 OUT, -HDB3 OUT) outputs on the positive transition of the transmitter clock (CTX) 4 clock pulses after the data appeared at the (NRZ-In) input.

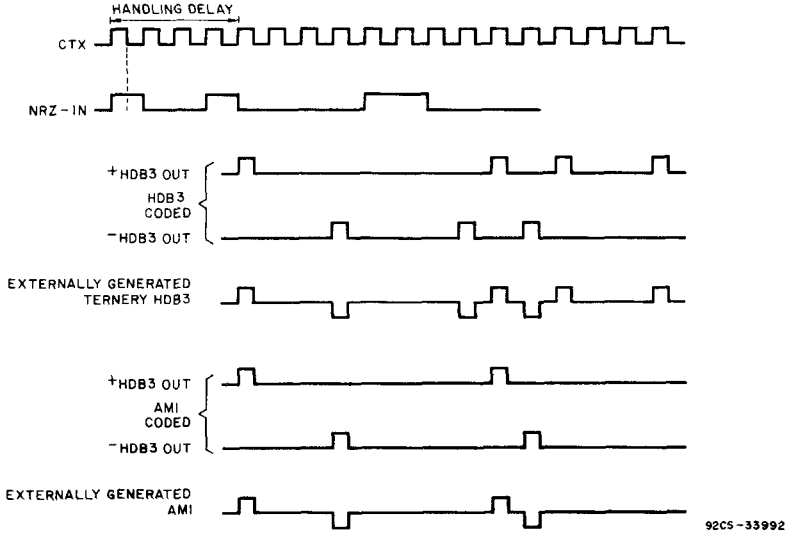


Fig. 2 - Transmitter coder operation timing waveforms - NRZ to HDB3/AMI coding.

Receiver Decoder (See Fig. 3)

The HDB3/AMI receiver decoder operates on 4 bit serial strings of binary coded HDB3/AMI signals, and a synchronous receiver clock (CRX), HDB3/AMI binary data is serially clocked into the receiver on the positive transition of the (CRX) clock. HDB3/AMI decoding is performed on the 4 bit string, and NRZ binary output data is clocked out to the (NRZ-OUT) output on the positive transition of the receiver clock (CRX) 4 clock pulses after the data appeared at the (+ HDB3 IN, -HDB3 IN) inputs.

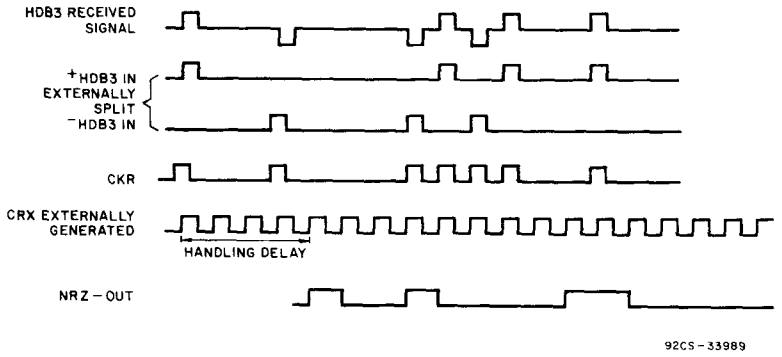


Fig. 3 - Receiver decoder operation timing waveforms - HDB3 to NRZ decoding.

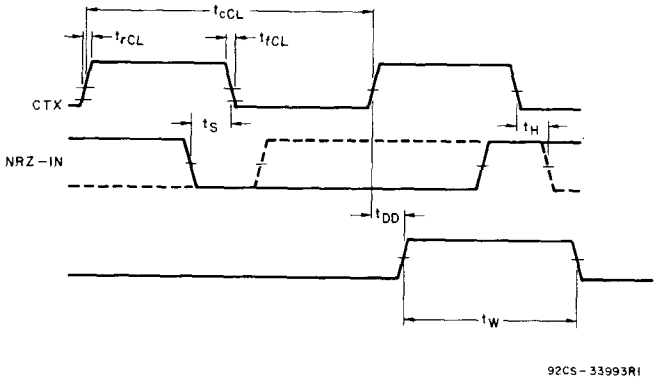


Fig. 4 - Transmitter coder timing waveforms.

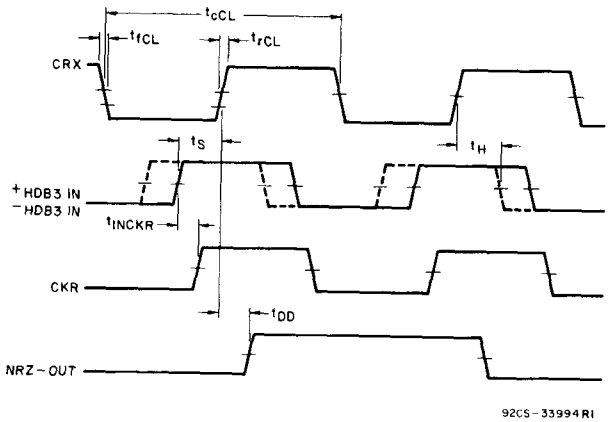


Fig. 5 - Receiver decoder timing waveforms.

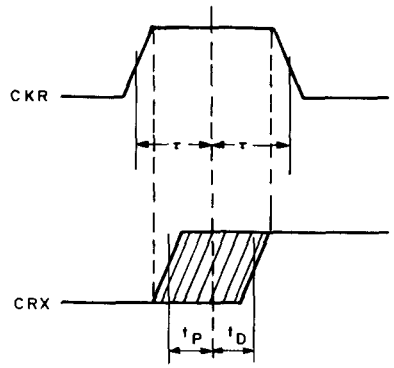


Fig. 6 - CRX Reconstruction Requirements.

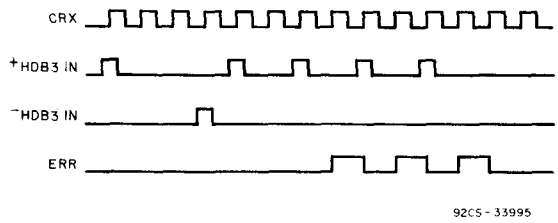


Fig. 7 - Receiver error-signals timing waveforms.

Definition of HDB3 Code Used In CD22103 HDB3 Transcoder (As Per CCITT G703 Annex Recommendations) and Error Detection

Coding of a binary signal into an HDB3 signal is done according to the following rules:

1. HDB3 signal is pseudoternary; the three states are denoted B+, B-, and 0.
2. Spaces in the binary signal are coded as spaces in the HDB3 signal. For strings of four spaces, however, special rules apply (See Item 4 below).
3. Marks in the binary signal are coded alternately as B+ and B-in the HDB3 signal (alternate mark inversion). Violations of the rule of alternate mark inversion are introduced when coding strings of four spaces (See Item 4 below).
4. Strings of four spaces in the binary signal are coded according to the following rules:

   A) The first space of a string is coded as a space if the polarity of the preceding mark of the HDB3 signal has a polarity opposite to the preceding violation and is not a violation by itself; it is coded as a mark, i.e., not a violation (i.e., B+ or B-), if the preceding mark of the HDB3 signal has the same polarity as that of the preceding violation or is by itself a violation.

   This rule ensures that successive violations are of alternate polarity so that no dc component is introduced.

   B) The second and third spaces of a string are always coded as spaces.

   C) The last space of a string of four is always coded as a mark, the polarity of which is such that it violates the rule of alternate mark inversion. Such violations are denoted V+ or V- according to their polarity.

The CD22103 is designed to code and decode HDB3 signals which are coded as binary digital signals (NRZ-In) and (+ HDB3 IN, -HDB3 IN), accompanied by sampling clocks (CTX) and (CRX). The two binary coded HDB3 outputs, (+ HDB3 OUT, -HDB3 OUT) may be externally mixed to create the ternary HDB3 signals (See Fig. 2).

The two binary HDB3 input signals have been split from the input ternary HDB3 in an external line receiver.

Error Detection

Received HDB3/AMI binary input signals are checked for coding violations, and an error signal (ERR) is generated as described below.

HDB3 Signals HDB3/$\overline{\text{AMI}}$ = High

The error signal (ERR) is flagged high for one CTX period if a violation pulse (±V) is received of the same polarity as the last received violation pulse.

A violation pulse (±V) is considered a reception error and does not cause replacement of the last string of 4 bits to zeros, if:

The received 4 data bits previous to reception of the violation pulse have not been the sequence BX00 (where X = don't care). The error signal (ERR) remains low.

NOTES:

The data sequences B000V and BB00V are valid HDB3 codings of the NRZ binary sequence 10000.

The error signal (ERR) count, is the accurate number of all single bit errors.

AMI Signals HDB3/$\overline{\text{AMI}}$ = Low

A coding error (ERR) is signaled when a violation pulse (+V) is received.

In either the HDB3 or AMI mode:
When high levels appear simultaneously on both HDB3 inputs (+ HDB3 IN, -HDB3 IN) a logical one is assumed in the HDB3/AMI input stream and the error signal (ERR) goes high.

Alarm Inhibit Signal

The alarm output (AIS) is set high if in two successive periods of the external Reset Alarm Signal, ($\overline{\text{RAIS}}$), less than three zeros are received.

The alarm output (AIS) is reset low when three or more zeros are received during two reset alarm signal periods.

CMOS Four-Digit LCD Decoder-Drivers

6-V Rating

Features
- *6-V supply-voltage rating*
- *No external components necessary*
- *4-digit segment drive capability*
- *Backplane input/output allows synchronization for cascading devices to drive more digits*
- *Decodes multiplexed binary to hexadecimal (CD22104) and decimal (CD22104A) outputs*

Applications
- *Digital meters and calculators*
- *General-purpose displays*
- *Wall and table clocks*
- *Automobile dashboard displays*
- *Appliance control panels*

H-1892

"E" Suffix

The RCA-CD22104 types are non-multiplexed, four-digit, seven-segment, liquid-crystal display decoder-drivers.

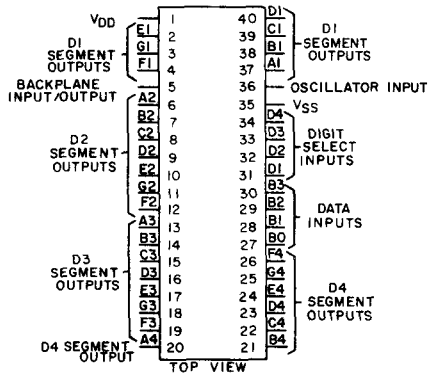
The CD22104 types contain all the circuitry necessary to drive conventional LCD displays (no external components required). Outputs are four sets of seven-segment driver signals and a backplane driver signal. The backplane signal, derived from an on-board free-running oscillator, is common to all four-digit displays.

The backplane and segment drives are designed so that p and n channels have the same ON resistances and thus equal rise and fall times. This equality eliminates any DC component, thereby maximizing display life. In addition to feeding the internal display drivers, the backplane signal can also be used as a master to drive a number of slave devices. The number of slaved devices should be limited to the load that keeps the backplane rise and fall times from exceeding 5 μs. If this limit is to be exceeded, the master backplane drivers should be disabled (by connecting pin 36, the oscillator input, to V_{SS}) and pin 5 should be fed from an external oscillator and all devices slaved to it. The maximum frequency of the external signal should be 125 Hz at room temperatures.

The on-board oscillator, which operates at 16 kHz when free-running (pin 36 floating), provides a backplane signal whose frequency is approximately 125 Hz. This frequency can be reduced by connecting an external capacitor to pin 36. Plots of backplane frequency vs. supply voltage at various values of external capacitance are shown in Fig. 3. The oscillator may be overdriven by an external signal but care must be taken to keep the lower voltage level above V_{SS} by at least 20 per cent of V_{DD} (for V_{DD}=5 V the signal should oscillate between +1 and +5 volts). This precaution prevents the backplane driver from being disabled, a condition that would present a DC component to the LCD display. A signal swinging from rail-to-rail can also be used to overdrive the oscillator but in this case the duty cycle should be such that the lower portion of the signal must be less than one-microsecond duration (the backplane disable sensing circuit will not respond to signals of this duration).

There are four data inputs and four digit-select inputs. The four-bit binary input is decoded by means of a PROM into seven-segment hexadecimal outputs for the CD22104 and into decimal seven-segment display outputs for the CD22104A. These devices are pin-compatible with the Intersil ICM7211IPL and ICM7211AIPL, respectively.

The CD22104 types are supplied in the 40-lead dual-in-line plastic (E suffix) package.



92CS-32933RI

CD22104, CD22104A
Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) ..... -0.3 to +6.5 V
(Voltages referenced to V_{SS} Terminal) ..... -0.3 to V_{DD} +0.3 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... ±10 mA
DC INPUT CURRENT, ANY ONE INPUT* .....
POWER DISSIPATION PER PACKAGE (P_D): ..... 500 mW
For T_A=-20 to +60° C ..... Derate Linearly at 12 mW/° C to 380 mW
For T_A=+60 to +70° C .....
DEVICE DISSIPATION PER OUTPUT TRANSISTOR ..... 100 mW
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE ..... -20 to +70° C
OPERATING-TEMPERATURE RANGE (T_A): ..... -55 to +125° C
STORAGE TEMPERATURE RANGE (T_{stg}) .....
LEAD TEMPERATURE (DURING SOLDERING): ..... +265° C
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. .....

*Pin 36 limited to ±5 mA.

STATIC ELECTRICAL CHARACTERISTICS
T_A=25° C, V_{DD}=5 V, V_{SS}=0 V

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Operating Supply Voltage Range	V_{DD}	V_{SS} = 0 V	3	5	6	V
Operating Current	I_{op}	Display Operating	—	10	50	μA
Oscillator Input Current	I_{OL}, I_{OH}	Pin 36	—	±2	±10	μA
Segment Rise and Fall Time	t_{rs}, t_{fs}	C_L = 200 pF	—	0.5	—	μs
Backplane Rise and Fall Time	t_{rB}, t_{fB}	C_L = 5000 pF	—	1.5	—	μs
Oscillator Frequency	f_{OSC}	Pin 36 Floating	—	16	—	kHz
Backplane Frequency	f_{BP}	Pin 36 Floating	—	125	—	Hz
Input High Voltage	V_{IH}		3.5	—	—	V
Input Low Voltage	V_{IL}		—	—	1.5	V
Input Leakage Current	I_{IL}	Pins 27-34	—	±0.01	±1	μA
Input Capacitance	C_I	Pins 27-34	—	5	—	pF
Backplane Input Leakage	$I_{IL(BP)}$	Pin 5 with Pin 36 @ V_{SS}	—	±0.01	±1	μA
Backplane Input Capacitance	$C_{I(BP)}$		—	200	—	pF

DYNAMIC ELECTRICAL CHARACTERISTICS
T_A=25° C, V_{DD}=5 V, V_{SS}=0 V

CHARACTERISTIC	SYMBOL	CONDITIONS	TYP. VALUES	UNITS
Digit-Select Active Pulse Width	t_{sa}	See Timing Diagram	0.5	μs
Data Setup Time	t_{ds}	See Timing Diagram	250	ns
Data Hold Time	t_{dh}	See Timing Diagram	100	ns
Inter-Digit Select Time	t_{ida}	See Timing Diagram	1	μs

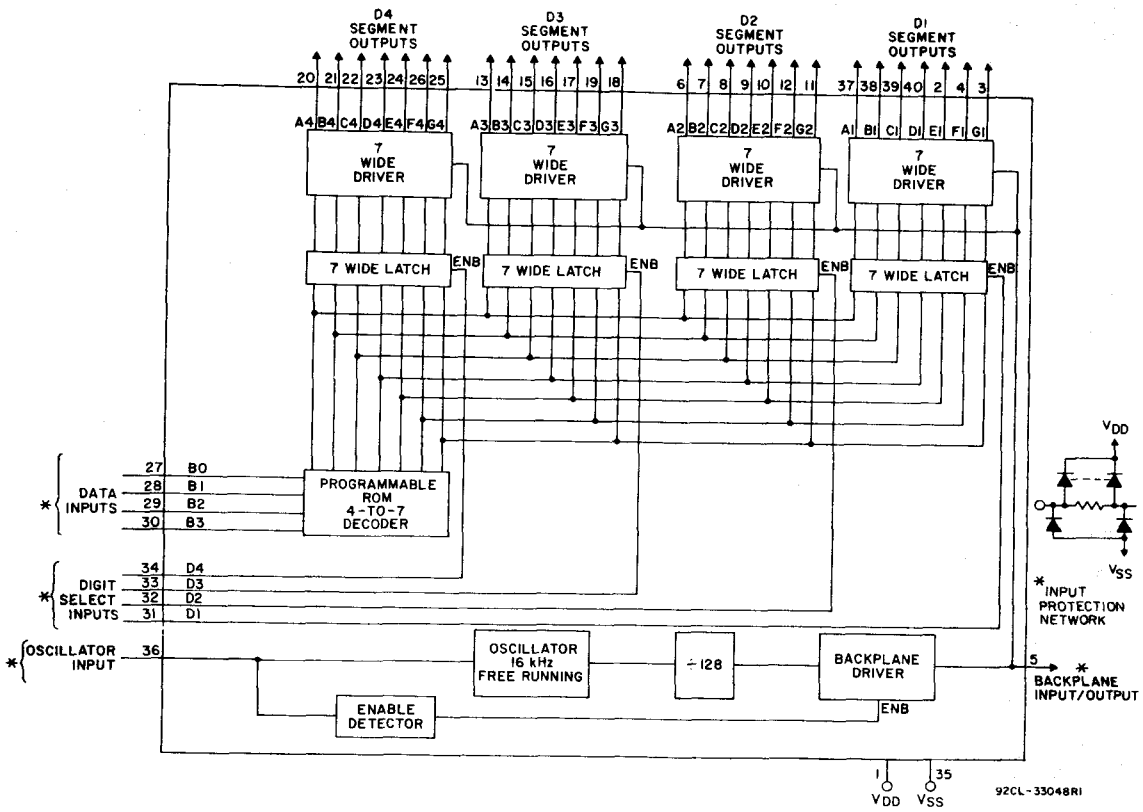


Fig. 1 - Block diagram of CD22104 and CD22104A.

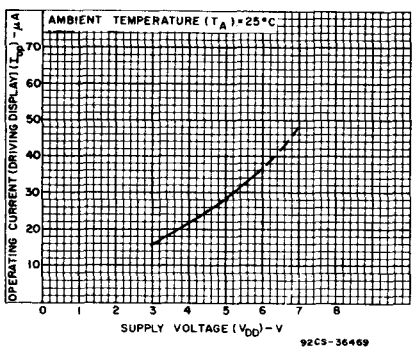


Fig. 2 - Typical operating current as a function of supply voltage.

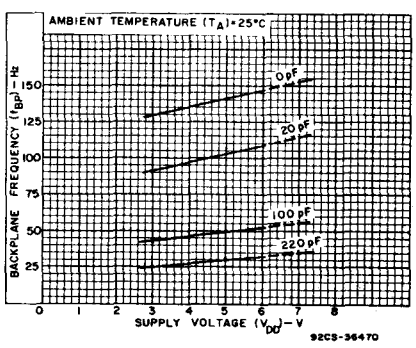


Fig. 3 - Typical backplane frequency as a function of supply voltage and external capacitance on pin 36.

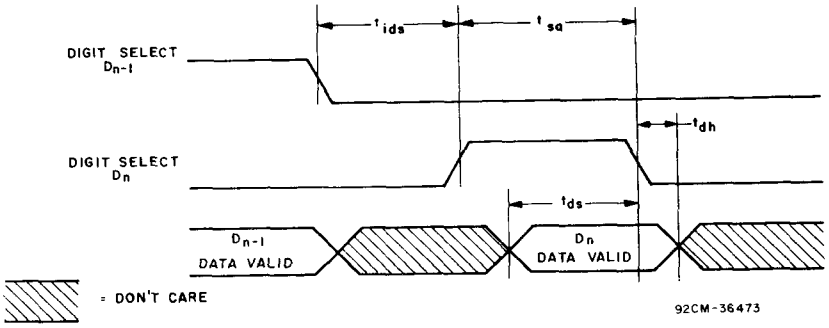


Fig. 4 - CD22104, CD22104A timing diagram.

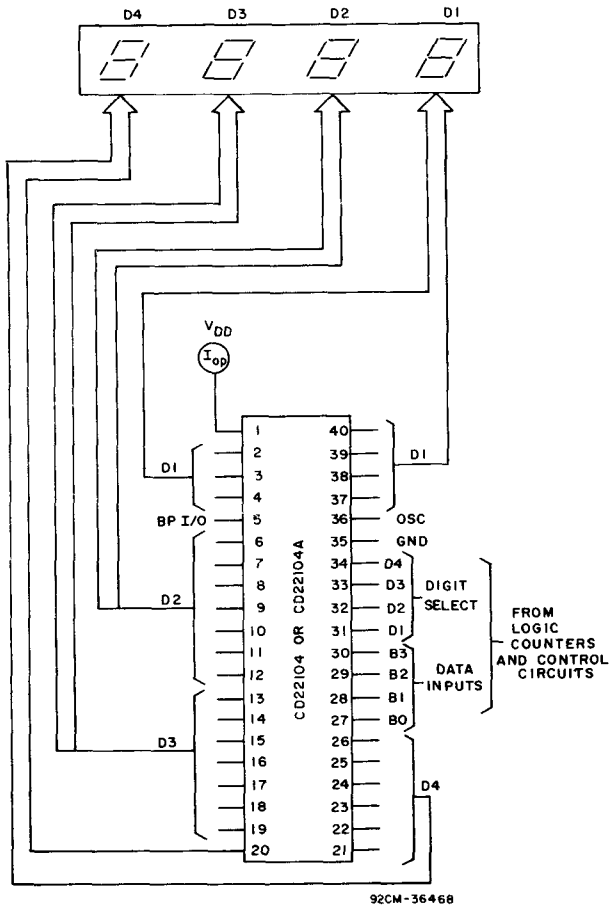


Fig. 5 - Test circuit.

Table I — Output Codes

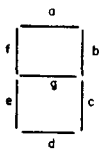
Binary Input B3 B2 B1 B0	Display Hexadecimal CD22104	Display Decimal CD22104A
0 0 0 0	0	0
0 0 0 1	1	1
0 0 1 0	2	2
0 0 1 1	3	3
0 1 0 0	4	4
0 1 0 1	5	5
0 1 1 0	6	6
0 1 1 1	7	7
1 0 0 0	8	8
1 0 0 1	9	9
1 0 1 0	-	-
1 0 1 1	b	E
1 1 0 0	C	H
1 1 0 1	d	L
1 1 1 0	E	P
1 1 1 1	F	(BLANK)

92CS-33050

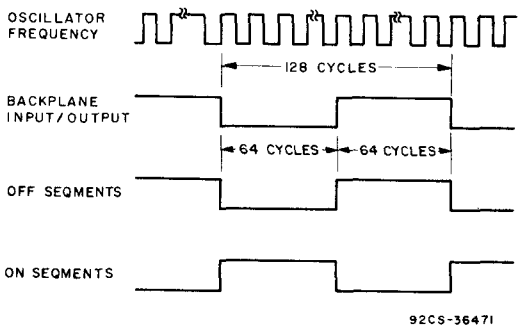
DIGIT SELECTION TRUTH TABLE

Pins 31	32	33	34	Digit Selected
1	0	0	0	D1 (LSD)
0	1	0	0	D2
0	0	1	0	D3
0	0	0	1	D4 (MSD)

DISPLAY SEGMENTS



92CS-31376



92CS-36471

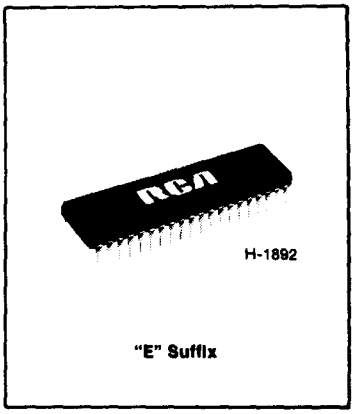
Fig. 6 - Display waveforms.

CMOS Four-Digit LCD Decoder-Drivers

6-V Rating

Features
- *6-V supply-voltage rating*
- *No external components necessary*
- *4-digit segment drive capability*
- *Backplane input/output allows synchronization for cascading devices to drive more digits*
- *Direct microprocessor interface*
- *Decodes binary into hexadecimal (CD22105) and decimal (CD22105A) outputs*

Applications
- *Microprocessor-controlled digital meters and calculators*
- *General-purpose displays*
- *Microprocessor-controlled automotive dashboard displays*
- *Microprocessor appliance control panels*



The RCA-CD22105 types are non-multiplexed, four-digit, seven-segment, liquid-crystal display decoder-drivers.

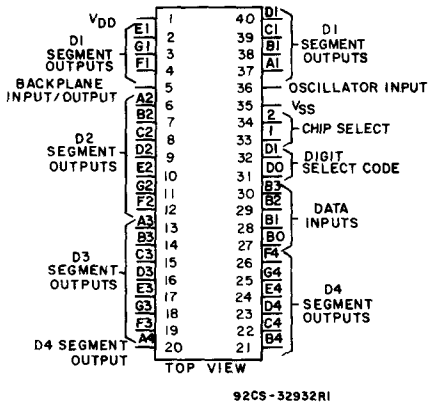
The CD22105 types contain all the circuitry necessary to drive conventional liquid-crystal displays (no external components required). Outputs are four sets of seven-segment driver signals and a backplane driver signal. The backplane signal, derived from an on-board free-running oscillator, is common to all four-digit displays.

The backplane and segment drives are designed so that p and n channels have the same ON resistances and thus equal rise and fall times. This equality eliminates any DC component, thereby maximizing display life. In addition to feeding the internal display drivers, the backplane signal can also be used as a master to drive a number of slave devices. The number of slaved devices should be limited to the load that keeps the backplane rise and fall times from exceeding 5 μs. If this limit is to be exceeded, the master backplane drivers should be disabled (by connecting pin 36, the oscillator input, to V_{SS}) and pin 5 should be fed from an external oscillator and all devices slaved to it. The maximum frequency of the external signal should be 125 Hz at room temperatures.

The on-board oscillator, which operates at 16 kHz when free-running (pin 36 floating), provides a backplane signal whose frequency is approximately 125 Hz. This frequency can be reduced by connecting an external capacitor to pin 36. Plots of backplane frequency vs. supply voltage at various values of external capacitance are shown in Fig. 3. The oscillator may be overdriven by an external signal but care must be taken to keep the lower voltage level above V_{SS} by at least 20 per cent of V_{DD} (for V_{DD}=5 V the signal should oscillate between +1 and +5 volts). This precaution prevents the backplane driver from being disabled, a condition that would present a DC component to the LCD display. A signal swinging from rail-to-rail can also be used to overdrive the oscillator but in this case the duty cycle should be such that the lower portion of the signal must be less than one-microsecond duration (the backplane disable sensing circuit will not respond to signals of this duration).

A four-bit data-input latch and a two-bit select-code latch under the control of two chip-select inputs permit interfacing with a microprocessor. This device simplifies designing a seven-segment display into a microprocessor system, without requiring extensive ROM or CPU time for decoding and display updating. The four-bit binary input is decoded by means of a PROM into a seven-segment hexadecimal output for the CD22105 type and into a decimal display for the CD22105A type. These types are pin-compatible with the Intersil ICM7211MIPL and ICM7211AMIPL, respectively.

The CD22105 types are supplied in the 40-lead dual-in-line plastic (E suffix) package.



CD22105, CD22105A
Terminal Assignment

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.3 to +6.5 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.3 to V_{DD} +0.3 V
DC INPUT CURRENT, ANY ONE INPUT* ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A=-20 to +60°C ..... 500 mW
For T_A=+60 to +70°C ..... Derate Linearly at 12 mW/°C to 380 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A=FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A): ..... -20 to +70°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -55 to +125°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

*Pin 36 limited to ±5 mA.

STATIC ELECTRICAL CHARACTERISTICS
T_A=25°C, V_{DD}=5 V, V_{SS}=0 V

CHARACTERISTIC	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN.	TYP.	MAX.	
Operating Supply Voltage Range	V_{DD}	V_{SS} = 0 V	3	5	6	V
Operating Current	I_{op}	Display Operating	—	10	50	μA
Oscillator Input Current	I_{OL}, I_{OH}	Pin 36	—	±2	±10	μA
Segment Rise and Fall Time	t_{rs}, t_{fs}	C_L = 200 pF	—	0.5	—	μs
Backplane Rise and Fall Time	t_{rB}, t_{fB}	C_L = 5000 pF	—	1.5	—	μs
Oscillator Frequency	f_{OSC}	Pin 36 Floating	—	16	—	kHz
Backplane Frequency	f_{BP}	Pin 36 Floating	—	125	—	Hz
Input High Voltage	V_{IH}		3.5	—	—	V
Input Low Voltage	V_{IL}		—	—	1.5	V
Input Leakage Current	I_{IL}	Pins 27-34	—	±0.01	±1	μA
Input Capacitance	C_I	Pins 27-34	—	5	—	pF
Backplane Input Leakage	$I_{IL(BP)}$	Pin 5 with Pin 36 @ V_{SS}	—	±0.01	±1	μA
Backplane Input Capacitance	$C_{I(BP)}$		—	200	—	pF

DYNAMIC ELECTRICAL CHARACTERISTICS
T_A=25°C, V_{DD}=5 V, V_{SS}=0 V

CHARACTERISTIC	SYMBOL	CONDITIONS	TYP. VALUES	UNITS
Chip-Select Active Pulse Width	t_{cas}	See Timing Diagram	100	ns
Data Setup Time	t_{dsm}	See Timing Diagram	50	ns
Data Hold Time	t_{dhm}	See Timing Diagram	25	ns
Inter-Chip Select Time	t_{ics}	See Timing Diagram	1	μs

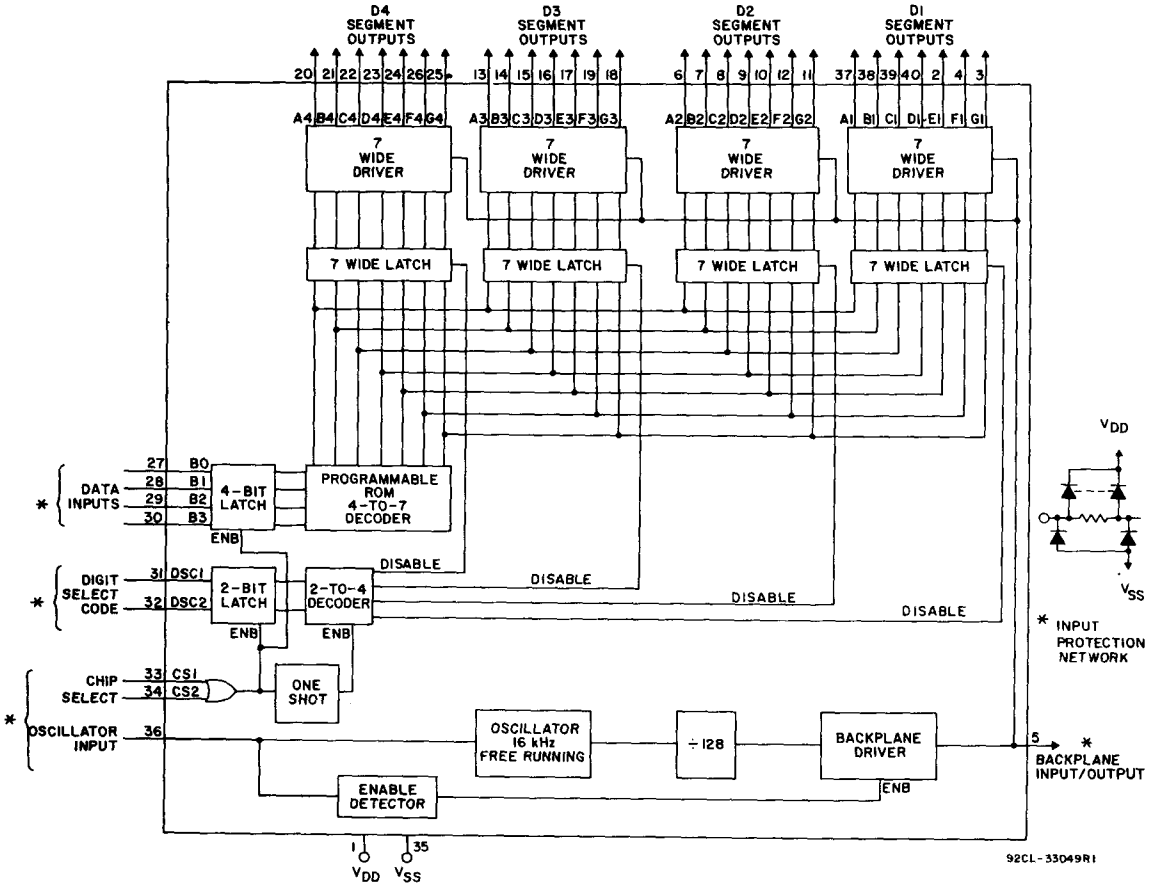


Fig. 1 - Block diagram of CD22105 and CD22105A.

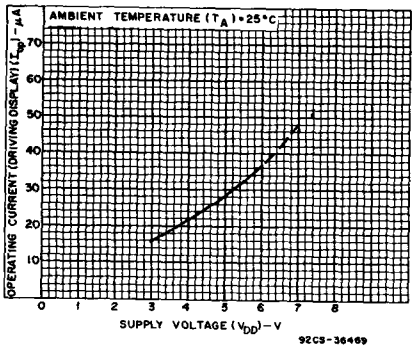


Fig. 2 - Typical operating current as a function of supply voltage.

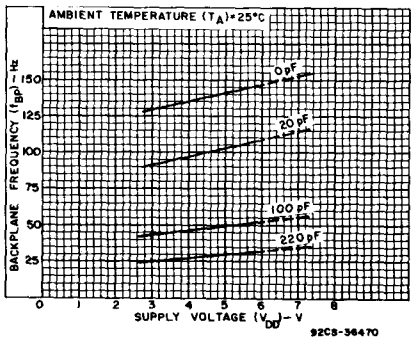


Fig. 3 - Typical backplane frequency as a function of supply voltage and external capacitance on pin 36.

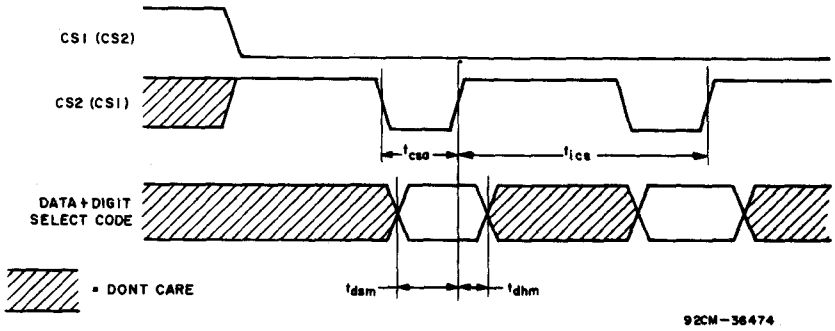


Fig. 4 - CD22105, CD22105A timing diagram.

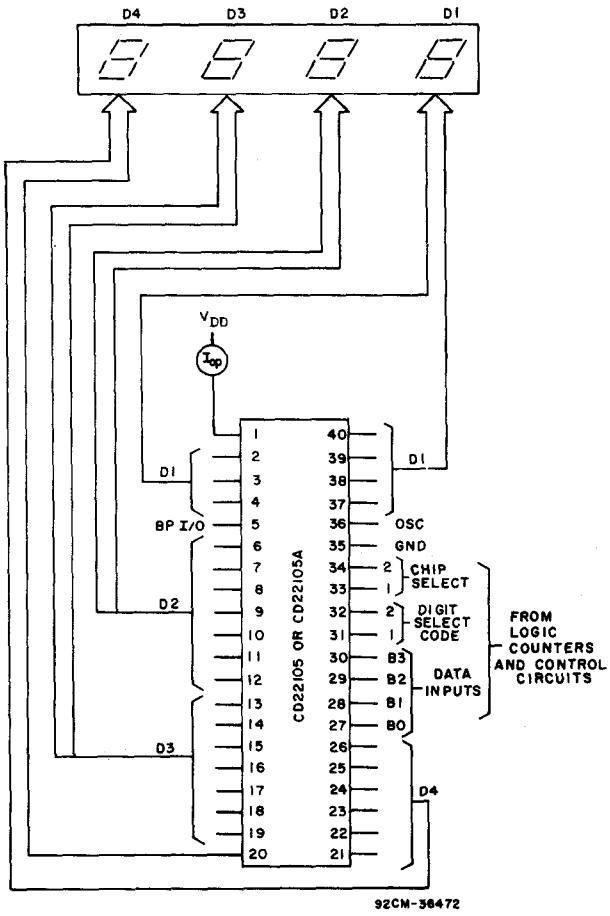


Fig. 5 - Test circuit.

Table I — Output Codes

Binary Input B3 B2 B1 B0	Display: Hexadecimal CD22105	Display: Decimal CD22105A
0 0 0 0	0	0
0 0 0 1	1	1
0 0 1 0	2	2
0 0 1 1	3	3
0 1 0 0	4	4
0 1 0 1	5	5
0 1 1 0	6	6
0 1 1 1	7	7
1 0 0 0	8	8
1 0 0 1	9	9
1 0 1 0	A	-
1 0 1 1	b	E
1 1 0 0	C	H
1 1 0 1	d	L
1 1 1 0	E	P
1 1 1 1	F	(BLANK)

92CS-33150

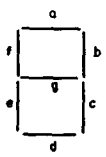
CHIP-SELECT TRUTH TABLE

Pins 33	Pins 34	Function
0	0	New inputs from μP are written into input latches
0	1	Inputs from μP are latched in input latches, decoded, and passed through selected (1 of 4) output latch to update selected digit
1	0	
1	1	

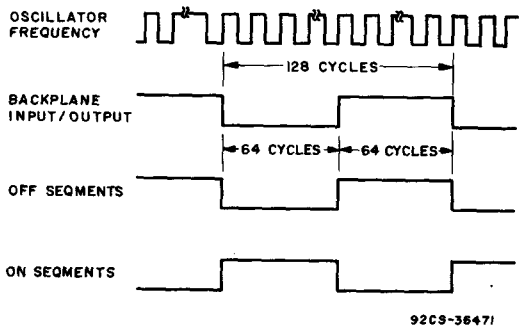
DIGIT SELECTION TRUTH TABLE

Pins 31	Pins 32	Digit Selected
1	1	D1 (LSD)
0	1	D2
1	0	D3
0	0	D4 (MSD)

DISPLAY SEGMENTS



92CS-31376



92CS-36471

Fig. 6 - Display waveforms.

CD22301
PCM Line Repeater

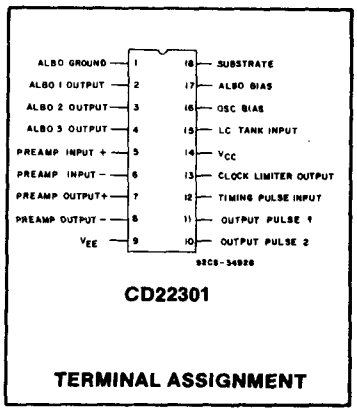
Preliminary Data

Features:

- *Automatic line buildout*
- *5.1 V supply voltage*
- *Buffered output*

Applications:

- *T1 1.544 Mbits/s bipolar carrier system*
- *T148 2.37 Mbits/s ternary carrier system*



CD22301

TERMINAL ASSIGNMENT

The RCA-CD22301 monolithic PCM repeater circuit is designed for T1 carrier systems operating with a bipolar pulse train of 1.544 Mbits/s. It can also be used in the T148 carrier system operating with a ternary pulse train of 2.37 Mbits/s. The circuit operates from a 5.1 V ± 5 % externally regulated supply.

The CD22301 provides active circuitry to perform all functions of signal equalization and amplification, automatic line buildout (ALBO), threshold detection, clock extraction, pulse timing, and buffered output formation.

The CD22301 is supplied in an 18-lead dual-in-line plastic package (E suffix).

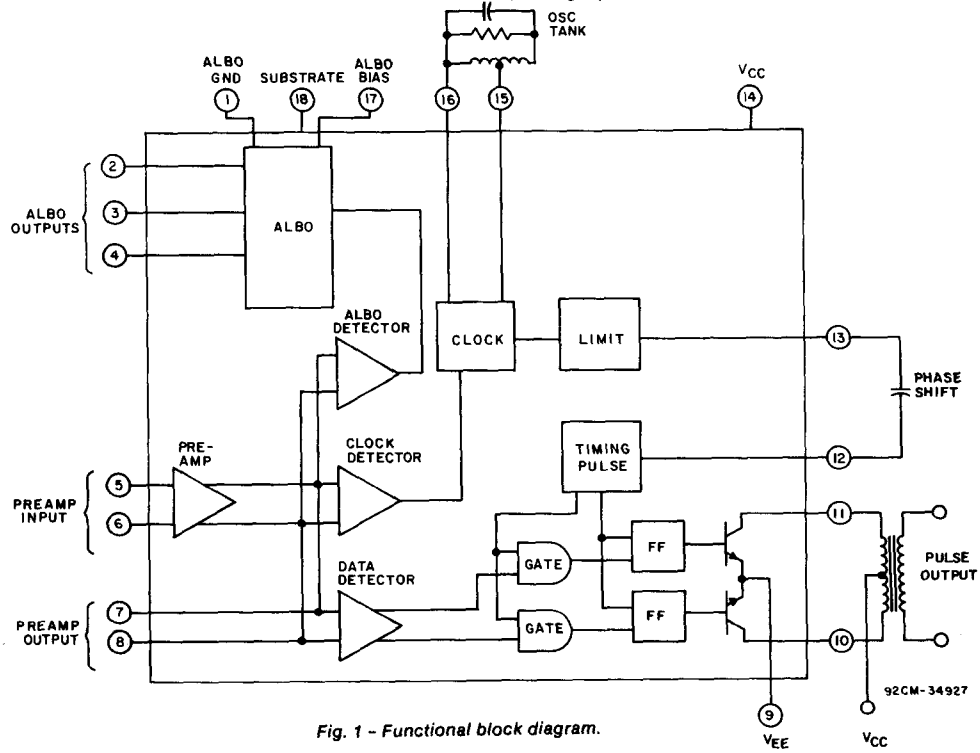


Fig. 1 - Functional block diagram.

MAXIMUM RATINGS, *Absolute Maximum Values:*

At ambient temperature (T_A) = 25°C

DC SUPPLY ..... 10 V
DC CURRENT (Into Pin 9 or 10) ..... 25 mA
PEAK CURRENT (Into Pin 9 or 10) ..... 100 mA
INPUT SURGE VOLTAGE (Between Pins 5 and 6, t = 10 ms) ..... 50 V
OUTPUT SURGE VOLTAGE (Between Pins 10 and 11, t = 1 ms) ..... 50 V
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to +60°C ..... 500 mW
For T_A = +60°C to +85°C ..... Derate linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = Full Package-Temperature Range ..... 100 mW
OPERATING TEMPERATURE RANGE (T_A) ..... -40 to +85°C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING)
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10s max. ..... +256°C

STATIC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5.1 V ± 5% (See Fig. 2)

CHARACTERISTIC	LIMITS			UNITS
	Min.	Typ.	Max.	
DC VOLTAGES				
Pins 2, 3, 4 and 17	—	0	0.1	V
Pins 5, 6, 7 and 8	2.4	2.9	3.4	V
Pins 10 and 11	—	5.1	—	V
Pins 12, 13, 15 and 16	3.1	3.6	4.1	V
DC CURRENTS				
Pin 14	—	22	30	mA
Pins 10 and 11	—	0	100	μA

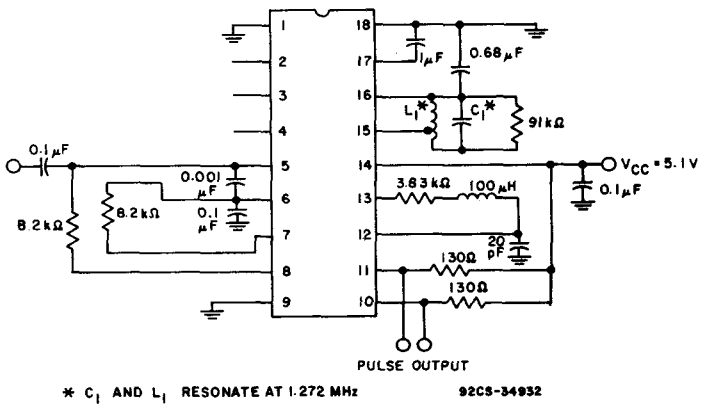


Fig. 2 - DC and output pulse test circuit.

DYNAMIC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 5.1 V ± 5%

CHARACTERISTIC	SYMBOL	FIG.	NOTE	LIMITS			UNITS
				MIN.	TYP.	MAX.	
Preamplifier Input Imedance	Z_{in}	3		20	—	—	kΩ
Preamplifier Output Impedance	Z_{out}	3		—	—	2	kΩ
Preamplifier Gain @ 2.37 MHz	A_o	3		47	50	—	dB
Preamplifier Output Offset Voltage	ΔV_{out}	3	1	-50	0	50	mV
Clock Limiter Input Impedance	$Z_{in}(CL)$	4	2	10	—	—	kΩ
ALBO Off Impedance	$Z_{ALBO}(off)$	4	3	20	—	—	kΩ
ALBO On Impedance	$Z_{ALBO}(on)$	4	4	—	—	10	Ω
DATA Threshold Voltage	$V_{TH}(D)$	5	5, 8	0.75	0.8	0.85	V
CLOCK Threshold Voltage	$V_{TH}(CL)$	5	6, 8	—	1.12	—	V
ALBO Threshold	$V_{TH}(AL)$	5	7, 8	1.5	1.6	1.7	V
$V_{TH}(D)$ as % of $V_{TH}(AL)$				42	45	49	%
$V_{TH}(CL)$ as % of $V_{TH}(AL)$				65	70	75	%
Buffer Gate Voltage (low)	V_{OL}	2	9	0.65	0.8	0.95	V
Differential Buffer Gate Voltage	ΔV_{OL}	2	9	-0.15	0	0.15	V
Output Pulse Rise Time	t_r	2, 6	9, 10	—	—	40	ns
Output Pulse Fall Time	t_f	2, 6	9, 10	—	—	40	ns
Output Pulse Width	t_w	2, 6	9, 10	290	324	340	ns
Pulse Width Differential	Δt_w	2, 6	9, 10	-10	0	10	ns
Clock Drive Current	I_{CL}			—	2	—	mA

Notes:

1. No signal input. Measure voltage between pins 7 and 8.
2. Measure clock limiter input impedance at pin 15.
3. Adjust potentiometer for 0 volts. Measure ALBO off impedances from pins 2, 3 and 4 to pin 1.
4. Increase potentiometer until voltage at pin 17 = 2 Vdc. Measure ALBO on impedances from pins 2, 3 and 4 to pin 1.
5. Adjust potentiometer for ΔV = 0 volts. Then slowly increase ΔV in the positive direction until pulses are observed at the DATA terminal.
6. Continue increasing ΔV until the DC level at the clock terminal drops to 4 volts.
7. Continue increasing ΔV until the ALBO terminal rises to 1 volt.
8. Turn potentiometer in the opposite direction and measure negative threshold voltages by repeating tests outlined in notes 5, 6 and 7.
9. Set e_{in} = 2.75 mV(rms) at f ≈ 1.185 MHz. Adjust frequency until maximum amplitude is obtained at pin 15. Observe output pulses at pins 10 and 11.
10. Adjust input signal amplitude until pulses just appear in outputs. Increase input amplitude by three dB.

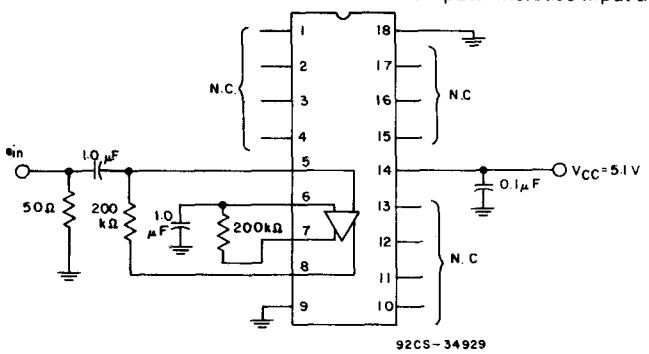


Fig. 3 - Preamplifier gain and impedance measurement circuit.

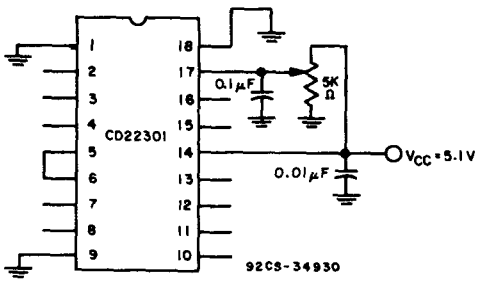


Fig. 4 – Test circuit for impedance measurement.

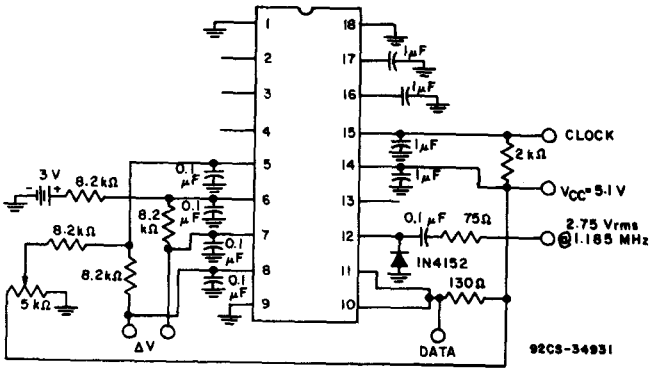


Fig. 5 – Test circuit for threshold voltage measurement.

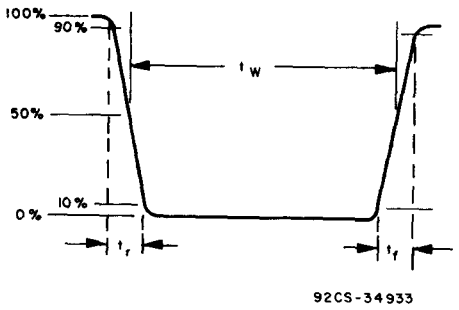


Fig. 6 – Output pulse waveform.

CMOS 16-Channel Precision Timer/Driver

Features:

- *Provides 17 precision-timed output pulses*
- *Variable output pulse width as a function of an external timer clock frequency*
- *High source current drive output pulses- up to 15 mA using bipolar drivers*
- *Serial data interface via shift register*
- *EP inputs provide added control logic flexibility for output selection in addition to shift register data*
- *Static operation- shift register and timers can operate at DC and still retain counts and data levels*
- *For multiple device use, shift registers can be cascaded*
- *Provides inherent serial-to-parallel data conversion*
- *Offers output disable capability using inhibit features*
- *Low power CMOS logic*
- *Input/output protection circuitry*

"E" Suffix

40-Lead Dual-In-Line Plastic Package

H-1892

The RCA CD22401 is a precision timer/driver. It is an interface circuit and has been designed to provide critically timed output pulses for high-speed printers. The device is fabricated using CMOS enhancement-mode technology with the resulting low power consumption.

The circuit consists of a 16-stage (optionally 17) shift register with each register output connected to a latch and its respective timer and output buffer stage. Thus, there are 17 latches, timers, and driver (output buffer) stages. The output driver pulse width is a function of the timer clock frequency, since it depends upon a fixed count in hardware.

Data is fed serially into the shift register by means of the shift register clock. Then the input sequence is strobed out in parallel to the shift register latch. A particular output is turned on (pulsed high) if the associated latch holds a logic "1" and when the proper enable signal is activated. Simultaneously, the enable signal starts the associated timer which controls the output pulse width. After a time period of 100 negative edges of the clock (99 to 100 clock pulses), the output is turned off. This provides timing accuracy within 1%.

The CD22401 is supplied in the 40-lead dual-in-line plastic package (E suffix) and in chip form (H suffix). It is useful in applications requiring precision pulse widths.

Register Operation

In operation, a serial string of 16 (17 using the optional flip-flop) bits is fed into the shift register (see Fig. 4 for shift register timing). Ones ("1s") determine an output drive pulse and zeros ("0s") indicate no drive. Any one output enable (EP) line is connected to four selected timers giving the potential for four outputs per one $\overline{EP}$ pulse with the exception that $\overline{EP5}$ connects one timer only. EP lines may be connected to each other.

After a sequence of 16 bits (or 17) is serially loaded into the shift register, a strobe pulse activates the latch so that the register data "word" is transferred out in parallel into the register latch. Here the data waits until an active enable signal combines with a "one" from any latch at which time the counter begins and the respective output driver goes high. The output will continue high until the counter achieves 100 negative edges. It has been assumed that the output inhibit control has not been activated. The inhibit is a control which gates the output "OFF" and can thereby prevent start-up or transient situations.

The register latch has 17 outputs each of which feeds its respective timer (one timer circuit for each output from the register latch). Also, each timer provides access to an output driver.

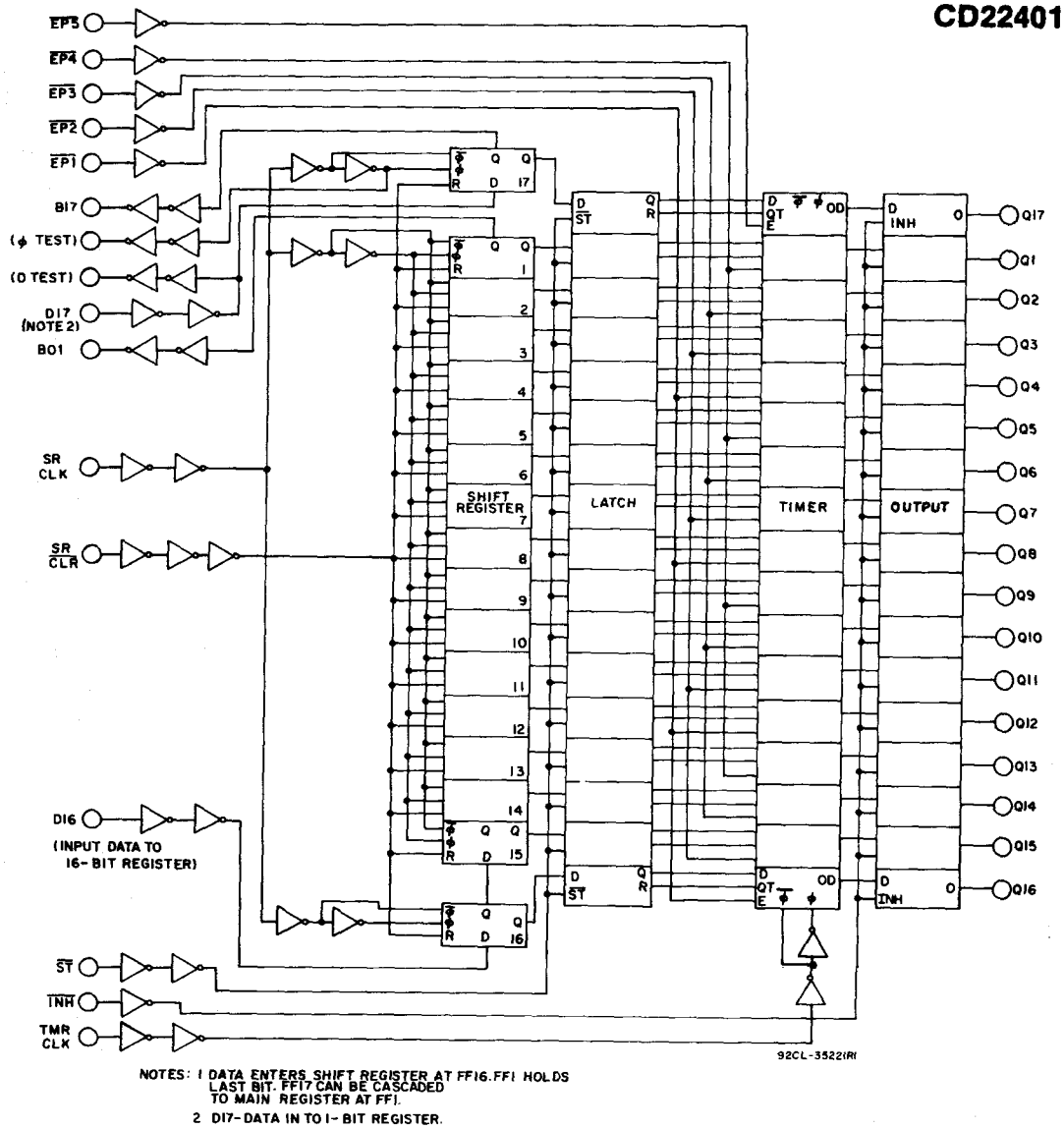
Timer Operation

When the timer begins counting and the output goes high, the latch is held reset to prevent retriggering before the count is finished.

During start-up (before reliable count operation), the timers need 128 clock pulses at the timer inputs to guarantee a reset condition before enable pulses are applied.

After an output pulse goes low (becomes inactive), seven clock pulses should be applied at the timer clock input before any timer is retriggered by means of an enable and data "one" combination (repeat of another output pulse at same pin).

The data and the enable pulses together control which combination of timers and driver stages become activated to produce output pulses.



NOTES: 1 DATA ENTERS SHIFT REGISTER AT FF16.FF1 HOLDS LAST BIT. FF17 CAN BE CASCADED TO MAIN REGISTER AT FF1.
2 DI7-DATA IN TO 1-BIT REGISTER.

Fig. 1 - CD22401 block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltage referenced to V_{SS} terminal) ..... -0.5 to 6.5 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = 0°C to 70°C (PACKAGE TYPE E) ..... 500 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A) ..... 0°C to 70°C
STORAGE-TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

CD22401

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

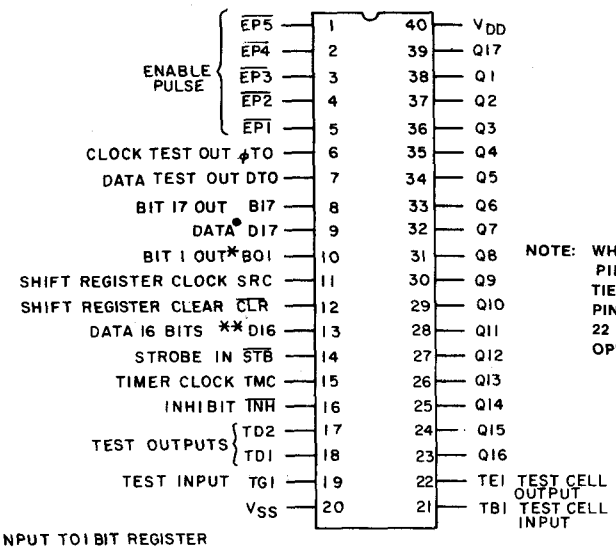
CHARACTERISTIC	LIMITS		UNITS
	V_{DD}	V_{SS}	
Supply Voltage Range (For T_A = Full Package Temperature Range)	5	0	V

STATIC ELECTRICAL CHARACTERISTICS at T_A = 25°C, V_{DD} = 5 V

CHARACTERISTIC		CONDITIONS	LIMITS			UNITS
			Min.	Typ.	Max.	
Input Low Voltage	V_{IL}		—	—	0.8	V
Input High Voltage	V_{IH}		2.4	—	—	
Output Voltage Low-Level	V_{OL}	V_{IN} = V_{IH} or V_{IL}	—	—	—	
		I_{OL} = 0 μA *	—	—	0.05	
		I_{OL} = 1.6 mA ‡	—	—	0.4	
		I_{OL} = 1 mA *	—	—	0.5	
Output Voltage High Level	V_{OH}	V_{IN} = V_{IH} or V_{IL}	—	—	—	
		I_{OH} = 0 μA *	3.5	—	—	
		I_{OH} = 5 mA *	3.2	—	—	
		I_{OH} = 10 mA *	2.5	—	—	
		I_{OH} = 15 mA *	2.2	—	—	
		I_{OH} = 0 μA ‡	4.9	—	—	

* Output Pins 23-39

‡ Output Pins 8, 10



NOTE: WHEN USING CD22401 PIN 19 SHOULD BE TIED TO V_{SS} (OR V_{DD}). PINS 6,7,17,18,21, AND 22 SHOULD BE LEFT OPEN.

•INPUT TO1 BIT REGISTER

*OUTPUT OF 16 BIT REGISTER

**INPUT TO 16 BIT REGISTER

92CS-35201RI

TERMINAL ASSIGNMENT

DYNAMIC ELECTRICAL CHARACTERISTICS At T_A = 25° C, Input t_r, t_f = 20 ns, C_L = 50 pF

CHARACTERISTIC		FIG.	TEST CONDITIONS		LIMITS			UNITS
			V_{DD}(V)	C_L	Min.	Typ.	Max.	
Timer Clock Frequency	t_{rTCL}	3	5	—	0	0.7	1	MHz
Timer Clock Pulse Width	t_{WTCL}	3	5	—	500	—	—	nsec
Timer Clock Rise and Fall Time	t_{rCK}, t_{fCK}	5	5	—	—	—	2	μsec
Output Inhibit Pulse Width	t_{WOI}	5	5	—	500	—	—	nsec
Inhibit Output Turn-Off Delay	t_{PHLI}	5	5	50	—	—	550	nsec
Output Turn-On Delay after Inhibit is OFF	t_{PLHI}	5	5	50	—	—	550	nsec
Enable Pulse (EP) Width	t_{WHEP}	3	5	—	500	—	—	nsec
Transfer Strobe Pulse Width *	t_{WTS}	3	5	—	350	—	—	nsec
Output L-H Transition Time	t_{TLH}	5	4.5	50	—	—	85	nsec
Output H-L Transition Time	t_{THL}	5	4.5	50	—	—	150	nsec
Output Turn-On Prop. Delay Time	t_{PLH}	5	4.5	50	—	—	1200	nsec
Output Turn-Off Prop. Delay Time	t_{PHL}	5	4.5	50	—	—	1200	nsec
High-Level Output Driver Pulse Width	t_{out}	3	4.5	50	99	—	100	Timer Clock Pulses
Shift Register Input Clock Frequency	t_{fSRCL}	2, 4	5	—	—	2	2.5	MHz
Shift Register Clock Pulse Width	t_{WSRCL}	2	5	—	200	—	—	nsec
Shift Register Data Set-Up Time	t_{setup}	2	5	—	100	—	—	nsec
Shift Register Data Hold Time	t_{SRHOLD}	2	5	—	200	—	—	nsec
Shift Register Data Pulse Width	t_{WSRD}	2	5	—	300	—	—	nsec
Shift Register Data Output Prop. Delay Time	t_{PDLH}	2	5	50	—	—	200	nsec
Shift Register Clear Pulse Width	t_{SRCLR}	2	5	—	200	—	—	nsec

* Data from shift register must be stable at time of transfer.

AC Waveforms

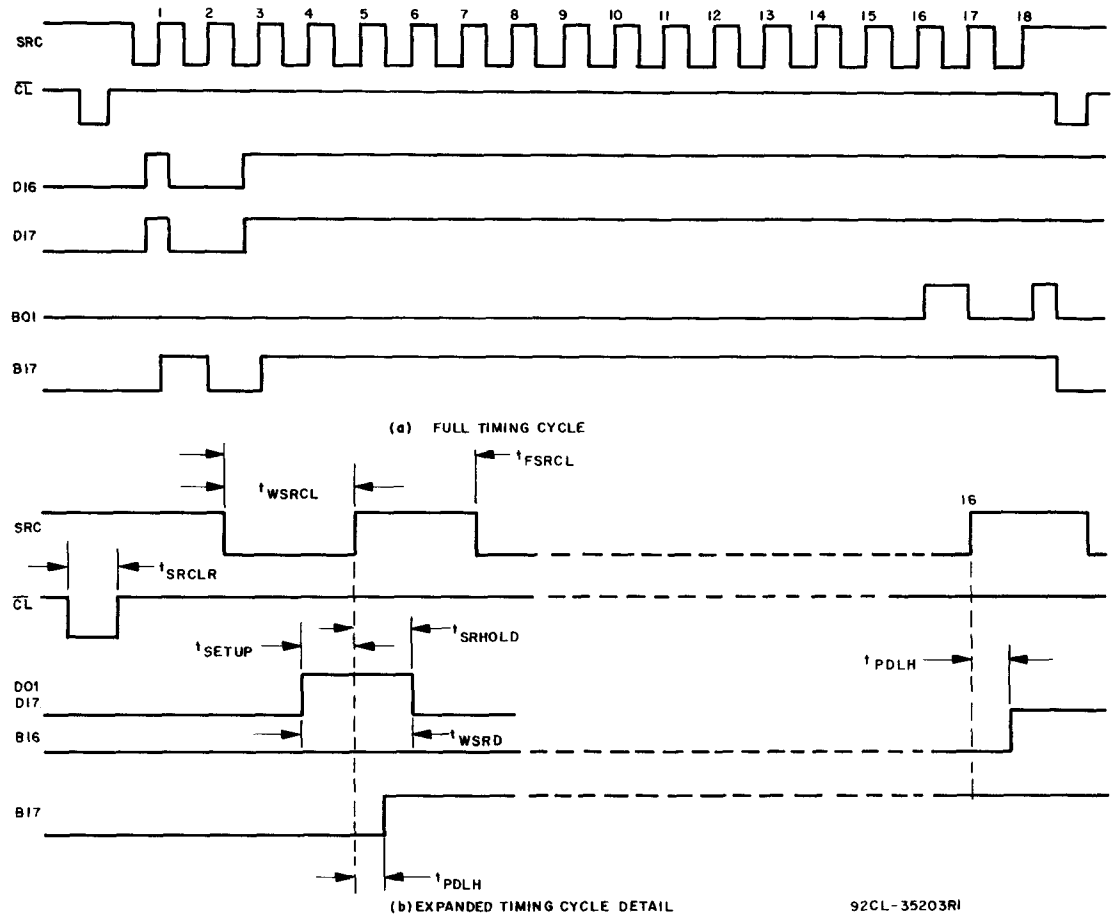


Fig. 2 - Functional timing diagram-shift registers function.

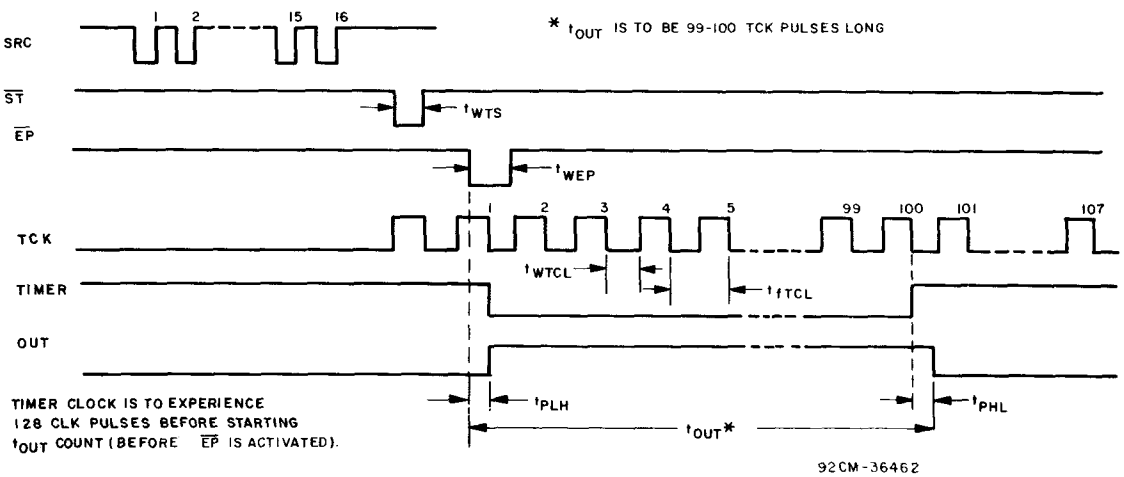


Fig. 3 - Functional timing diagram-shift registers function.

AC Waveforms (cont'd)

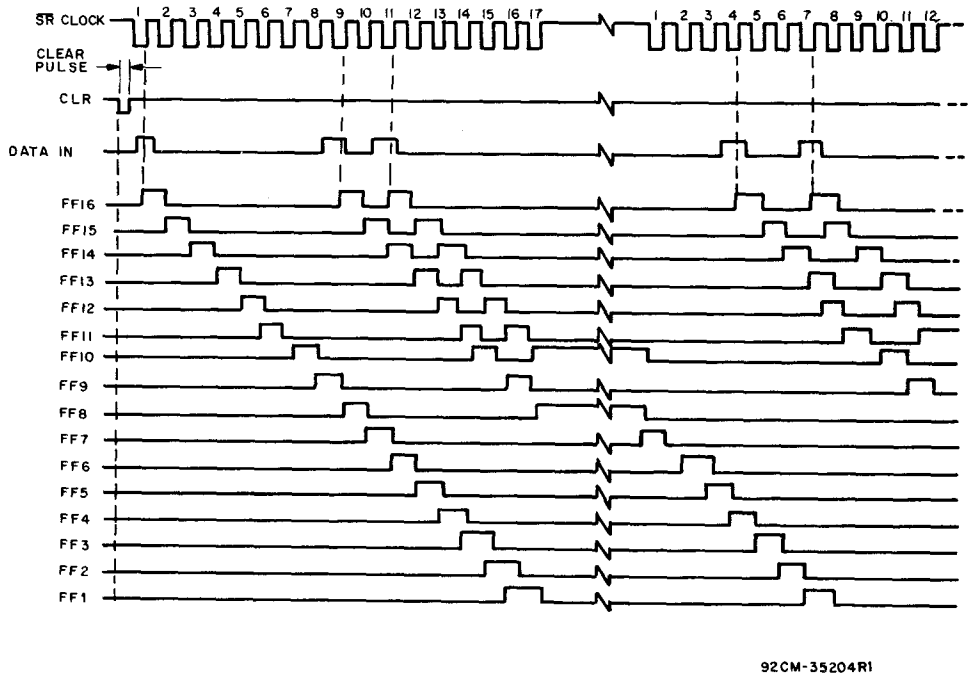


Fig. 4 - Functional timing diagram-shift registers function.

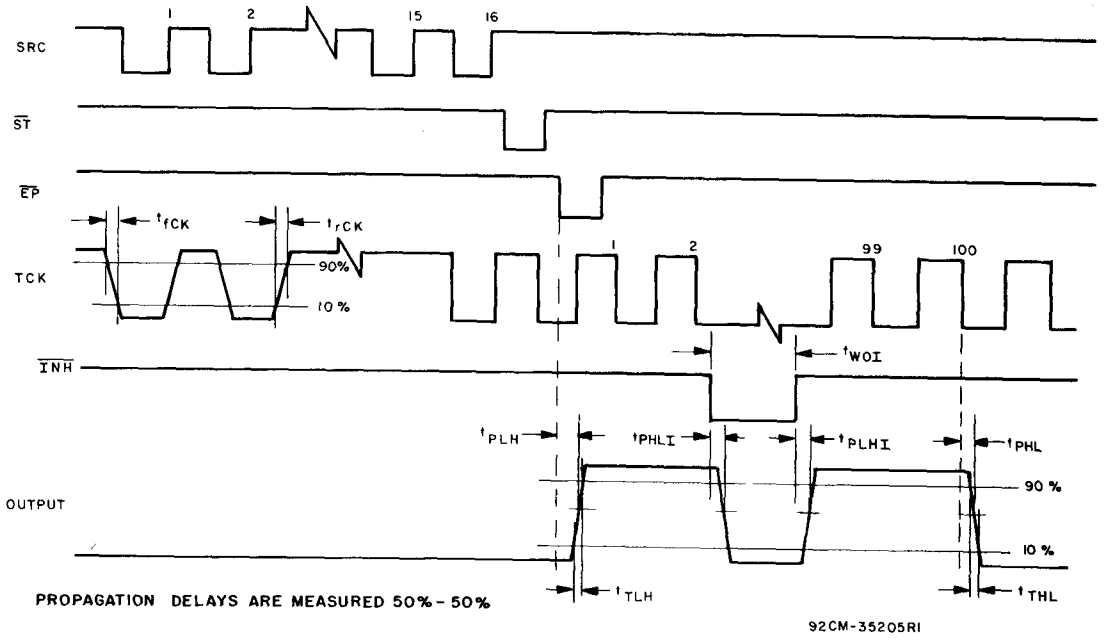


Fig. 5 - Functional timing diagram-shift register function detail.

CMOS Pulse Code Modulation Sampled — Data Filters

Preliminary Data

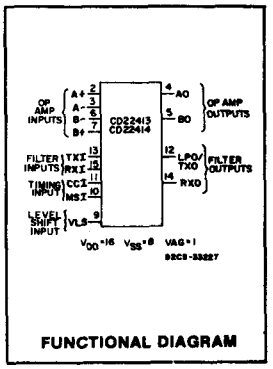
The RCA-CD22413 and CD22414 are sampled-data, switched-capacitor filters intended for use in PCM CODEC systems or other telecommunication systems requiring band limiting. Transmit and receive filters in both devices are 5-pole elliptical types, operating at a sample rate of 128 kHz. In addition, the CD22413 contains a 3-pole Chebyshev high-pass filter in the transmit section that provides 50/60 Hz and 15 Hz rejection. Both devices also include two operational amplifiers which may be used as building blocks in a system.

A 50% duty-cycle clock on the convert-clock input (CCI) determines the cutoff frequencies for the filters. The cutoff frequency (f_o) is given by the equation; f_o = 0.02422 X Clock Frequency. Normally, the clock frequency is 128 kHz for a cutoff frequency of 3100 Hz. The master sync input (MSI) should be 8 kHz and have it's low-to-high transition coincide with each new PAM sample received at Receive-Filter-In (RXI). RXI will accept 19% to 100% duty cycle PAM at 8 kHz.

Timing and synchronization signals (CCI and MSI) may be made either TTL- or CMOS-compatible through use of the Logic-Shift Voltage (VLS) input. Specific input conditions are listed in the table of Logic-Shift-Voltage inputs. The analog ground (VAG) should be held at approximately (V_{DD}-V_{SS})/2. If VAG is within one volt of V_{DD2} the chip will be powered down. The CD22413 is pin-compatible with the MC14413; the CD22414 is pin-compatible with the MC14414.

The CD22413 and CD22414 are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffix), 16-lead dual-in-line plastic packages (E suffix), and chip form (H suffix).

Features:
- *Single supply (10V-16V) or dual supply operation*
- *Transmit bandpass and receive low pass filters (CD22413)*
- *Transmit and receive low pass filters (CD22414)*
- *30 mW (typ.) operating power*



FUNCTIONAL DIAGRAM

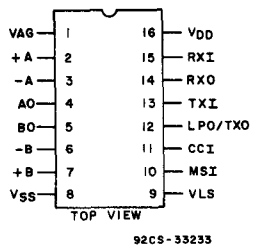
MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
(Voltages referenced to V_{SS} Terminal) ..... -0.5 to +18 V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10 mA
POWER DISSIPATION PER PACKAGE (P_D)
For T_A = -40 to +60°C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E) ..... Derate Linearly at 12 mW/°C to 200 mW
For T_A = -55 to +100°C (PACKAGE TYPES D, F) ..... 500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F) ..... Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
For T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100 mW
OPERATING-TEMPERATURE RANGE (T_A)
PACKAGE TYPES D, F, H ..... -55 to +125°C
PACKAGE TYPE E ..... -40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. ..... +265°C

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Terminal Designation	LIMITS			UNITS
		Min.	Typ.	Max.	
DC Supply Voltage (For T_A = Full Package Temperature Range)	V_{DD} - V_{SS}	10	12	16	Vdc
Convert Clock Frequency	CCI	50	128	400	kHz
Master Sync Frequency	MSI	—	8	32	



TERMINAL ASSIGNMENTS

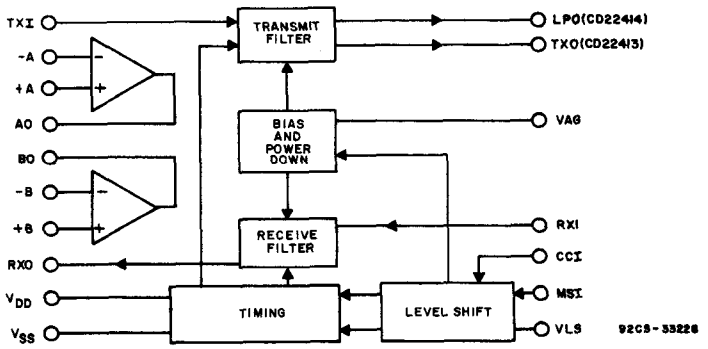


Fig. 1 - Block diagram of CD22413 and CD22414.

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V, T_A = 25°C)

CHARACTERISTIC		V_{DD} Vdc	LIMITS Min.	Typ.	Max.	UNITS
Operating Current	I	12	—	2.5	3.5	mA
Power-Down Current, (PDI = V_{SS})	I_{PD}	12	—	10	50	μA
Input Capacitance	C_{IN}	12	—	5	7.5	pF

MODE CONTROL LOGIC LEVELS

CHARACTERISTIC		V_{DD} Vdc	LIMITS Min.	Typ.	Max.	UNITS
VLS Power-Down Mode	V_{IH}	12	11	—	—	V
		15	14	—	—	
VLS TTL Mode		12	2	—	10	V
		15	2	—	13	
VLS CMOS Mode	V_{IL}	12	—	—	0.8	V
		15	—	—	0.8	
VAG Power-Down Mode	V_{IH}	12	11	—	—	V
		15	14	—	—	
VAG Analog-Ground Mode	V_{IL}	12	—	—	8	V
		15	—	—	11	

CMOS LOGIC LEVELS (VLS = V_{SS})

CHARACTERISTIC		V_{DD} Vdc	LIMITS Min.	Typ.	Max.	UNITS
Input Current	I_{IN}					
CCI		12	—	±0.00001	±0.3	μA
MSI "1" Level		—	—	30	—	
(Internal Pulldown Resistors) "0" Level		—	—	−0.00001	−0.3	
Input Voltage CCI, MSI						
"0" Level	V_{IL}	12	—	5.25	3.6	V
		15	—	6.75	4	
"1" Level	V_{IH}	12	8.4	6.75	—	
		15	11	8.25	—	

TTL LOGIC LEVELS (VLS = 6 V, V_{SS} = 0 V)

CHARACTERISTIC		V_{DD} Vdc	LIMITS Min.	Typ.	Max.	UNITS
Input Current	I_{IN}					
CCI		12	—	±0.00001	±0.3	μA
MSI "1" Level		—	—	3	—	
(Internal Pulldown Resistor) "0" Level		—	—	−0.00001	−0.3	
Input Voltage CCI, MSI						
"0" Level	V_{IL}	12	—	—	VLS +0.8	V
"1" Level	V_{IH}	12	VLS+2	—	—	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V, T_A = 25° C)

CHARACTERISTIC		LIMITS Min.	Typ.	Max.	UNITS
Input Current, (RXI, TXI, VAG)	I_{IN}	—	±0.00001	±0.03	μA
AC Input Impedance (1 kHz) (RXI, TXI, VAG)	Z_{IN}	—	2	—	MΩ
Input Common Mode Voltage Range (TXI, RXI, +A, −A, +B, −B)	V_{ICR}	1.5	—	10.5	V
Input Offset Current (+A to −A, +B to −B)	I_{IO}	—	±10	—	nA
Input Bias Current (+A, −A, +B, −B)	I_{IB}	—	±0.10	±1	nA
Input Offset Voltage (+A to −A, +B to −B)	V_{IO}	—	±10	±25	mV
Output Voltage Range (AO, BO, TXO, LPO, RXO)	V_{OR}				
(R_L = 20 kΩ to VAG, R_B = ∞)		1.5	—	10.5	V
(R_L = 600 Ω to VAG, R_B = 1.6 kΩ to V_{DD})		4.3	—	7.9	
(R_L = 900 Ω to VAG, R_B = 1.8 kΩ to V_{DD})		4	—	8.2	
Small Signal Output Impedance (1 kHz) (TXO CD22413)	Z_O	—	50	—	Ω
(LPO CD22414)		—	50	—	
(RXO)		—	50	—	
Output Current (V_{OH} = 11V) (TXO, LPO, RXO, AO, BO)	I_{OH}	—	−400	—	μA
(V_{OL} = 1V) (TXO, LPO, RXO, AO, BO)	I_{OL}	—	5	—	mA

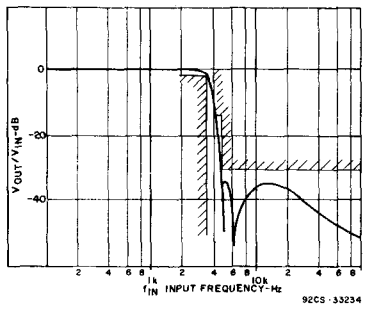


Fig. 3 - Receive filter typical and minimum performance for CD22413 or CD22414 with sinx x correction included.

RECEIVE FILTER SPECIFICATIONS (V_{DD} - V_{EE} 12V, CCI = 128 kHz, MSI = 8 kHz. includes sinx x correction, V_{in} = 0 dBm0, full scale = +3 dBm0, 7 V_{p-p}, T_A = 25°C)

CHARACTERISTIC		LIMITS Min.	Typ.	Max.	UNITS
Gain (1020 Hz)		−0.2	0	+0.2	dB
Passband Ripple (50 Hz to 300 Hz)		—	0.24	0.3	
Out of Band Rejection	See Note 1				
3400 Hz		—	−0.8	−1.5	
4000 to 4600 Hz		−14	−15.5	—	
4600 to 64 kHz		−30	−33	—	
Output Noise (RXI = VAG)	See Note 2	—	10	15	dBrnc0
Dynamic Range		78	83	—	dB
Differential Group Delay					
1150 to 2300 kHz Delay		—	12	22	μs
1000 to 2500 kHz Delay		—	25	35	
800 to 2700 kHz Delay		—	31	41	

Note 1: Referenced to passband minimum. Note 2: Referenced to 900Ω.

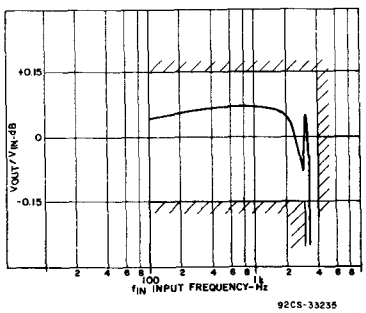


Fig. 4 - Receive filter typical and minimum passband performance for CD22413 or CD22414.

TRANSMIT FILTER SPECIFICATIONS (V_{DD}-V_{EE} = 12 V, CCI = 128 kHz MSI = 8 kHz, V_{in} = 0 dBm0, full scale = +3 dBm0, 7 V_{p-p}, T_A = 25°)

CHARACTERISTIC		LIMITS Min.	Typ.	Max.	UNITS
Gain (1020 Hz)		-0.15	—	+0.15	
Passband Ripple (300 Hz to 3000 Hz)		—	0.22	0.3	
Rejection	See Note 1				
60 Hz	CD22413 only	-20	-24	—	dB
180 Hz	CD22413 only	—	-0.6	-1	
3400 Hz		—	-0.8	-1.5	
4000 to 4600 Hz		-14	-15.5	—	
4600 to 64 kHz		-32	-33	—	
Output Noise	CD22413	—	—	—	
(300 to 3400 Hz)	CD22414	—	8	12	dBrnc0
Dynamic Range (7 Vpp Max)		81	87	—	dB
Differential Group Delay					
1150 to 2300 kHz Delay		—	12	22	μs
1000 to 2500 kHz Delay		—	25	35	
800 to 2700 kHz Delay		—	31	41	

Note 1: Referenced to passband minimum.

SWITCHING CHARACTERISTICS (V_{DD} - V_{SS} = 10 V, T_A = 25° C)

CHARACTERISTIC		LIMITS Min.	Typ.	Max.	UNITS
Input Rise and Fall Time, t_r, t_f	CCI, MSI	—	—	4	μs
Pulse Width, t_{WH}	CCI, MXI	100	50	—	ns
Clock Pulse Frequency, f_{CL}	CCI	50	—	500	kHz
Set Up Time, t_{SU} MSI Rising Edge to CCI Rising Edge (CCI = 128 kHz)*		-3	—	+3	μs

*Specifications assume use of 50% duty cycle for clocks.

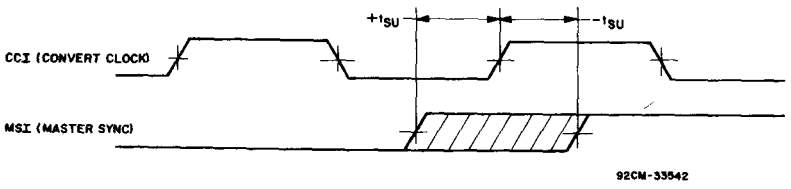


Fig. 2 - Switching characteristics wave forms.

LOGIC SHIFT VOLTAGE INPUTS

VLS PIN	LOGIC INPUT (CCI AND MSI)
VSS < VLS < VSS + 0.8V	CMOS
VDD - 1V < VLS < VDD	POWER DOWN
VSS + 2V < VLS < VDD - 2V	TTL (VLS + 0.8V < INPUT < VLS + 2V)

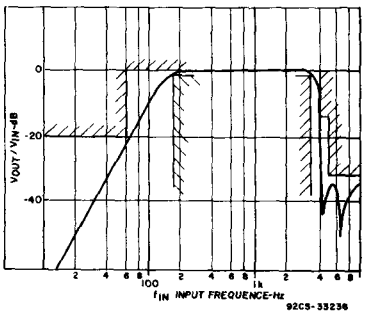


Fig. 5 - Transmit filter typical and minimum performance for CD22413 or CD22414 using Figs. 11 and 12.

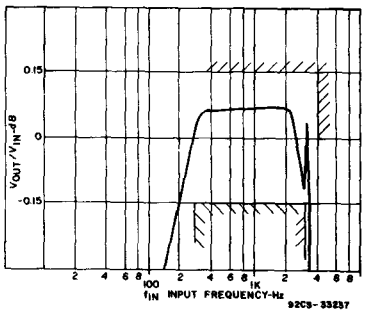


Fig. 6 - Transmit filter typical and minimum passband performance for CD22413 or CD22414 using Figs. 11 or 12.

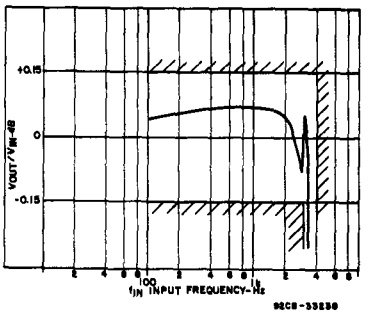


Fig. 7 - Transmit filter typical and minimum passband performance for CD22414.

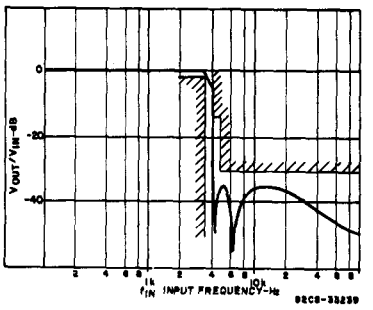


Fig. 8 - Transmit filter typical and minimum performance for CD22414.

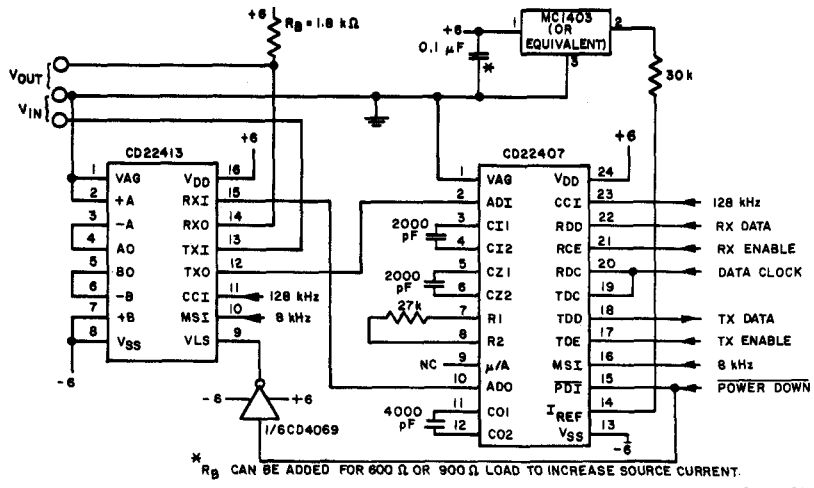


Fig. 9 - Typical circuit configuration using the CD22407 CODEC and CD22413 filter (split supply).

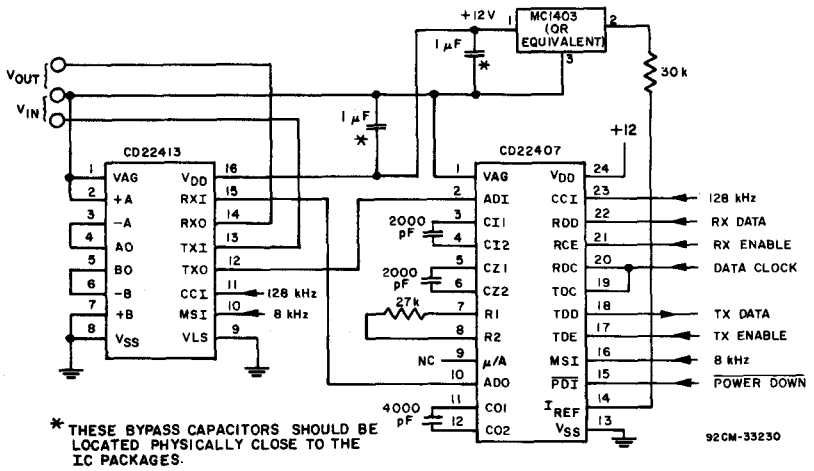


Fig. 10 - Typical circuit configuration using the CD22407 CODEC and CD22413 filter (single supply).

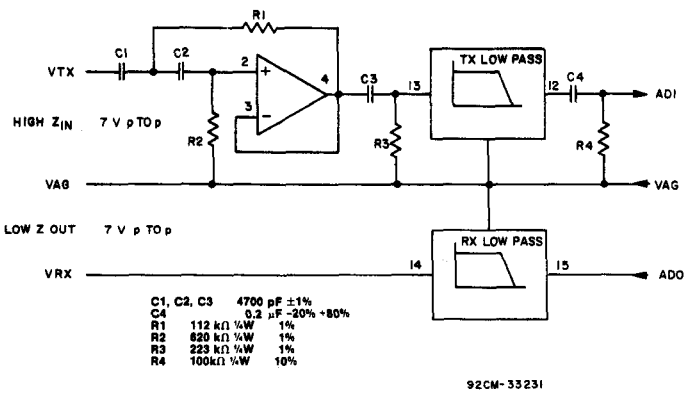


Fig. 11 - Filter schematic for CD22413 with 60-Hz reject filter.

VAG — (Analog Ground) This pin should be held at approximately (V_{DD}-V_{EE})/2. All analog inputs and outputs are referenced to this pin. If this pin is brought to within approximately 1 V of V_{DD}, the chip will be powered down.

+A Non-inverting input of op-amp A.

-A Inverting input of op-amp A.

AO Output of uncommitted op-amp A

BO Output of uncommitted op-amp B

-B Inverting input of op-amp B

+B Non-inverting input of op-amp B

V_{SS} This is the most negative supply pin and digital ground for the package.

VLS (Logic Shift Voltage) The voltage on this pin determines the logic compatability for the CCI and MSI inputs. If VLS is within 0.8 V of V_{SS}, the thresholds will be for CMOS operating between V_{DD} and V_{SS}. If VLS is within 1 V of V_{DD}, the chip will power down. If VLS is between V_{DD} - 2 V and V_{SS} 2 V, the thresholds for logic inputs at CCI and MSI will be between VLS + 0.8 V and VLS + 2 V for TTL compatability.

CCI (Convert Clock Input) Normally, a 128 kHz clock signal should be applied to this pin to operate both filters at f_o = 3100 Hz. For other break frequencies use the following equation: f_o = 0.02422 f clock.

MSI (Master Sync Input) This pin should receive a low-to-high transition concurrent with each new PAM sample received at the receive filter input, ADI. A new transmit filter output sample will be presented at this time.

TXO (Transmit Bandpass Output — CD22413) This is the output of the transmit-bandpass filter. It is 100% duty cycle PAM at 8 kHz.

LPO (Transmit Lowpass Output — (CD22414) This is the output of the transmit-lowpass filter. It is 100% duty cycle PAM at 128 kHz.

TXI (Transmit Input) This is the transmit-filter input.

RXO (Receive Output) This pin is the output of the receive filter. It is 100% duty cycle PAM at the same frequency as the CCI pin, normally 128 kHz.

RXI (Receive Input) This is the receive filter input. It will accept 3/16 to 100% duty cycle PAM at 8 kHz.

V_{DD} Nominally 12 volts.

NOTE: Both VAG and VLS are high-impedance units.

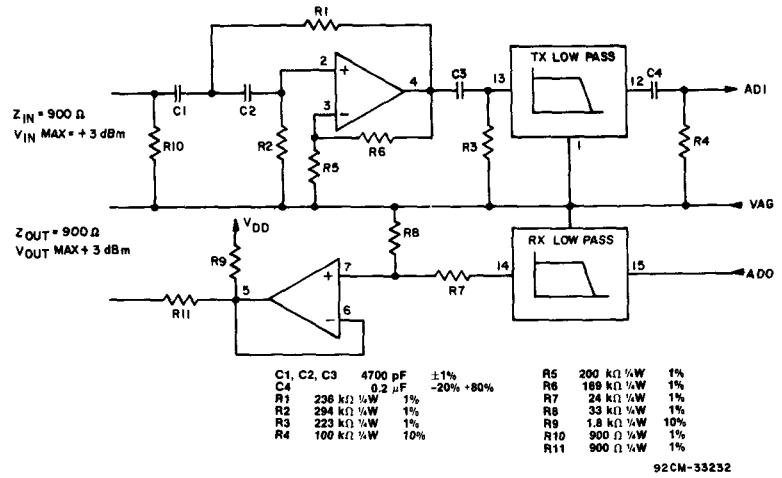


Fig. 12 - Filter schematic for CD22414 with 60-Hz rejection and 900-Ω termination.

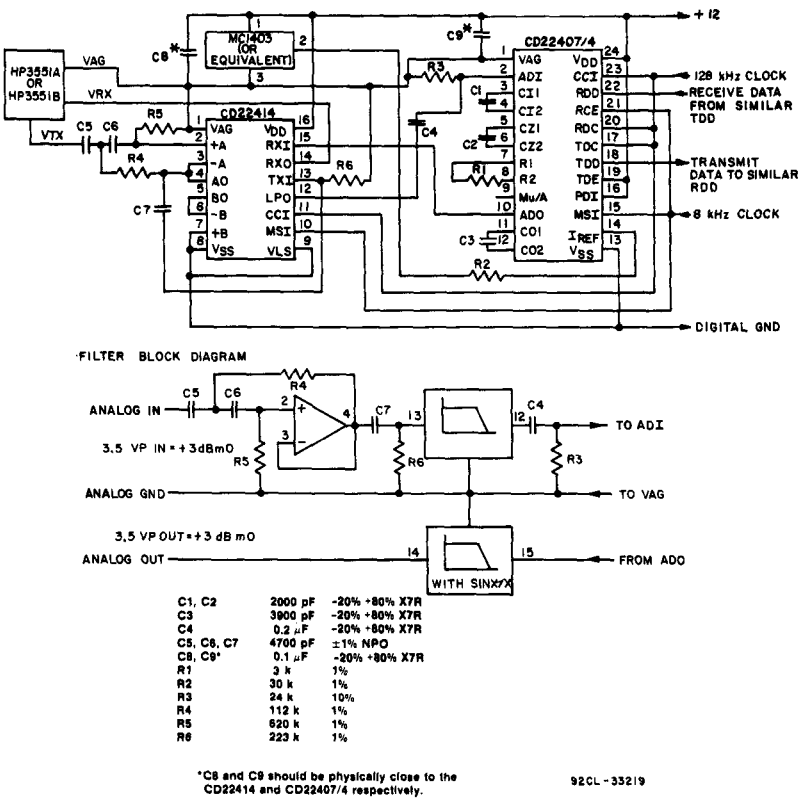


Fig. 13 - Analog transmission test circuit for CD22414 PCM filter and CD22407/CD22404 PCM CODEC.

TYPICAL END TO END PERFORMANCE OF RCA CODEC & FILTER

All measurements made using HP3779B PCM Test Set. See Fig. 13.

SPECIFICATION	Performance of CD22407/4 CODEC & CD22414 Filter	Bell System D3 Voice Freq. Requirements PUB 43801	CCITT G7.12 Voice Freq. Requirements
Channel Saturation	+3 dBm0	+3 dBm0	+3 dBm0
Gain Tracking with 1 kHz tone			
+3 to −40 dBm0	±0.3 dB	≤±0.5 dB	≤±0.5 dB
−40 to −50 dBm0	±0.6 dB	≤±1 dB	≤±1 dB
−55 dBm0	±2 dB	≤±3 dB	≤±3 dB
Quantizing Distortion @ 1 kHz			
+3 to −30 dBm0	37 dB	≥33 dB	>33 dB
−35 dBm0	34 dB	≥30 dB	≥30 dB
−40 dBm0	31 dB	≥27 dB	≥27 dB
−45 dBm0	26 dB	≥22 dB	≥22 dB
Idle Channel Noise with			
VTX = VAG	17 dBrnc0	≤23 dBrncO	≤−64 dBm0P
Quiet Code Noise (all 1's at decoder (RDD) Input)	15 dBrnc0	≤15 dBrnc0	≤−75 dBm0P
Selective Response @ multiples of 8 kHz	−60 dBm0	See Frequency Response	≤−50 dBm0
Frequency Response @ 0 dBm0 input			
50 Hz gain	−26 dB	—	≤−24 dB
60 Hz gain	−22 dB	≤−20 dB	—
200 to 300 Hz ripple	45 dB	≤0.6 dB	≤1 dB
3400 Hz gain	−1.6 dB	≥−3 dB	≥−1.8 dB
4000 Hz gain	−35 dB	≤−28 dB	≤−28 dB
≥4600 Hz gain	<−62 dB	≤−60 dB	≤−60 dB
Single Frequency Spurious Response			
In band with input 1 kHz @ 0 dBm	≤−44 dB	≤−40 dB	≤−40 dB
Out of band with input 0 to 12 kHz @ 0 dBm	≤−32.5 dB	≤−28 dB	≤−25 dB
Differential Delay Distortion			
1150 to 2300	58 μs	≤60 μs	—
1000 to 2500	72 μs	≤100 μs	—
900 to 2700	91 μs	≥200 μs	—

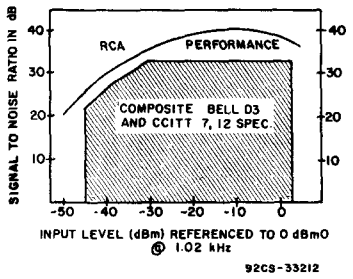


Fig. 14 - Signal-to-noise performance for CD22407 and CD22414. (See Fig. 13.)

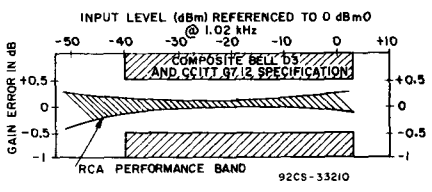


Fig. 15 - Gain tracking error for CD22407 and CD22414. (See Fig. 13.)

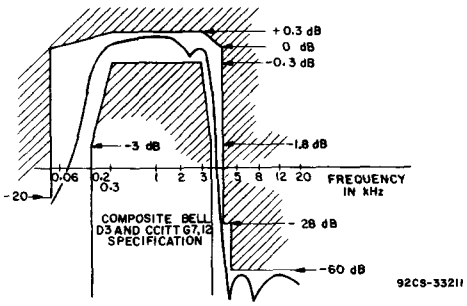


Fig. 16 - Frequency response of CD22407 and CD22414 CODEC and filter. (See Fig. 13.)

CMOS Dual-Tone Multifrequency Tone Generator

For Use in Dual-Tone Telephone Dialing Systems

Features

- *Mute drivers on chip*
- *Device power can either be regulated dc or telephone loop current*
- *Use of an inexpensive 3.579545-MHz TV crystal provides high accuracy and stability for all frequencies*

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE RANGE ($V_{DD} - V_{SS}$) ..... −0.5 to +12 V
INPUT VOLTAGE RANGE ..... −0.5 to V_{DD} +0.5 V
POWER DISSIPATION, P_D:
At T_A = −40 °C to +60 °C ..... 500 mW
At T_A = +60 °C to +85 °C ..... Derate Linearly at 12 mW/ °C to 200 mW
POWER DISSIPATION PER OUTPUT ..... 100 mW
OPERATING TEMPERATURE RANGE ..... −40 °C to +85 °C
LEAD TEMPERATURE DURING SOLDERING:
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm)
from case for 10 s max. ..... +265 °C

General Description

The RCA-CD22859 is a CMOS dual-tone multifrequency (DTMF) tone generator for use in dual-tone telephone dialing systems. The device can easily be interfaced to a standard pushbutton telephone keyboard, to provide enabling operation directly with the telephone lines.

The CD22859 generates standard DTMF sinusoidal dialing tones from an on-chip reference crystal oscillator. The reference oscillator uses an inexpensive 3.579545-MHz color TV crystal to create highly stable and accurate tones. The sinusoidal tones are digitally synthesized by a stair-step approximation.

One of four low-frequency band row tones and one of four high-frequency band column tones are selected by driving one of the four row inputs and one of the four column inputs low. Simultaneous selection of more than one row input and/or more than one column input will inhibit tone generation, or generate a single-tone sinusoid. These operating modes are described in the functional truth table.

Control logic is included to allow easy interface to standard K500-type telephones. Two CMOS outputs Tx, Rx, capable of driving external p-n-p receiver and transmitter muting transistors are provided. A low input to the CD pin, inhibits tone generation, turns off the reference oscillator, and causes Tx and Rx outputs to logic '0'. During tone generation mode, $\overline{CD}$ = 1 and Tx, Rx = logic 1.

All row, column, and $\overline{CD}$ inputs are provided with pull-up resistors to allow the use of SPST switch matrixes.

The CD22859 types are supplied in a 16-lead hermetic dual-in-line side-brazed ceramic package (D suffix), and a 16-lead dual-in-line plastic package (E suffix), and in chip form (H suffix).

DTMF Generator Functional Truth Table

	Inputs				Outputs		
Keyboard Mode	**Number of Column Inputs Activated "Low"**	**Number of Row Inputs Activated Low**	**$\overline{CD}$**	**Tone**	**OSC Running**	**RX**	**TX**
X	X	X	"0"	None	No	"0"	"0"
No key depressed	0	0	"1"	None	No	"0"	"0"
	0	1	"1"	Dual Tone R_a,C_1	Yes	"1"	"1"
	1,2,3, or 4	0	"1"	None	No	"0"	"0"
Normal Dialing One Key Depressed (See Note 1)	1	1	"1"	Dual Tone R_a,C_b	Yes	"1"	"1"
Two or More Keys In Same Row (See Note 2)	2,3, or 4	1	"1"	Single Row Tone R_a	Yes	"1"	"1"
Two or More Keys In Same Column	1	2,3, or 4	"1"	Single Column Tone C_b	Yes	"1"	"1"
Two or More Keys In Different Rows & Columns	2,3 or 4	1	"1"	None	Yes	"1"	"1"
	1		1	None	Yes	"1"	"1"

Where:
X = Do Not Care
R_a,C_b refers to Tone Output frequencies corresponding to Row 1, Row 2, Row 3, Row 4, Column 1, Column 2, Column 3, Column 4
a = 1,2,3,4 b = 1,2,3,4 a = b, or a ≠ b

1. Corresponds to normal dual-tone operation.
2. Corresponds to single-tone generation mode.

STATIC ELECTRICAL CHARACTERISTICS at $T_A = -25°C$ to $+60°C$

CHARACTERISTIC	V_{DD} (V)	V_O (V)	LIMITS Min.	LIMITS Max.	UNITS
Tone Outputs ($R_L = 82$)					
V_O; Dual-Tone Output	3.7-9.3		350	700	mV rms
$V_O(C_L)$; Single-Tone Output, Column*	3.7-9.3		300	—	mV rms
$V_O(R_L)$; Single-Tone Output, Row**	3.7-9.3		260	—	mV rms
Distortion (Note 1)	3.9-9.3		—	10	%
Rise and Fall Time (Dual-Tone Out) (Note 2)	3.9-9.3		—	5	ms
Pre-Emphasis (Note 3)	3.9-9.3		1	3	dB
Output Frequency (Note 4)	3.9-9.3		(Nom. − 1%)	(Nom. + 1%)	Hz
Mute Output Current					
Transmitter					
I_{OH} (Source)	1.7 10	1.2 9.5	−0.5 −3.4	— —	mA
I_{OL} (Sink)	10	2.5	—	10	μA
Receiver					
I_{OH} (Source)	1.7 10	1.2 9.5	−0.5 −3.4	— —	mA
I_{OL} (Sink)	10	2.5	—	10	μA

*Two or more row inputs low, and one column input low.

**Two or more column inputs low, and one row input low.

Notes:

1. Distortion is defined as: The ratio of all extraneous frequency components generated in the voiceband 0.5 kHz to 3 kHz, to the power of the dual-tone signal, measure across R_L.

$$= \frac{(V_1^2 + V_2^2 = \ldots + V_n^2)}{V_L^2 + V_H^2}$$

where $V_1, V_2, \ldots V_n$ are extraneous frequency components in the voiceband 0.5 kHz to 3 kHz, V_L is the low-band frequency tone, and V_H is the high-band frequency tone.

2. Tone rise time is defined as the time for each of the 2 DTMF frequencies to attain 90% of full amplitude, measured from the time when a row and column signal are driven low.
3. Pre-emphasis is the ratio of the high-group level to the low-group level.
4. Refer to Fig. 1 for standard DTMF frequencies.

DYNAMIC ELECTRICAL CHARACTERISTICS at $T_A = -25°C$ to $+60°C$
All voltages referenced to $V_{SS} = 0$ V.

CHARACTERISTIC	V_{DD}	LIMITS Min.	LIMITS Max.	UNITS
DC Supply Voltage				
Tone Generation Mode with Valid Input*		2.5	10	V
Non-Tone Generation**		1.7	10	V
Operating Current				
Tone Generation Mode (Outputs Unloaded)	3.7 V 9.3 V		1.7 13	mA
No Keydown Mode	3.7 V 9.3 V		100 200	μA
Input Pull-Up Current	3-10 V		400	μA
Input Low Voltage (V_{IL}) Max.	3-10 V		0.2 V_{DD}	V
Input High Voltage (V_{IH}) Min.	3-10 V	0.8 V_{DD}		V

*All logic and counters functional.

**Mute switches remain open.

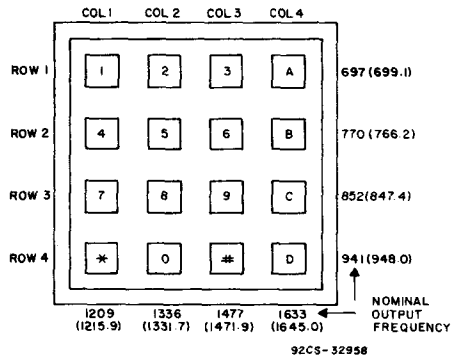
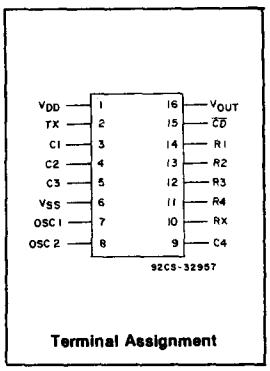


Fig. 1 - Bell and nominal output frequencies (in parenthesis) for 3.579545-MHz crystal.



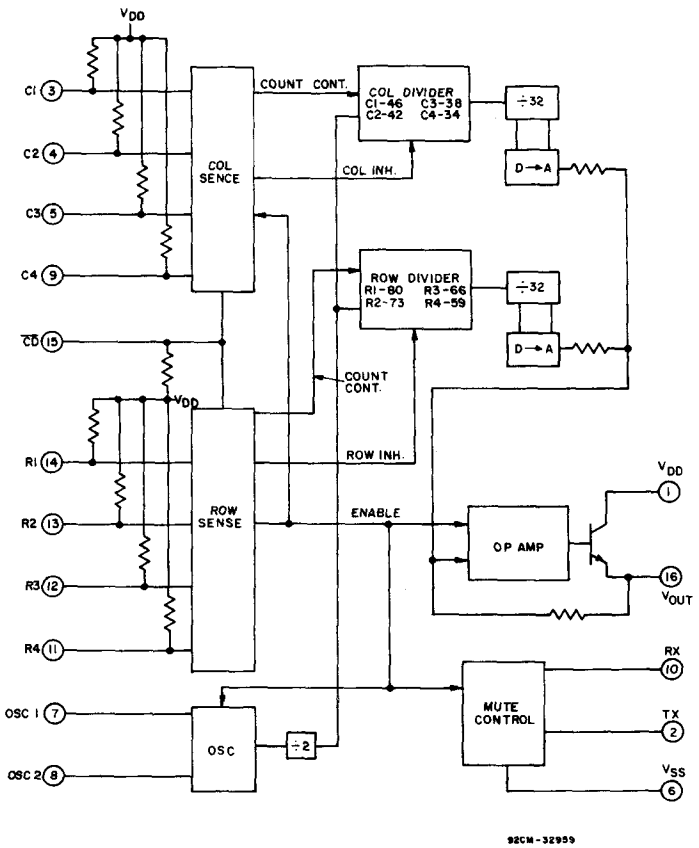


Fig. 2 - Touch-tone generator.

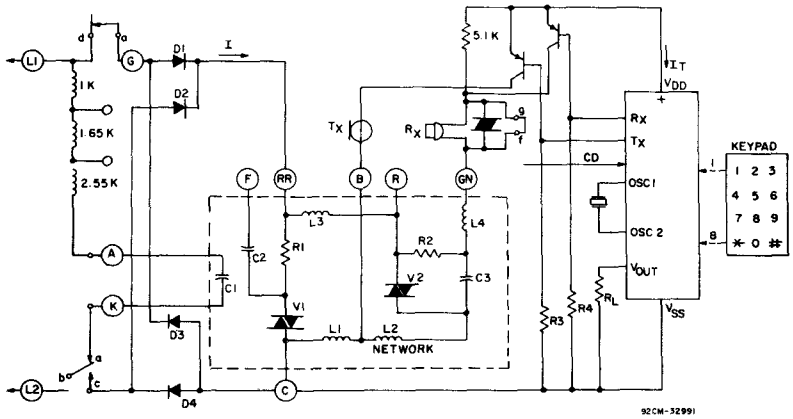
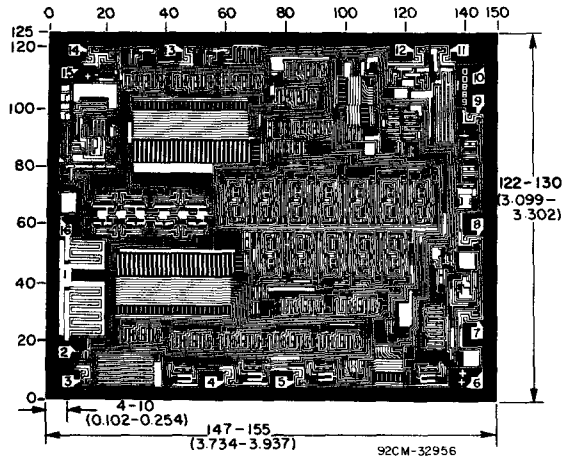


Fig. 3 - Interface with standard K500 telephone network.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

Dimensions and pad layout for CD22859H chip.

CMOS High-Speed 8-Bit Bidirectional CMOS/TTL Interface Level Converter

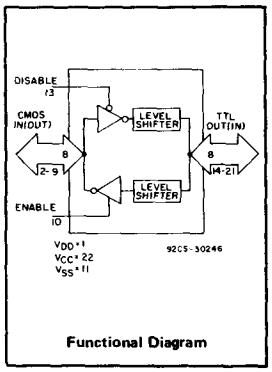
The RCA-CD40115 is a high-speed 8-bit integrated circuit designed to interface CMOS logic levels with TTL logic levels on the data bus of microprocessor-based systems. CMOS/TTL interface is provided by eight parallel bidirectional buffer/level converters. Buffer INPUT/OUTPUT terminals are either inputs or outputs depending on the desired direction of data flow. A low on both the ENABLE and DISABLE control inputs selects the direction of data flow from CMOS Inputs to TTL Outputs. A high on both control inputs selects the direction of data flow from TTL Inputs to CMOS Outputs. A low on the ENABLE and a high on the DISABLE inhibits data flow in either direction and places the CMOS Outputs in a high-impedance (3-state) mode.

The TTL Input/Output terminals and the ENABLE and DISABLE control inputs are TTL-compatible without the use of external pull-up resistors. The TTL input logic 0 to logic 1 transition occurs at a level of approximately 1.5 volts. The ENABLE and DISABLE inputs may be driven to the V_{DD} rail; therefore, either TTL or CMOS logic drivers, capable of sinking one TTL load, may be used to determine the direction of data flow. The large CMOS and TTL output buffers in this device have high output sink and source current capability and can drive the data bus capacitance with a transition time of approximately 0.1 ns/pF. This fast output transition time, together with the small propagation delay time of the device, allow high-speed operation.

The CD40115 is supplied in a 22-lead hermetic dual-in-line ceramic package.

Features:

- **Eight inverting channels with 5V-to-12V or 12V-to-5V level conversion**
- **Three operating modes:**
  - **CMOS-to-TTL level conversion**
  - **TTL-to-CMOS level conversion**
  - **Interface off; high-impedance CMOS input/output**
- **Low propagation delay time:**
  - **CMOS-to-TTL conversion – 10 ns typ.**
  - **TTL-to-CMOS conversion – 30 ns typ.**
- **High TTL sink current – 30 mA typ.**
- **No external TTL input pull-up resistors *required***
- **High speed drive of large data bus capacitances**
- **Input/output and power supply terminals located for ease of PC board layout**



Functional Diagram

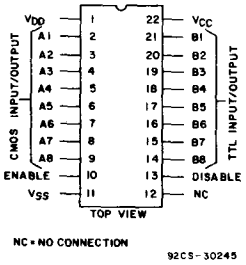
Applications:

- **Interface CMOS microprocessor with TTL memories and peripheral devices**
- ***Interface between and within logic systems which combine CMOS and TTL devices***

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (Voltages referenced to VSS Terminal)

V_{DD}	−0.5 to +12.6 V
V_{CC}	−0.5 to +6 V
INPUT VOLTAGE RANGE:	
Data Inputs, CMOS to TTL	−0.5 to V_{DD}+0.5 V
Data Inputs, TTL to CMOS	−0.5 to V_{CC}+0.5 V
Enable, Disable Inputs	−0.5 to V_{DD}+0.5 V
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −55°C to +100°C	500 mW
For T_A = +100 to +125°C	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
For T_A = Full Package-Temperature Range	100 mW
OPERATING TEMPERATURE RANGE (T_A)	−55 to +125°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance of 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C



TERMINAL ASSIGNMENT

TRUTH TABLE

ENABLE	DISABLE	FUNCTION
0	0	Convert CMOS Level to TTL Level
1	1	Convert TTL Level to CMOS Level
0	1	High Impedance (Z)
1	0	Invalid*

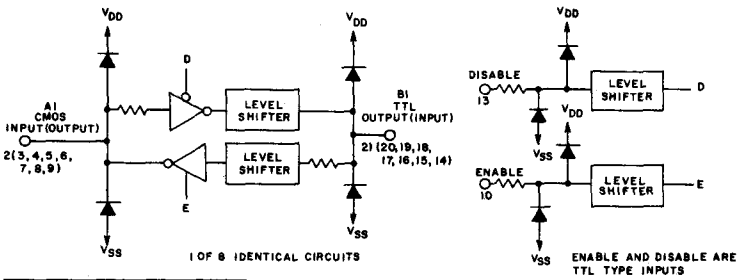
0 = Low Level 1 = High Level

Z = High Impedance on CMOS Output side; TTL side are inputs.

INVALID = Both CMOS and TTL sides are ON as outputs.

See Operating and Handling Considerations – Bypassing and Unused Inputs.

* Excessively high currents from V_{DD} to V_{SS} could flow in this mode during power turn-on or turn-off if other IC's drive into the bus lines (on either the TTL or CMOS side). *This high current condition could occur during a* transient or steady-state invalid mode.



Input (Output)		Output (Input)	
Data	Terminal No.	Data	Terminal No.
A1	2	B1	21
A2	3	B2	20
A3	4	B3	19
A4	5	B4	18
A5	6	B5	17
A6	7	B6	16
A7	8	B7	15
A8	9	B8	14

Fig. 1 – Functional block diagram.

STATIC ELECTRICAL CHARACTERISTICS At T_A = 25°C, V_{DD} = 12 V, V_{CC} = 5 V

CHARACTERISTIC		TEST CONDITIONS	TYPICAL VALUES	UNITS
Data Flow – CMOS Inputs to TTL Outputs				
Quiescent Device Current, From V_{DD} Supply,	I_{DD}		4	mA
From V_{CC} Supply,	I_{CC}		5	μA
Input Current,	I_{IN}	V_{IN}=0,12 V; Any CMOS input	±50	μA
Output Current,	I_{OH}	V_{OH}=3 V, V_{IL}=2 V	15	mA
	I_{OL}	V_{OL}=0.4 V, V_{IH}=10 V	30	
Data Flow – TTL Inputs to CMOS Outputs				
Quiescent Device Current, From V_{DD} Supply,	I_{DD}		4	mA
From V_{CC} Supply,	I_{CC}		5	μA
Input Current,	I_{IL}	V_{IL}=0 to 0.7 V; Any TTL input	−250	μA
	I_{IH}	V_{IH}=2.3 V; Any TTL input	−50	
Output Current,	I_{OH}	V_{OH}=11.5 V, V_{IL}=0.7 V	20	mA
	I_{OL}	V_{OL}=0.5 V, V_{IH}=2.3 V	20	
CMOS 3-State Output Leakage Current,	I_{OUT}	V_O=0,12 V, V_{IN}=0,5 V	±50	μA
Enable and Disable Inputs				
Input Current,	I_{IL}	V_{IL}=0 to 0.7 V	−250	μA
	I_{IH}	V_{IH}=2.3 V (TTL)	−50	
	I_{IH}	V_{IH}=12 V (CMOS)	50	

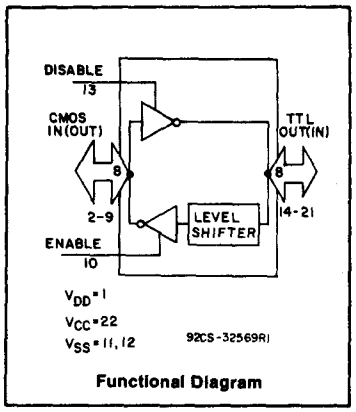
DYNAMIC ELECTRICAL CHARACTERISTICS At T_A = 25°C, V_{DD} = 12 V, V_{CC} = 5 V

CHARACTERISTIC	TEST CONDITIONS		TYPICAL VALUES		UNITS
	INPUT	OUTPUT	C_L=50 pF	C_L=200 pF	
Propagation Delay Times, Data-In to Data-Out, t_{PHL}, t_{PLH}	CMOS	TTL	10	15	ns
	TTL	CMOS	30	40	
Enable or Disable to Data-Out, t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL}			35		ns
Transition Time, t_{THL}, t_{TLH}	CMOS	TTL	10	15	ns
	TTL	CMOS	10	15	

CMOS High-Speed 8-Bit Bidirectional CMOS/TTL Interface Level Converter

Features:

- *Eight inverting channels with conversion from V_{DD} to V_{CC} or V_{CC} to V_{DD} ($4\ V \leq V_{DD} \leq 12\ V$ and $4\ V \leq V_{CC} \leq V_{DD}$)*
- *Three operating modes:*
  CMOS-to-TTL level conversion
  TTL-to-CMOS level conversion
  Interface off; high-impedance on both sides



Functional Diagram

The RCA-CD40116 is a high-speed 8-bit integrated circuit designed to interface CMOS logic levels with TTL logic levels on the data bus of microprocessor-based systems. CMOS/TTL interface is provided by eight parallel bidirectional buffer/level converters. Buffer INPUT/OUTPUT terminals are either inputs or outputs depending on the desired direction of data flow.

A low level on the DISABLE input with the ENABLE input either high or low, permits conversion of CMOS inputs to TTL outputs. A high level on both the DISABLE and ENABLE inputs permits data flow from TTL inputs to CMOS outputs. A low level on the ENABLE input and a high level on the DISABLE input sets both inputs/outputs to the high-impedance state.

The TTL Input/Output terminals and the ENABLE and DISABLE control inputs are TTL-compatible without the use of external pull-up resistors. The TTL input logic 0 to logic 1 transition occurs at a level of approximately 1.5 volts. The ENABLE and DISABLE inputs may be driven to the V_{DD} rail; therefore, either TTL or CMOS logic drivers, capable of sinking one TTL load, may be used to determine the direction of data flow. The large CMOS and TTL output buffers in this device have high output sink and source current capability and can drive the data bus capacitance with a transition time of approximately 0.25 ns/pF. This fast output transition time, together with the small propagation delay time of the device, allow high-speed operation.

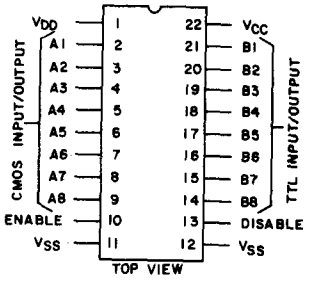
Pin 12 is an additional V_{SS} Pin which is connected directly to the TTL-to-CMOS converters to avoid oscillation in these amplifiers. Pin 12 is connected to Pin 11 through a poly resistor which isolated Pin 12 from V_{SS} switching noise (groung noise).

The CD40116 is supplied in a 22-lead hermetic dual-in-line ceramic package (D suffix), 22-lead plastic package (E suffix), and in chip form (H suffix).

- *Low propagation delay time:*
  CMOS-to-TTL conversion - 25 ns typ.
  TTL-to-CMOS conversion - 30 ns typ.
  (V_{DD} = 12 V, V_{CC} = 5 V)
- *High TTL sink current - 11 mA typ.*
- *No external TTL input pull-up resistors required*
- *High speed drive of large data bus capacitances*
- *Input/output and power supply terminals located for ease of PC board layout*

Applications:

- *Interface CMOS microprocessor with TTL memories and peripheral devices*
- *Interface between and within logic systems which combine CMOS and TTL devices*



TERMINAL ASSIGNMENT

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE (Voltage reference to V_{SS} Terminal)
- V_{DD} ..... -0.5 to + 12.8 V*
- V_{CC} ..... -0.5 to V_{DD}

INPUT VOLTAGE RANGE:
- Data Inputs, CMOS to TTL ..... -0.5 to V_{DD} + 0.5 V
- Data Inputs, TTL to CMOS ..... -0.5 to V_{CC} + 0.5 V
- Enable, Disable Inputs ..... -0.5 to V_{DD} + 0.5 V

POWER DISSIPATION PER PACKAGE (P_D):
- For T_A = -40°C to + 60°C (E) ..... 500 mW
- For T_A = + 60°C to + 85°C (E) ..... Derate linearly at 12 mW/°C to 200 mW
- For T_A = -55°C to + 100°C (D) ..... 500 mW
- For T_A = + 100 to + 125°C (D) ..... Derate linearly at 12 mW/°C to 200 mW

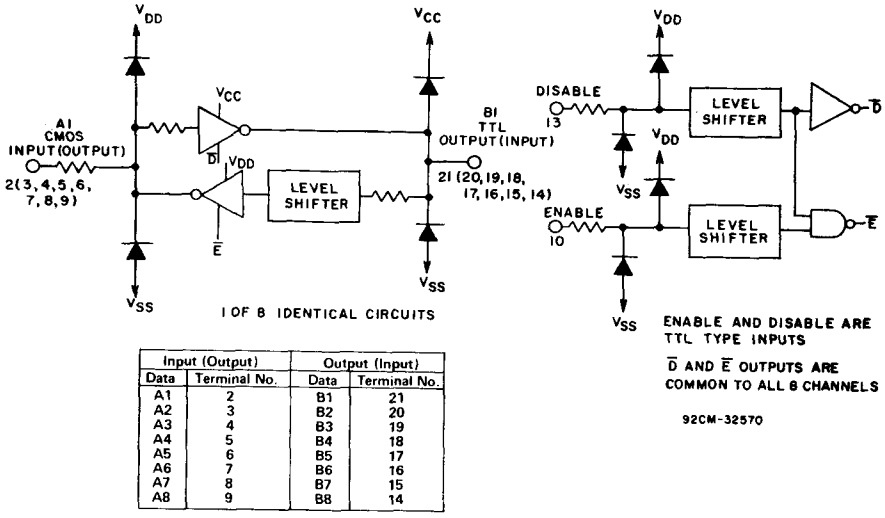
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
- For T_A = Full Package-Temperature Range ..... 100 mW

OPERATING TEMPERATURE RANGE (T_A)
- Package Type D ..... -55 to + 125°C
- Package Type E ..... -40 to + 85°C

STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65 to + 150°C

LEAD TEMPERATURE (DURING SOLDERING):
- At distance of 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max ..... + 265°C

*At 125°C V_{DD} should not exceed +12 V.



Input (Output)		Output (Input)	
Data	Terminal No.	Data	Terminal No.
A1	2	B1	21
A2	3	B2	20
A3	4	B3	19
A4	5	B4	18
A5	6	B5	17
A6	7	B6	16
A7	8	B7	15
A8	9	B8	14

Fig. 1 - Functional block diagram.

TRUTH TABLE

ENABLE	DISABLE	FUNCTION
X	0	Convert CMOS Level to TTL Level
1	1	Convert TTL Level to CMOS Level
0	1	High Impedance (Z)

0 = Low Level 1 = High Level X = Don't Care

Z = High Impedance on both CMOS and TTL sides.

See Operating and Handling Considerations — Bypassing and Unused Inputs.

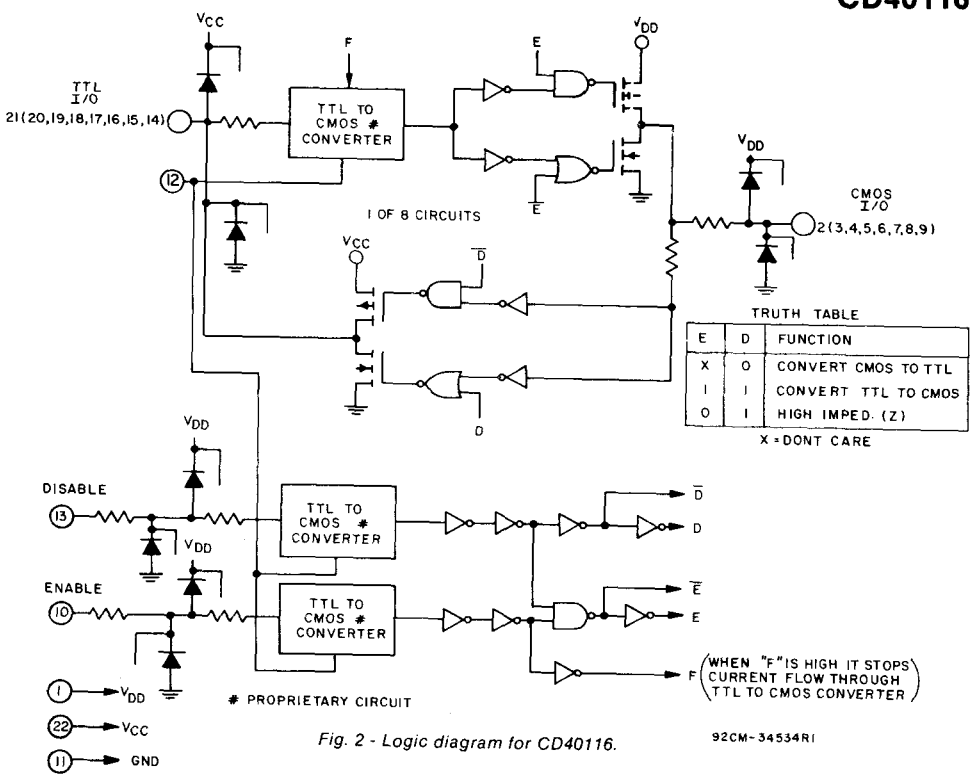


Fig. 2 - Logic diagram for CD40116.

STATIC CHARACTERISTICS V_{DD} = 12 V, V_{CC} = 5 V

CHARACTERISTIC	TEST CONDITIONS	Limits at Indicated Temperatures (°C) Values at -55, +25, +125 for D, H Packages Values at -40, +25, +85 for E Packages							UNITS
		-55	-40	+85	+125	+25 MIN.	+25 TYP.	+25 MAX.	
Quiescent Device Current, From V_{DD} Supply, I_{DD} MAX	ENABLE = 1	5	5	5	5	—	1	5	mA
	ENABLE = 0	5	5	5	5	—	0.2	5	
From V_{CC} Supply, I_{CC} MAX		100	100	200	200	—	5	100	μA
Data Flow — CMOS Inputs to TTL Outputs									
Input Current, I_{IN} MAX	V_{IN} = 0, 12 V; Any CMOS input	±60	±60	±60	±60	—	±5	±60	μA
Output Current, I_{OH} MIN	V_{OH} = 3 V, V_{IL} = 2 V	-7.5	-7	-4.9	-4.2	-6	-12	—	mA
I_{OL} MIN	V_{OL} = 0.4 V, V_{IH} = 10 V	7.5	7	4.9	4.2	6	11	—	
TTL 3-State Output Leakage Current I_{OUT} MAX	ENABLE = 1	-500	-500	-500	-500	—	-250	-500	μA
	ENABLE = 0	±100	±100	±100	±100	—	±5	±100	μA
Data Flow — TTL Inputs to CMOS Outputs									
Input Current, I_{IL} MAX	V_{IL} = 0 to 0.7 V;	-500	-500	-500	-500	—	-250	-500	μA
I_{IH} MAX	V_{IH} = 2.3 V;	-450	-350	-350	-350	—	-175	-350	
I_{IH} MAX	V_{IH} = 5 V; Any TTL input	+100	+100	+100	+100	—	+50	+100	
Output Current, I_{OH} MIN	V_{OH} = 11.5 V, V_{IL} = 0.7 V	-4.3	-4.2	-2.9	-2.5	-3.5	-6.5	—	mA
I_{OL} MIN	V_{OL} = 0.5 V, V_{IH} = 2.3 V	4.3	4.2	2.9	2.5	3.5	6.5	—	
CMOS 3-State Output Leakage Current I_{OUT} MAX	V_O = 0, 12 V, V_{IN} = 0, 5 V	±60	±60	±60	±60	—	±5	±60	μA
Enable and Disable Inputs									
Input Current, I_{IL} MAX	V_{IL} = 0 to 0.7 V	-500	-500	-500	-500	—	-250	-500	μA
I_{IH} MAX	V_{IH} = 2.3 (TTL)	-450	-350	-350	-350	—	-175	-350	
I_{IH} MAX	V_{IH} = 12 V (CMOS)	60	60	60	60	—	5	60	

DYNAMIC ELECTRICAL CHARACTERISTICS AT T_A = 25°C; V_{DD} = 12 V, V_{CC} = 5 V

CHARACTERISTIC	TEST CONDITIONS		LIMITS			UNITS
	INPUT	OUTPUT	C_L = 50 pF		C_L = 200 pF	
			TYP	MAX	TYP	
Propagation Delay Times, Data-In to Data-Out, t_{PHL}, t_{PLH}	CMOS	TTL	25	35	35	ns
	TTL	CMOS	30	45	50	
Disable to TTL Out, $t_{PHZ/LZ}$			30	45	30	ns
$t_{PZH/ZL}$			35	50	35	
Enable to CMOS Out, $t_{PHZ/LZ}$			20	30	20	ns
$t_{PZH/ZL}$			45	60	45	
Transition Time, t_{THL}, t_{TLH}	CMOS	TTL	20	40	55	ns
	TTL	CMOS	20	40	55	

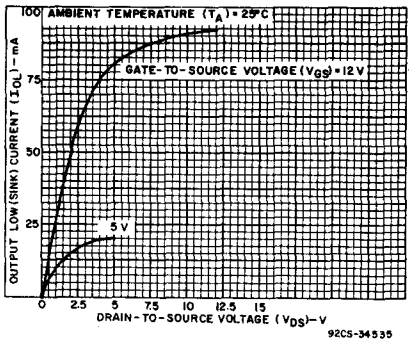


Fig. 3 - Typical N-Channel output low (sink) current characteristics - CMOS to TTL.

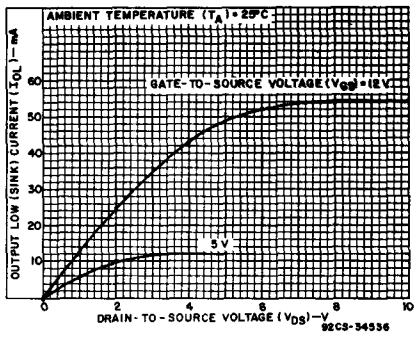


Fig. 4 - Typical output low (sink) current characteristics - TTL to CMOS.

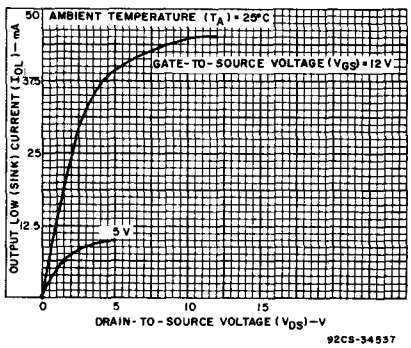


Fig. 5 - Minimum N-Channel output low (sink) current characteristics - CMOS

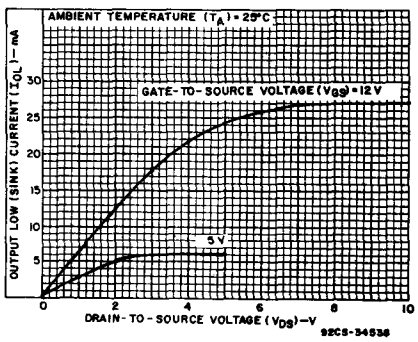


Fig. 6 - Minimum output low (sink) current characteristics - TTL to CMOS.

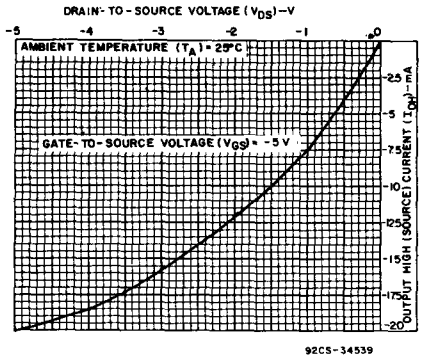


Fig. 7 - Typical P-channel output high (source) current characteristics - CMOS to TTL.

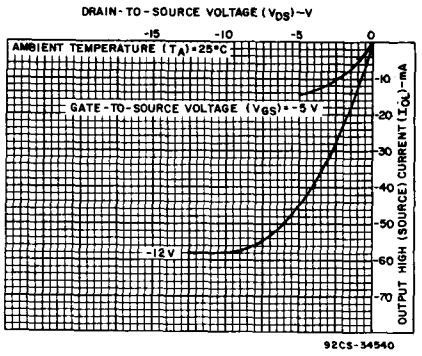


Fig. 8 - Typical output high (source) current characteristics - TTL to CMOS.

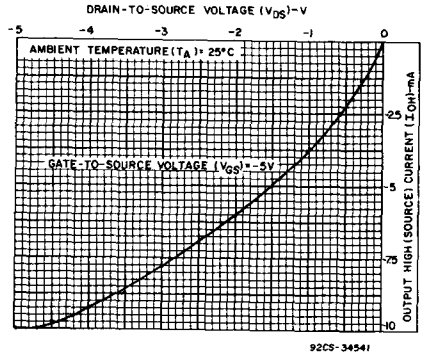


Fig. 9 - Minimum P-Channel output high (source) current characteristic - CMOS to TTL.

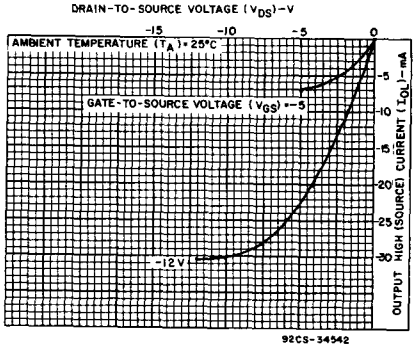


Fig. 10 - Minimum output high (source) current characteristics - TTL to CMOS.

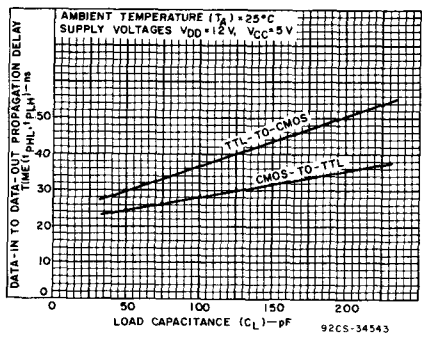


Fig. 11 - Typical DATA-IN to DATA-OUT propagation delay as a function of load capacitance.

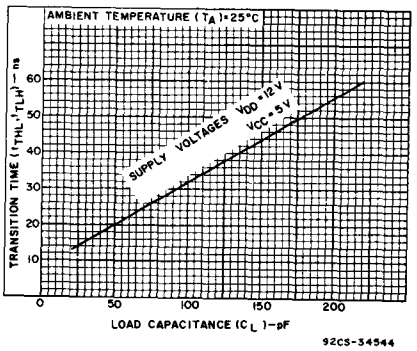


Fig. 12 - Typical transition time as a function of load capacitance CMOS-to-TTL or TTL-to-CMOS.

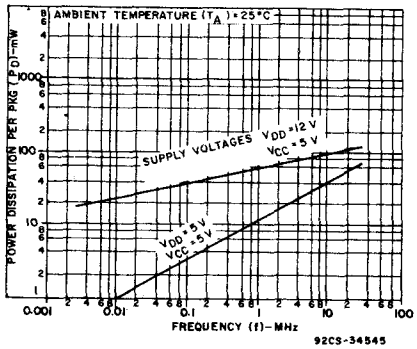


Fig. 13 - Power dissipation as a function of frequency - CMOS to TTL.

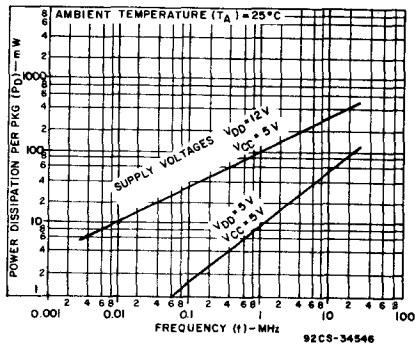
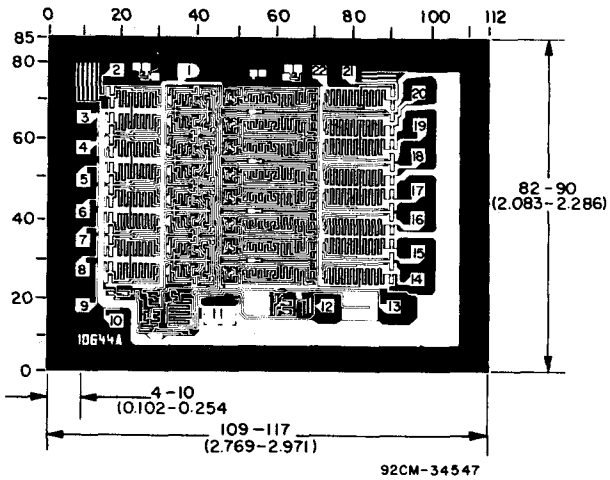


Fig. 14 - Power dissipation as a function of frequency - TTL to CMOS.



The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

Dimensions in parentheses are in millimeters and are derived from the basis inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and Pad Layout for CD40116H