CMOS 21-Stage Counter

High-Voltage Types (20-Volt Rating)

The RCA-CD4045B is a timing circuit consisting of 21 counter stages, two output-shaping flip-flops, two inverter output drivers, and input inverters for use in a crystal oscillator. The CD4045B configuration provides 21 flip-flop counting stages, and two flip-flops for shaping the output waveform for a 3.125% duty cycle. Push-pull operation is provided by the inverter output drivers.

The first inverter is intended for use as a crystal oscillator/amplifier. However, it may be used as a normal logic inverter if desired. A crystal oscillator circuit can be made less sensitive to voltage-supply variations by the use of source resistors. In this device, the sources of the p and n transistors have been brought out to package terminals. If external resistors are not required, the sources must be shorted to their respective substrates (S_p to V_{DD}, S_n to V_{SS}). See Fig. 1. The first inverter in conjunction with an outboard inverter, such as 1/6 CD4069, and R_X, C_X, and R_S can also be used to construct an RC oscillator. The following data is supplied as a guide in the selection of values for R_X, R_S, and C_X used in Fig. 11:

1. R_X max = 10 MΩ with R_S = 10 MΩ and C_X = 50 pF
2. C_X max = 25 μF with R_S = 560 kΩ and R_X = 50 kΩ

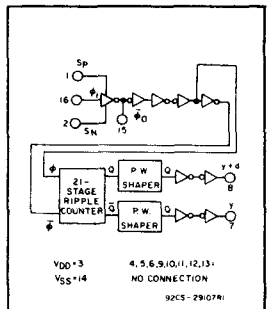
The CD4045B types are supplied in 16-lead dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

Applications:

- **Digital equipment in which ultra-low dissipation and/or operation using a battery source is required.**
- **Accurate timing from a crystal oscillator for timing applications such as wall clocks, table clocks, automobile clocks, and digital timing references in any circuit requiring accurately timed outputs at various intervals in the counting sequence.**
- **Driving miniature synchronous motors, stepping motors, or external bipolar transistors in push-pull fashion.**

Features:

- **Very low operating dissipation . . . . . <1 mW (typ.) @ V_{DD} = 5 V, fφ = 1 MHz**
- **Output drivers with sink or source capability . . . . . 7 mA (typ.) @ V_{DD} = 5 V**
- **Medium speed (typ.) . . . fφ = 25 MHz @ V_{DD} = 10 V**
- **100% tested for quiescent current at 20 V**
- **5-V, 10-V, and 15-V parametric ratings**
- **Meets all requirements of JEDEC Tentative Standard No. 13A, Standard Specifications for Descripiton of 'B' Series CMOS Devices"**



FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	−0.5 to +20 V
INPUT VOLTAGE RANGE, ALL INPUTS	−0.5 to V_{DD} +0.5 V
DC INPUT CURRENT, ANY ONE INPUT	±10 mA
POWER DISSIPATION PER PACKAGE (P_D):	
For T_A = −40 to +60°C (PACKAGE TYPE E)	500 mW
For T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
For T_A = −55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
For T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100 mW
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	−55 to +125°C
PACKAGE TYPE E	−40 to +85°C
STORAGE TEMPERATURE RANGE (T_{stg})	−65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

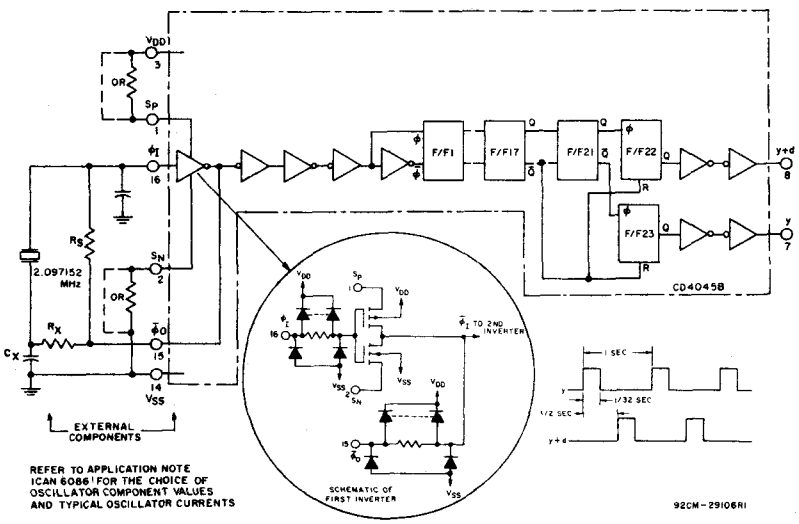


Fig. 1 – CD4045B and outboard components in a typical 21-stage counter application.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C) Values at −55, +25, +125 Apply to D, F, K, H Packages Values at −40, +25, +85, Apply to E Package							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Quiescent Device Current, I_{DD} Max.	–	0,5	5	5	5	150	150	–	0.04	5	μA
	–	0,10	10	10	10	300	300	–	0.04	10	
	–	0,15	15	20	20	600	600	–	0.04	20	
	–	0,20	20	100	100	3000	3000	–	0.08	100	
Output Low (Sink) Current I_{OL} Min.	0.4	0,5	5	4.5	4.3	2.9	2.5	3.6	7	–	mA
	0.5	0,10	10	11.2	10.5	7.7	6.3	9.1	18	–	
	1.5	0,15	15	29.4	28	19.6	16.8	23.8	47	–	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	−4.5	−4.3	−2.9	−2.5	−3.6	−7	–	
	9.5	0,10	10	−11.2	−10.5	−7.7	−6.3	−9.1	−18	–	
	13.5	0,15	15	−29.4	−28	−19.6	−16.8	−23.8	−47	–	
Pin 15 Output Low and High Current, I_{OL}, I_{OH}	0.4,4.6	0,5	5	–				±0.1	±0.18	–	mA
	0.5,9.5	0,10	10	–				±0.2	±0.3	–	
	1.5,13.5	0,15	15	–				±0.5	±1	–	
Output Voltage: Low-Level, V_{OL} Max.	–	0,5	5	0.05				–	–	0.05	V
	–	0,10	10	0.05				–	–	0.05	
	–	0,15	15	0.05				–	–	0.05	
Output Voltage: High-Level, V_{OH} Min.	–	0,5	5	4.95				4.95	5	–	
	–	0,10	10	9.95				9.95	10	–	
	–	0,15	15	14.95				14.95	15	–	
Input Low Voltage V_{IL} Max.	0.5,4.5	–	5	1.5				–	–	1.5	V
	1,9	–	10	3				–	–	3	
	1.5,13.5	–	15	4				–	–	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	–	5	3.5				3.5	–	–	
	1,9	–	10	7				7	–	–	
	1.5,13.5	–	15	11				11	–	–	
Input Current I_{IN} Max.	–	0,18	18	±0.1	±0.1	±1	±1	–	$±10^{-5}$	±0.1	μA

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges

CHARACTERISTIC	V_{DD} (V)	LIMITS Min.	LIMITS Max.	UNITS
Supply-Voltage Range (For T_A = Full Package-Temperature Range)	–	3	18	V
Minimum Input-Pulse Width, t_W	5	–	100	ns
	10	–	50	
	15	–	40	
Maximum Input–Pulse Frequency, fϕ (External Pulse Source)	5	5	–	MHz
	10	12	–	
	15	15	–	

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = 25°C; Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200 kΩ

CHARACTERISTIC	TEST CONDITIONS	V_{DD} V	LIMITS Min.	Typ.	Max.	UNITS
Propagation Delay Time: ϕ_I to y or y+d out t_{PHL}, t_{PLH}		5	–	2.2	5.5	μs
		10	–	0.9	2.7	
		15	–	0.65	2	
Transition Time: t_{THL}, t_{TLH}		5	–	25	50	ns
		10	–	13	25	
		15	–	10	20	
Minimum Input-Pulse Width t_W		5	–	50	100	ns
		10	–	25	50	
		15	–	20	40	
Input-Pulse Rise or Fall Time: $t_r\phi$, $t_f\phi$		5	–	–	500	μs
		10	–	–	500	
		15	–	–	500	
Maximum Input-Pulse Frequency: (External Pulse Source) f_ϕ		5	5	10	–	MHz
		10	12	25	–	
		15	15	30	–	
Input Capacitance, C_{IN}	Any Input		–	5	7.5	pF
Variation of Output Frequency (Unit-to-Unit)	f = 5 MHz	5	–	0.05	–	%
		10	–	0.03	–	
		15	–	0.1	–	
RC Oscillator Operation						
Maximum Oscillator Frequency (See Fig. 11) f_{osc}	R_X = 50 kΩ, R_S = 560 kΩ, C_X = 50 pF	5	45	60	75	kHz
		10	45	60	75	
		15	45	60	75	

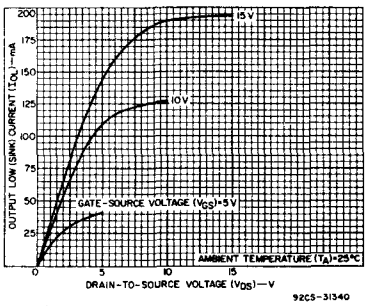


Fig. 2 – Typical output low (sink) current characteristics.

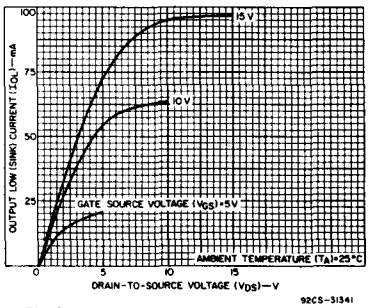


Fig. 3 – Minimum output low (sink) current characteristics.

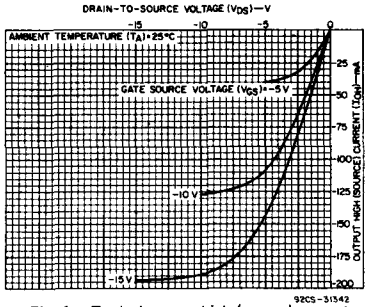


Fig. 4 – Typical output high (source) current characteristics.

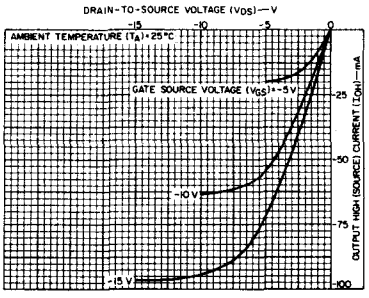


Fig. 5 – Minimum output high (source) characteristics.

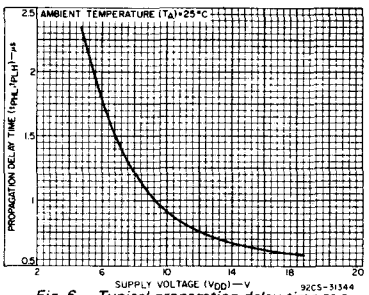


Fig. 6 – Typical propagation delay time as a function of supply voltage (ϕ_I to y or y + d out vs. V_{DD}).

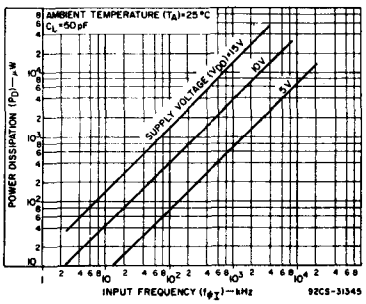


Fig. 7 – Typical power dissipation as a function of input frequency (21 counting stages).

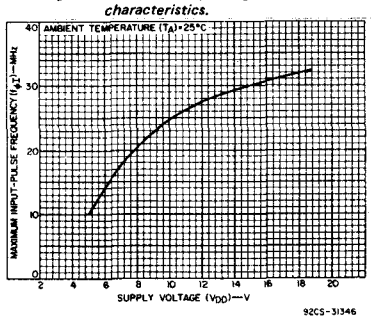


Fig. 8 – Typical maximum input-pulse frequency as a function of supply voltage.

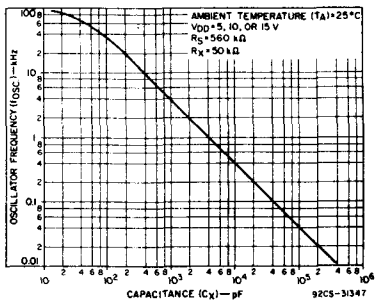


Fig. 9 – Typical RC oscillator frequency as a function of capacitance (C_X), See Fig. 11.

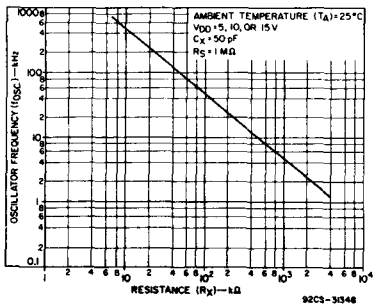


Fig. 10 – Typical RC oscillator frequency as a function of resistance (R_X), See Fig. 11.

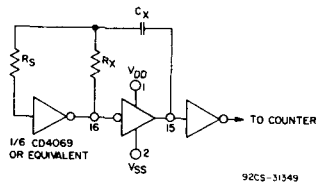


Fig. 11 – Typical RC circuit.

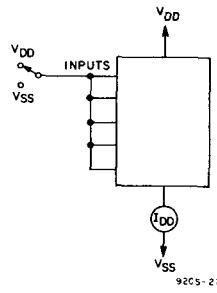


Fig. 12 – Quiescent-device-current test circuit.

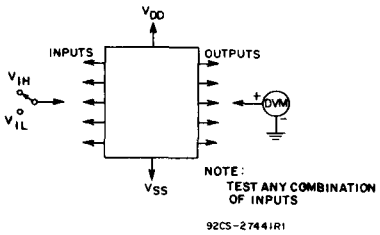


Fig. 13 – Noise-immunity test circuit.

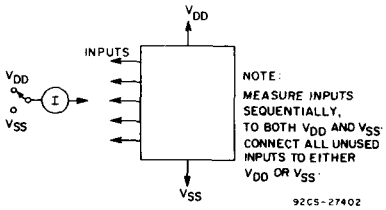


Fig. 14 – Input-leakage-current test circuit.

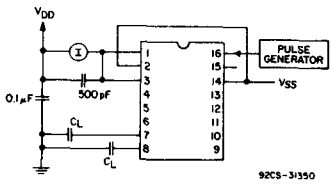
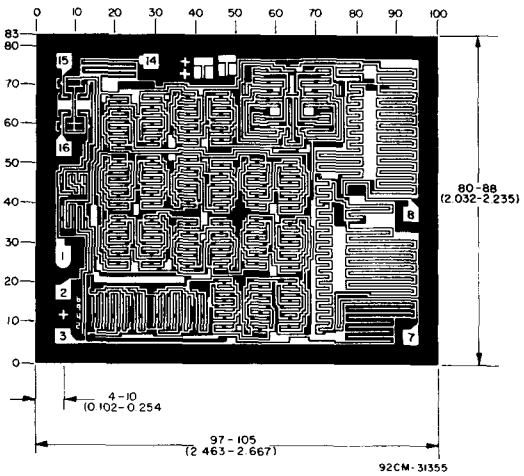


Fig. 15 – Dynamic power dissipation test circuit.

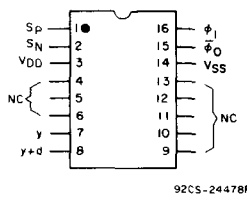


Dimensions and pad layout for CD4045B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

The photographs and dimensions of each CMOS chip represent a chip when it is part of the wafer. When the wafer is separated into individual chips, the angle of cleavage may vary with respect to the chip face for different chips. The actual dimensions of the isolated chip, therefore, may differ slightly from the nominal dimensions shown. The user should consider a tolerance of −3 mils to +16 mils applicable to the nominal dimensions shown.

TERMINAL DIAGRAM
Top View



NC = NO CONNECTION

NOTE Observe power-supply terminal connections, V_{DD} is terminal No. 3 and V_{SS} is terminal No. 14 (not 16 and 8 respectively, as in other CD4000B Series 16-lead devices).