CD4046A Types

CMOS Micropower Phase-Locked Loop

The RCA-CD4046A CMOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat packages (K suffix), and in chip form (H suffix).

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the RCA-CD4024, CD4018, CD4020, CD4022, CD4029, and CD4059. One or more CD4018 (Presettable Divide-by-N Counter) or CD4029 (Presettable Up/Down Counter), or CD4059A (Programmable Divide-by-"N" Counter), together with the CD4046A (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0" ≤30% ($V_{DD}-V_{SS}$), logic "1" ≥ 70% ($V_{DD}-V_{SS}$)]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analagously to an over-driven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator I supplies the averaged voltage to the VCO input, and causes the VCO to oscillate at the center frequency (f_o).

The frequency range of input signals on which the PLL will lock if it was initially out of lock is defined as the frequency capture range ($2f_C$).

The frequency range of input signals on which the loop will stay locked if it was initially in lock is defined as the frequency lock range ($2f_L$). The capture range is ≤ the lock range.

With phase comparator I the range of frequencies over which the PLL can acquire lock (capture range) is dependent on the low-pass-filter characteristics, and can be made as large as the lock range. Phase-comparator I enables a PLL system to remain in lock in spite of high amounts of noise in the input signal.

One characteristic of this type of phase comparator is that it may lock onto input frequencies that are close to harmonics of the VCO center-frequency. A second characteristic is that the phase angle between the signal and the comparator input varies between 0° and 180°, and is 90° at the center frequency. Fig. 2 shows the typical, triangular, phase-to-output response characteristic

Features:

- **Very low power consumption: 70 µW (typ.) at VCO f_o = 10 kHz, V_{DD} = 5 V**
- **Operating frequency range up to 1.2 MHz (typ.) at V_{DD} = 10 V**
- **Wide supply-voltage range: $V_{DD} - V_{SS}$ = 5 to 15 V**
- **Low frequency drift: 0.06%/°C (typ.) at V_{DD} = 10 V**
- **Choice of two phase comparators:**
  1. **Exclusive-OR network**
  2. **Edge-controlled memory network with phase-pulse output for lock indication**
- **High VCO linearity: 1% (typ.)**
- **VCO inhibit control for ON-OFF keying and ultra-low standby power consumption**
- **Source-follower output of VCO control input (Demod. output)**
- **Zener diode to assist supply regulation**
- **Quiescent current specified to 15 V**
- **Maximum input leakage current of 1 µA at 15 V (full package-temperature range)**

Applications:

- **FM demodulator and modulator**
- **Frequency synthesis and multiplication**
- **Frequency discriminator**
- **Data synchronization**
- **Voltage-to-frequency conversion**
- **Tone decoding**
- **FSK – Modems**
- **Signal conditioning**
- **(See ICAN-6101) "RCA CMOS Phase-Locked Loop – A Versatile Building Block for Micropower Digital and Analog Applications"**

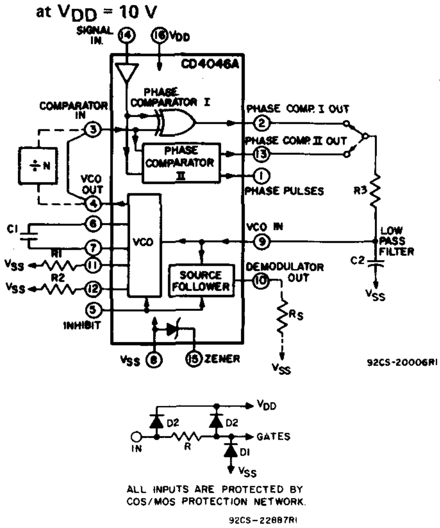


Fig. 1 – COS/MOS phase-locked loop block diagram.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg})	–65 to +150°C
OPERATING-TEMPERATURE RANGE (T_A):	
PACKAGE TYPES D, F, K, H	–55 to +125°C
PACKAGE TYPE E	–40 to +85°C
DC SUPPLY-VOLTAGE RANGE, (V_{DD}) (Voltages referenced to V_{SS} Terminal)	–0.5 to +15 V
POWER DISSIPATION PER PACKAGE (P_D):	
FOR T_A = –40 to +60°C (PACKAGE TYPE E)	500 mW
FOR T_A = +60 to +85°C (PACKAGE TYPE E)	Derate Linearly at 12 mW/°C to 200 mW
FOR T_A = -55 to +100°C (PACKAGE TYPES D, F, K)	500 mW
FOR T_A = +100 to +125°C (PACKAGE TYPES D, F, K)	Derate Linearly at 12 mW/°C to 200 mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES)	100 mW
INPUT VOLTAGE RANGE, ALL INPUTS	–0.5 to V_{DD} +0.5 V
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max.	+265°C

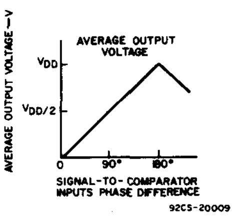


Fig.2 – Phase-comparator I characteristics at low-pass filter output.

of phase-comparator I. Typical waveforms for a CMOS phase-locked-loop employing phase comparator I in locked condition of f_o is shown in Fig. 3.

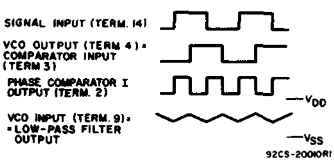


Fig.3 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator I in locked condition of f_o.

Phase-comparator II is an edge-controlled digital memory network. It consists of four flip-flop stages, control gating, and a three-state output circuit comprising p- and n-type drivers having a common output node. When the p-MOS or n-MOS drivers are ON they pull the output up to V_{DD} or down to V_{SS}, respectively. This type of phase comparator acts only on the positive edges of the signal and comparator inputs. The duty cycles of the signal and comparator inputs are not important since positive transitions control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant.

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following range:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply Voltage Range (For T_A = Full Package Temperature Range	3	12	V

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic	Test Conditions	V_O Volts	V_{DD} Volts	Limits All Package Types Min.	Typ.	Max.	Units
Phase Comparator Section							
Operating Supply Voltage, $V_{DD}-V_{SS}$	VCO Operation		–	5	–	15	V
	Comparators only		–	3	–	15	
Total Quiescent Device Current, I_L: Term. 14 Open	Term. 15 open		5	–	25	–	µA
	Term. 5 at V_{DD}		10	–	200	—	
Term. 14 at V_{SS} or V_{DD}	Terms. 3 & 9 at V_{SS}		5	–	5	15	
			10	–	25	60	
			15	–	50	500	
Term. 14 (SIGNAL IN) Input Impedance, Z_{14}			5	1	2	–	MΩ
			10	0.2	0.4	–	
			15	–	0.2	–	
AC-Coupled Signal Input Voltage Sensitivity* (peak-to-peak)	See Fig.7		5	–	200	400	mV
			10	–	400	800	
			15	–	700	–	
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity Low Level			5	1.5	2.25	–	V
			10	3	4.5	–	
			15	4.5	6.75	–	
High Level		V_O Volts	5	–	2.75	3.5	
			10	–	5.5	7	
			15	–	8.25	–	
Output Drive Current: n-Channel (Sink), I_{DN}	Phase Comparator I & II Term. 2 & 13	0.5	5	0.43	0.86	–	mA
		0.5	10	1.3	2.5	–	
	Phase Pulses	0.5	5	0.23	0.47	–	
		0.5	10	0.7	1.4	–	
p-Channel (Source), I_{DP}	Phase Comparator I & II Term. 2 & 13	4.5	5	−0.3	−0.6	–	
		9.5	10	−0.9	−1.8	–	
	Phase Pulses	4.5	5	−0.08	−0.16	–	
		9.5	10	−0.25	−0.5	–	
Input Leakage Current, I_{IL}, I_{IH} Max.	Any Input		15	–	$\pm10^{-5}$	±1	µA

* For sine wave, the frequency must be greater than 1 kHz for Phase Comparator II.

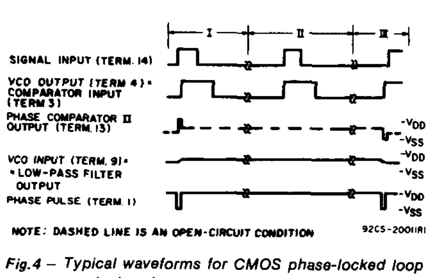


Fig.4 – Typical waveforms for CMOS phase-locked loop employing phase comparator II in locked condition.

CD4046A Types

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic	Test Conditions	V_O Volts	V_{DD} Volts	Limits (All Package Types) Min.	Typ.	Max.	Units
VCO Section							
Operating Supply Voltage $V_{DD}-V_{SS}$	As fixed oscillator only			3	–	15	V
	Phase-lock-loop operation			5	–	15	
Operating Power Dissipation, P_D	f_o = 10 kHz, R_1 = 1 MΩ, $R_2 = \infty$, $VCO_{IN} = \frac{V_{DD}}{2}$		5	–	70	–	μW
			10	–	600	–	
			15	–	2400	–	
Maximum Operating Frequency, f_{max}	R1 = 10 kΩ, $R_2 = \infty$, $VCO_{IN} = V_{DD}$; C1 = 100 pF		5	0.25	0.5	–	MHz
	C1 = 50 pF		10	0.6	1.2	–	
			15	–	1.5	–	
Center Frequency (f_o) and Frequency Range, $f_{max}-f_{min}$	Programmable with external components R1, R2, and C1 *See Design Information*						
Linearity	VCO_{IN} = 2.5 V ± 0.3 V, R1 > 10 kΩ		5	–	1	–	%
	= 5 V ± 2.5 V, R1 > 400 kΩ		10	–	1	–	
	= 7.5 V ± 5 V, R1 = 1 MΩ		15	–	1	–	
Temperature-Frequency Stability•: No Frequency Offset f_{MIN} = 0	$\%/°C \propto \frac{1}{f \cdot V_{DD}}$, $R_2 = \infty$		5	–	0.12–0.24	–	%/°C
			10	–	0.04–0.08	–	
			15	–	0.015–0.03	–	
Frequency Offset $f_{MIN} \neq 0$	$\%/°C \propto \frac{1}{f \cdot V_{DD}}$		5	–	0.06–0.12	–	
			10	–	0.05–0.1	–	
			15	–	0.03–0.06	–	
Input Resistance of VCO_{IN} (Term 9), R_I			5,10,15	–	10^{12}	–	Ω
VCO Output Voltage (Term 4) Low Level, V_{OL}	Driving CMOS-Type Load (e.g. Term 3 Phase Comparator Input)		5,10,15	–	–	0.01	V
High Level, V_{OH}			5	4.99	–	–	
			10	9.99	–	–	
			15	14.99	–	–	
VCO Output Duty Cycle			5,10,15	–	50	–	%
VCO Output Transition Times, t_{THL}, t_{TLH}			5	–	75	150	ns
			10	–	50	100	
			15	–	40	–	
VCO Output Drive Current: n-Channel (Sink), I_{DN}		0.5	5	0.43	0.86	–	mA
		0.5	10	1.3	2.6	–	
p-Channel (Source), I_{DP}		4.5	5	–0.3	–0.6	–	
		9.5	10	–0.9	–1.8	–	
Source-Follower Output (Demodulated Output): Offset Voltage ($VCO_{IN}-V_{DEM}$)	R_S > 10 kΩ		5,10	–	1.5	2.2	V
			15	–	1.5	–	
Linearity	R_S>50kΩ, VCO_{IN} = 2.5±0.3 V		5	–	0.1	–	%
	= 5±2.5 V		10	–	0.6	–	
	= 7.5±5 V		15	–	0.8	–	
Zener Diode Voltage (V_Z)	I_Z = 50 μA			4.5	5.2	6.1	V
Zener Dynamic Resistance, R_Z	I_Z = 1 mA			–	100	–	Ω

• Positive coefficient.

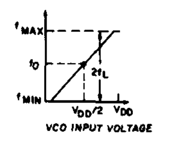
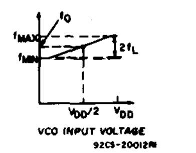
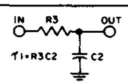
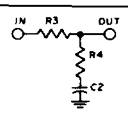
Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 4 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.

DESIGN INFORMATION

This information is a guide for approximating the values of external components for the CD4046A in a Phase-Locked-Loop system. The selected external components must be within the following ranges:

$10\,k\Omega \leqslant R1, R2, R_S \leqslant 1\,M\Omega$
$C1 \geqslant 100$ pF at $V_{DD} \geqslant 5$ V;
$C1 \geqslant 50$ pF at $V_{DD} \geqslant 10$ V

In addition to the given design information refer to Fig.5 for R1, R2, and C1 component selections.

Characteristics	Phase Comparator Used	Design Information: VCO WITHOUT OFFSET $R_2 = \infty$	Design Information: VCO WITH OFFSET
VCO Frequency	1		
	2	Same as for No.1	
For No Signal Input	1	VCO will adjust to center frequency, f_o	
	2	VCO will adjust to lowest operating frequency, f_{min}	
Frequency Lock Range, $2\,f_L$	1	$2\,f_L$ = full VCO frequency range	
	1	$2\,f_L = f_{max} - f_{min}$	
	2	Same as for No.1	
Frequency Capture Range, $2\,f_C$	1		(1), (2) $2\,f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$
Loop Filter Component Selection	1		For $2\,f_C$, see Ref. (2)
	2	$f_C = f_L$	
Phase Angle Between Signal and Comparator	1	90° at center frequency (f_o) approximating 0° and 180° at ends of lock range ($2\,f_L$)	
	2	Always 0° in lock	

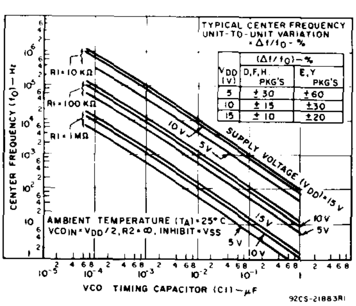


Fig.5(a) – Typical center frequency vs C1 for R1 = 10 kΩ, and 1 MΩ and $f_o \sim 1/R1\,C1$.

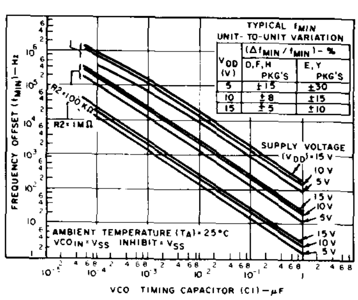


Fig.5(b) – Typical frequency offset vs C1 for R2 = 10 kΩ, 100 kΩ, and 1 MΩ.

NOTE: Lower frequency values are obtainable if larger values of C1 than shown in Figs. 5(a) and 5(b) are used.

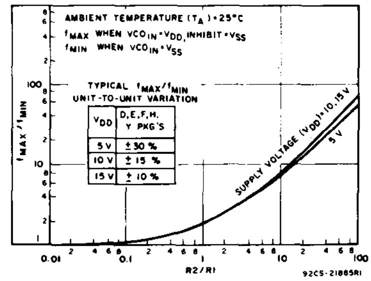


Fig.5(c) – Typical f_{max}/f_{min} vs R2/R1.

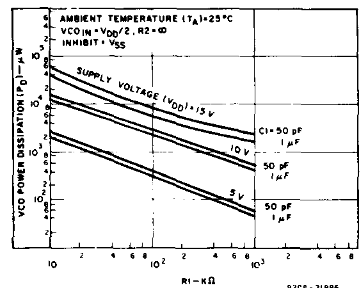


Fig.6(a) – Typical VCO power dissipation at center frequency vs R1.

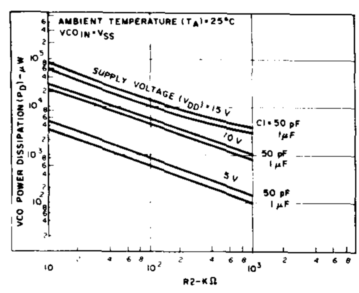


Fig.6(b) – Typical VCO power dissipation at f_{min} vs R2.

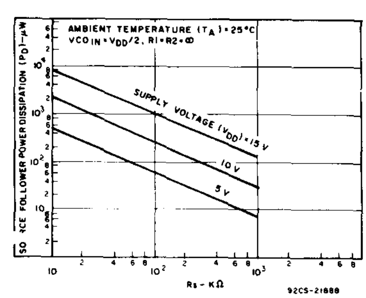


Fig.6(c) – Typical source follower power dissipation vs R_S.

NOTE: To obtain approximate total power dissipation of PLL system for no-signal input

P_D (Total) = $P_D(f_o) + P_D(f_{MIN}) + P_D(R_S)$ – Phase Comparator I

P_D (Total) = $P_D(f_{MIN})$ – Phase Comparator II

DESIGN INFORMATION (Cont'd):

Characteristics	Phase Comparator Used	Design Information	
Locks On Harmonic of Center Frequency	1	Yes	
	2	No	
Signal Input Noise Rejection	1	High	
	2	Low	
VCO Component Selection		VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET
	1	– Given: f_o – Use f_o with Fig.5a to determine R1 and C1	– Given: f_o and f_L – Calculate f_{min} from the equation $f_{min} = f_o - f_L$ – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ from the equation $\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1
	2	– Given: f_{max} – Calculate f_o from the equation $f_o = \frac{f_{max}}{2}$ –Use f_o with Fig.5a to determine R1 and C1	– Given: f_{min} & f_{max} – Use f_{min} with Fig.5b to determine R2 and C1 – Calculate $\frac{f_{max}}{f_{min}}$ – Use $\frac{f_{max}}{f_{min}}$ with Fig.5c to determine ratio R2/R1 to obtain R1

For further information, see

(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966

(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

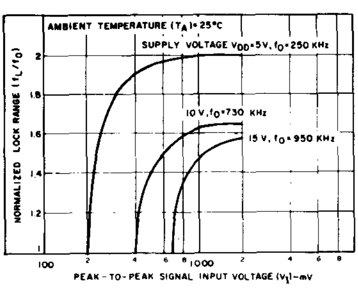


Fig.7 – Typical lock range vs signal input amplitude.

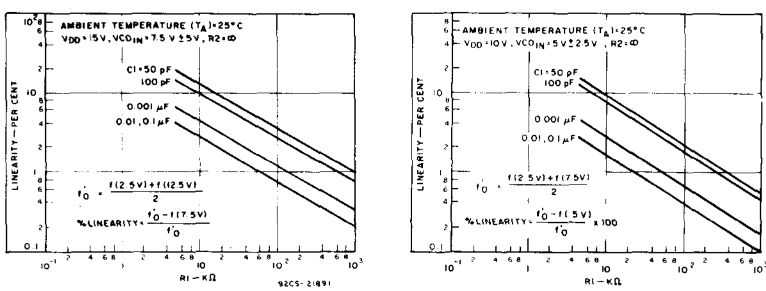


Fig.8(a) and (b) – Typical VCO linearity vs R1 and C1.